

Final Project Report

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I. INTRODUCTION

THIS is the project report for the implementation of a standard five-stage pipelined 32-bit MIPS processor in VHDL.

II. METHODOLOGY

- A. Instruction Fetch*
- B. Instruction Decode*
- C. Execute*
- D. Memory*
- E. Write-back*

III. RESULTS AND DISCUSSION

IV. OPTIMIZATION

V. LIMITATIONS

VI. CONCLUSION