Instrumentation II

CH – 08
Circuit Layout

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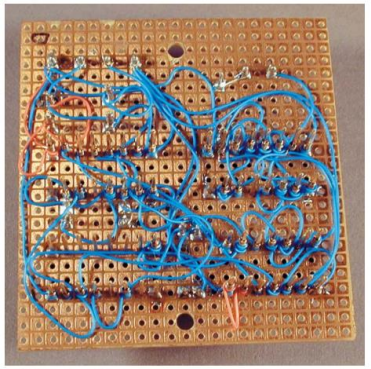
Circuit Layout

- ✓ Poorly selected placement, packages, and routing will increase:
  - noise
  - susceptibility
  - EMI in electronic circuits.

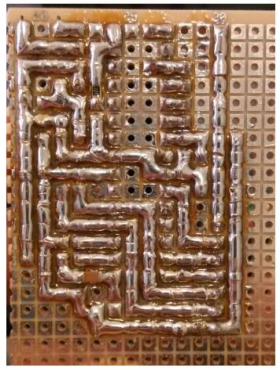
- ✓ Circuit boards combine electronic components and connectors into a functional system through **electrical connections** and **mechanical support**.

Circuits Boards and PCBs

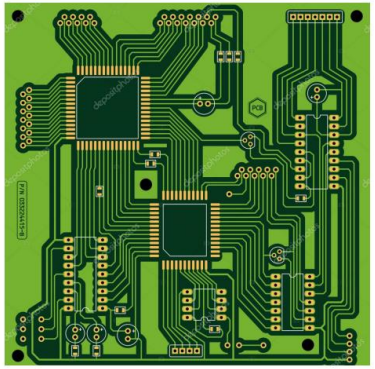
- ✓ Wire wrap
  - suitable for prototype development
  - limited in operation to less than 5 or 10 MHz (above that loop inductances reduces performance)
- ✓ Stitch weld
  - wire is welded to the pins, not wrapped;
  - loop inductances are lower and allows 100 MHz operation
  - Stitch weld resists vibration and shock
- ✓ PCBs
  - etched and plated connections
  - suited for both manufacturing and rugged environments
  - automated placement and soldering of components possible.



Figures: Wire wrap



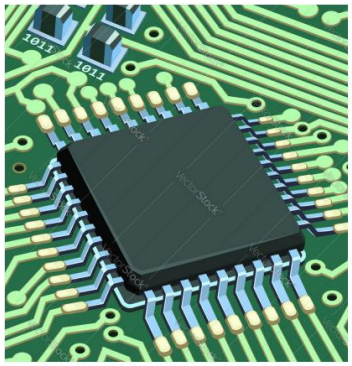
Stitch weld



PCB

Circuits Boards and PCBs

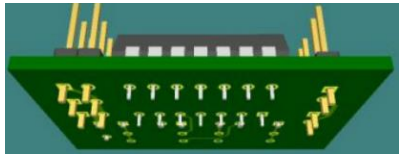
- ✓ MCMs (Multi-Chip Modules):
  - **Higher** levels of **circuit density** by bonding the bare die of ICs onto a substrate.
  - Compact packaging of MCMs **improves signal speeds** and reduces load capacitance.

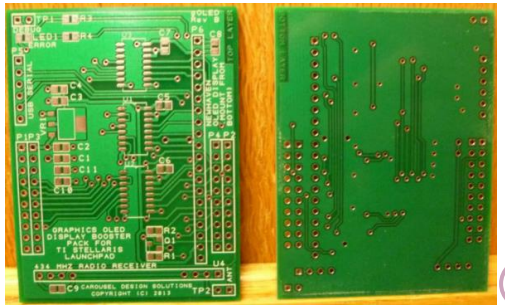


Chip on board

MCM.

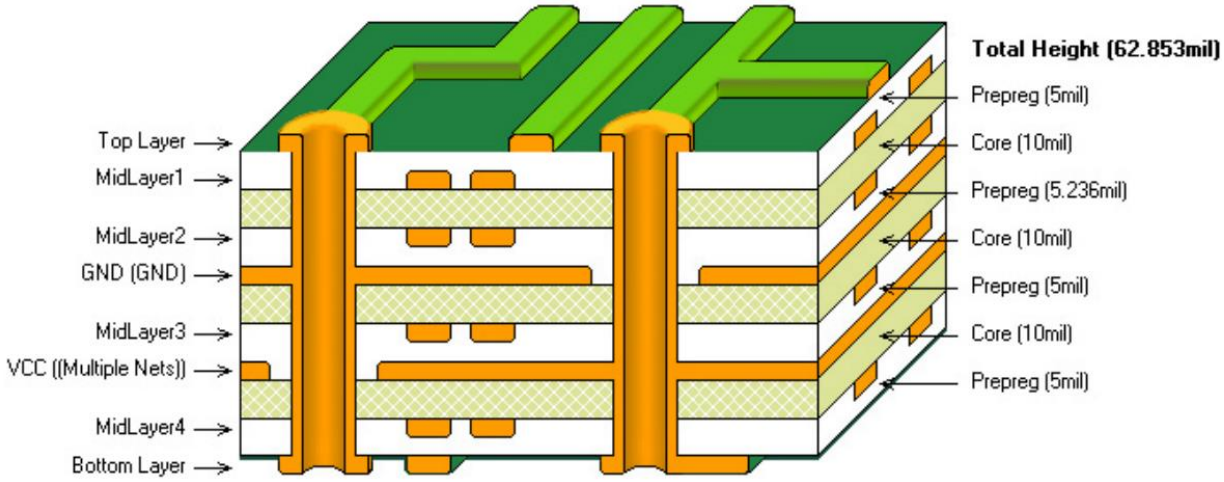
- ✓ Printed Circuit Boards (PCBs)
  - Contain layers of insulating material and copper conductors with plated holes, called **vias**, to interconnect the conductors and fixed connecting wires called tracks
  - Types:
    - Single-Sided PCB: signal traces are on only one side, does not use plated-through holes.
    - Double-Sided PCB: signal traces on both sides of the circuit board, dense, support higher-frequency operation





✓ Multilayer PCB

- stack of alternating layers of copper-clad laminate, or **core, and prepreg.**
- very dense circuit connections
- control impedance much more tightly
- absolutely necessary for high-frequency circuits.
- Through-hole, buried, and blind vias connect signal paths on different layers together.



Component Placement

- ✓ Improper layout can degrade operation or even prevent a circuit from working.
- ✓ We should **group** circuits **according to their characteristics**.
- ✓ In general, follow these rules:
  - Group **high-current circuits near the connector** to isolate stray currents and near the edge of the PCB to remove heat.
  - Group **high-frequency circuits near the connector** to reduce path length, crosstalk, and noise
  - Group low-power and low-frequency circuits away from high-current and high-frequency circuits.
  - Group analog circuits separately from digital logic.

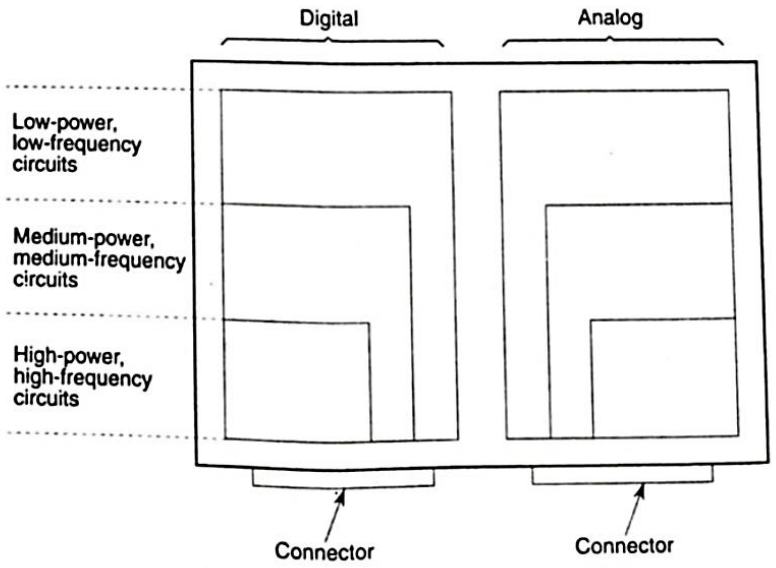


FIG. 8.7 Grouping of components. Arrange high-power and high-frequency circuits near the connector and away from the low-power circuits.

Routing Signal Tracks

- ✓ Principles to know before designing PCBs:
  - Signal propagation
  - Circuit layout
- ✓ Poor layout causes:
  - false triggering of logic, setup and hold violations, and transmission delays
- ✓ **1. Trace density** (lines per unit area) determines:
  - Number of signal layers, the size of the PCB, and cost.
  - Higher trace densities - provide flexibility in packaging and reduce the cost of materials.
  - Tradeoff - greater cost and difficulty in producing and may degrade signal integrity.

Routing Signal Tracks

✓ 2. Common Impedance

- **Minimize** the number of circuits that share the **same return path**.
- Voltage drops (caused by current switching) on the ground line (return path) increase system noise.
- Use **unbroken return plane** to lower the effective impedance

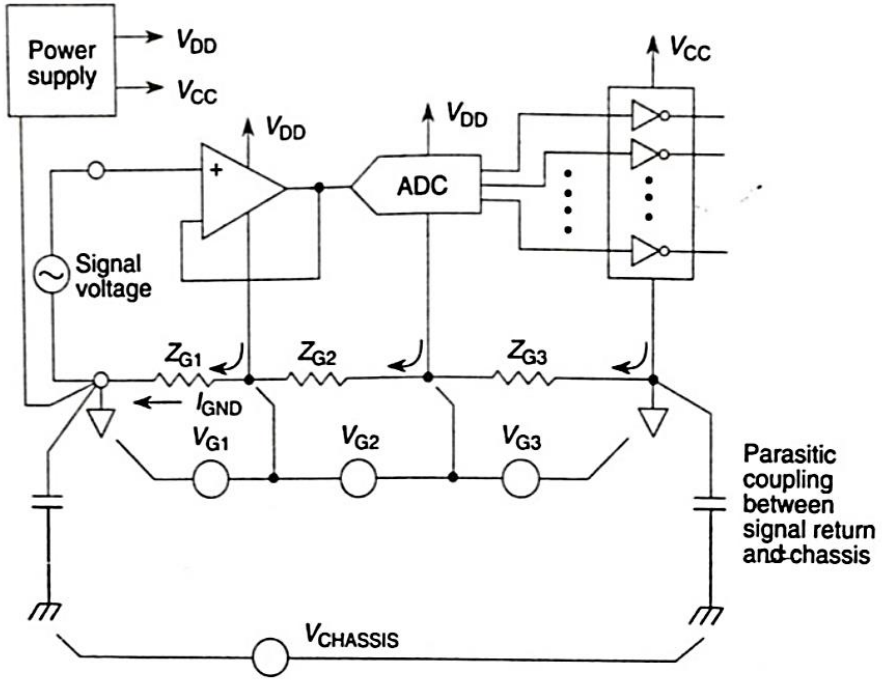
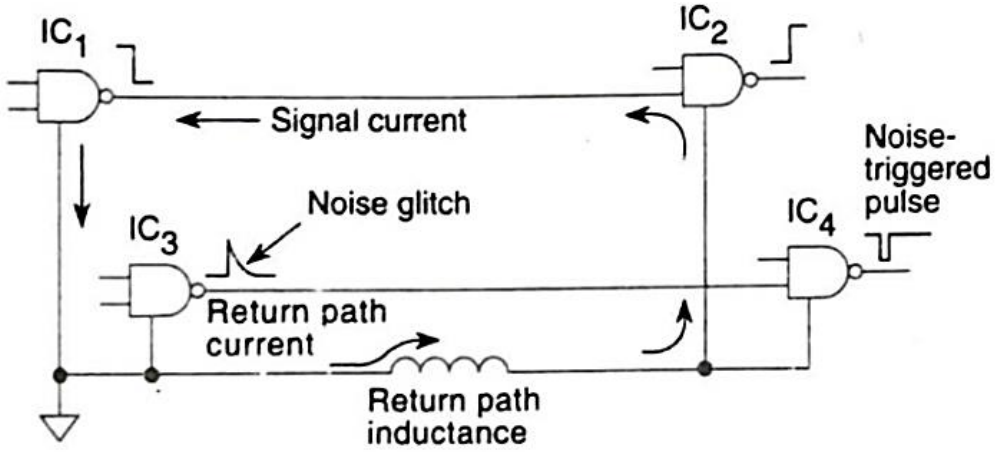


FIG. 8.8 Common impedance. Common-impedance paths cause components to reside at different ground potentials from one another. Larger common impedance will cause larger ground potentials (V_{G1}, V_{G2}, V_{G3}) and coupling to the chassis ($V_{CHASSIS}$); these will bias the signal voltage and introduce error.

Routing Signal Tracks

✓ 3. Distribute Signal and Return Carefully

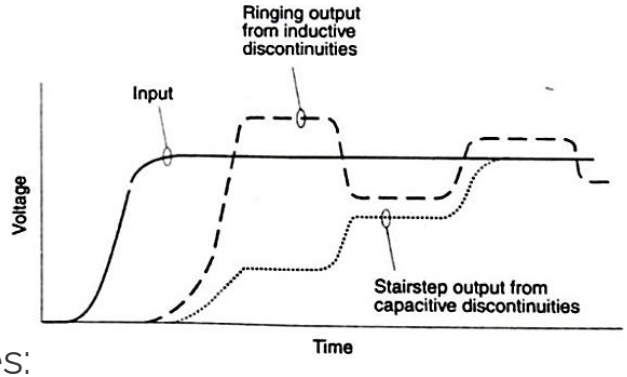
- Long return (ground) paths can shift the ground potential excessively.
- At higher frequencies the current tries to return in the plane directly below the signal trace.
- If the return is longer than the signal, then the current has a high inductance path.



Routing Signal Tracks

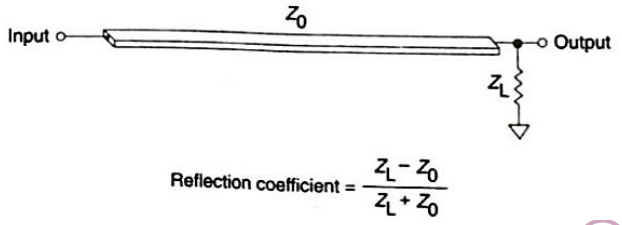
✓ 4. Transmission Line Concerns

- Signal conductors are never ideal transmission lines.
- Dispersion: Square waves or pulses have multiple harmonics, and higher frequencies attenuate more than lower frequencies. Also, different frequencies propagate at different speeds.
- Propagation delay: depends on both **interconnection length** and **signal velocity**. Can be reduced by interconnection length and low dielectric constant, in the PCB.
- Line resistance, skin effects, and dielectric losses



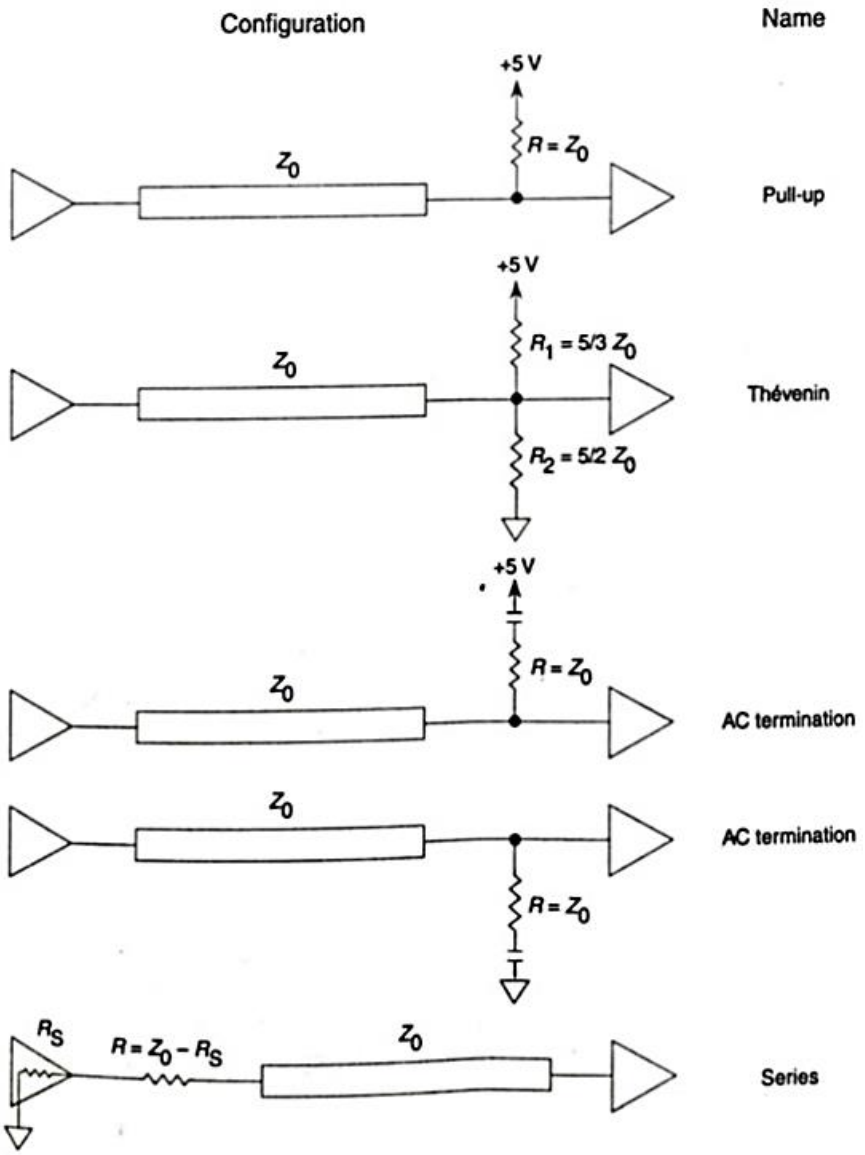
✓ 5. Trace Impedance and Matching

- Lower Z0 → Less susceptible to interference.
- Impedance mismatches lead to reflections that causes:
  - Delay switching
  - Trigger logic falsely.



Routing Signal Tracks

- ✓ Ways for impedance matching:
  - Tailor both the **dielectric constant** of the PCB materials between signal traces and the return plane.
  - Keep wire **bonds and leads short** in IC packages to reduce inductive impedance
  - **Terminate** the signal trace appropriately



Routing Signal Tracks

✓ 6. Avoiding Crosstalk

- 1. Don't run parallel traces for long distances, particularly asynchronous signals.
- 2. Increase separation between conductors.
- 3. Shield clock lines with guard strips.
- 4. Reduce magnetic coupling by reducing the loop area of circuits.
- 5. Sandwich signal lines between return planes to reduce crosstalk.
- 6. Isolate the clock, chip-select, chip-enable, read, and write lines (because crosstalk occurs in synchronous systems on the pulse edges when data are sampled).

- You will have to balance noise, EMI, and trace density.

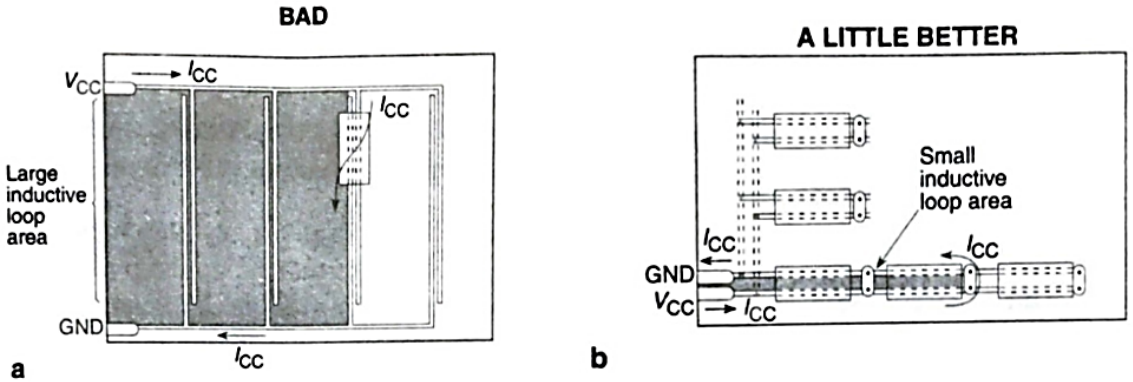
Ground, Returns and Shields

✓ Grounding

- The signal reference should be a **single point** that is as **close** as possible to the **power entry** to the PCB.
- A ground plane connected to the single-point reference will also reduce common impedance.

✓ Distribute Power and Return Carefully

- Lay out the power and return together and symmetrically, or in a grid.
- Use multilayer PCB with power and return (or ground) planes

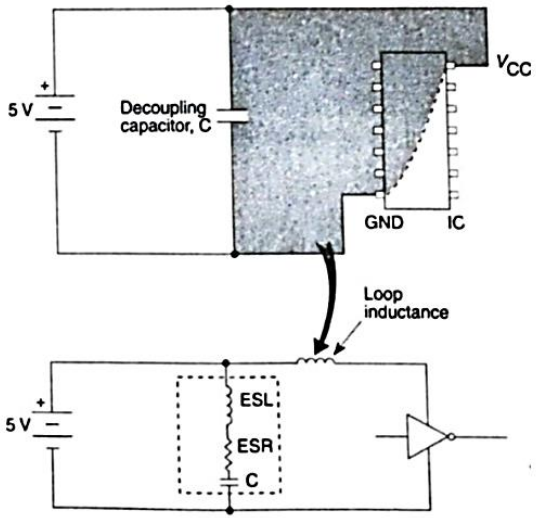


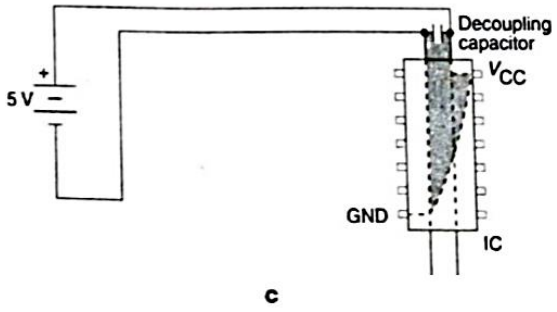
(a) Interleaved combs arrangement can create large loops.
(b) Running power and return together reduces the loop area.

Ground, Returns and Shields

✓ Shielding

- A **return (or ground) plane** is the **most effective shield** for any circuit.
- Power and return planes provide circuit paths with the lowest impedance.
- 1. Use power and return planes with minimum separation.
- 2. Place decoupling capacitors near (or in) IC packages.
- 3. Don't disrupt the power and return planes with slots or traces.
- 4. Route digital traces over digital return and analog traces over analog return.
- 5. Fill the **regions between analog traces with copper** foil and connect to ground.

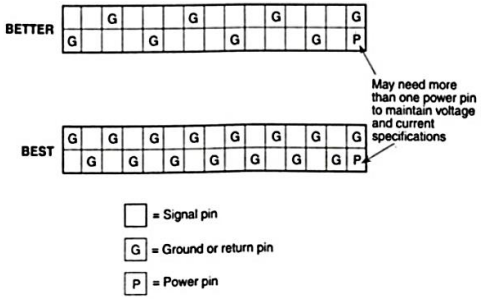




Cables and Connectors

✓ Connectors are the mechanical and electrical interface between a cable and a circuit board.

- They have two pieces that fit together and **hold through friction**.
- The metal-to-metal contact **provides the electrical path**.
- 1. Preassign connector ground pins.
- 2. Distribute and intersperse grounds (return paths).
- 3. Place clock next to a ground line.
- 4. Minimize I/O.
- 5. **Use long rise and fall times** to reduce high frequency harmonics.
- 6. Keep **current to less than 1 A per connector** pin; otherwise use multiple pins or special pins with large current capacity
- **Shape or keying polarizes** a connector so that it cannot be plugged in the wrong way



Testing and Maintenance

- ✓ Testing and maintenance have five levels:
  - Component, Circuit, Board, Module, Instrument.
- ✓ Testing and maintenance do not predict problems, but they can **shorten the time to repair**.
- ✓ **Testing**
  - **Scan Testing** - Stimulates points within a chain of circuitry, records the results, and compares them with expected or calibrated data.
  - **Functional Testing** - Tests exercise a subset of all the operations that the circuit may generate.
  - **BIT (Built-in self-test)** - Usually dedicates some circuitry for testing the remainder of the system; it can implement scan or functional tests.

Testing and Maintenance

- ✓ Good layout and design will accommodate **testing at various levels** during production by making parts of the **circuit accessible**.
  - **Partition the system**, both functionally and physically, so that faults can be detected independently.
  - Make circuits testable without the front panel.
  - Provide test outputs **compatible with standard test equipment**.
  - Eliminate warm-up problems or delays to allow rapid testing
- ✓ **Maintenance**
  - If throwaways - maintenance is not a consideration.
  - Others, like control processors for a traffic light system, require extensive planning, support, and maintenance to run smoothly for years.
  - Concerns in the maintenance of circuit boards are **access and ease, support equipment, and instruction and repair manuals**.
  - Design for maintenance should make circuit boards easy to **locate, disconnect, and remove**.