Data Acquisition & Microcontroller/PC Interfacing

5.1> Introduction

⇒ Data can be in the form of analog or digital signals.

5.2> Sampling Theory

⇒ In converting Analog Signal to digital signal, the analog signal is "sampled" to obtain the digital value.

{Read as defined time instances}

⇒ We must be very careful in performing the Sampling operation so that the analog signal characteristic do not get distorted in the sampling process.

↳ This requirement for proper sampling is given by "Shannon's sampling theorem".

↓

Sampling frequency should be at least twice that of the highest frequency in the signal.

{Otherwise, distortion (or aliasing) in the sampled signal will occur}

⇒ In practice, a Sampling rate of at least five times higher than the highest frequency in the signal is typically used.

5.3> Analog to Digital Converter

↳ Hardware device for converting analog signal to digital signals

⇒ To prevent variation in the input signal from affecting the output while the conversion is taking place, the analog signal is first passed through a Sample & hold circuit (which holds the input voltage) before it is converted.

* A/D Characteristics

- Conversion rate
- Voltage range
- Bit resolution
- Quantization error

Conversion Rate → How many conversions are performed in a unit of time.

↳ On micro controller Conversion rate depends on:-

- Clock Speed
- Bit range

Voltage Range → Analog Voltage range the device can handle.

Bit resolution → Number of bits that the Converted analog signal is mapped into.

Voltage resolution = Range / 2^n

{bit resolution}

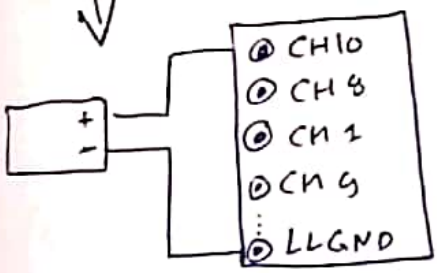
Quantization error → uncertainity in the discretized Voltage value.

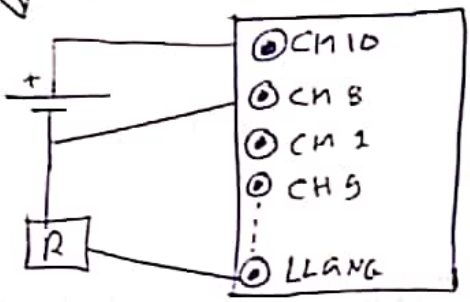
* A/D Operation

⇒ Most A/D Converters are built to operate on the Principle of successive approximation.

* A/D Input Signal Configuration

→ Single ended input
→ Differential input





⇒ Sensitive to noise, Since Signal wire can act as antenna picking up electrical noise

⇒ Better Configuration for handling noise than Single-ended mode.

↓

Electromagnetic interference induced in one lead of the signal is usually induced in the other lead.

↓

Since differential input mode measures difference effect is canceled.

The measure of the ability of ADC in differential input mode to eliminate the common voltage is called CMRR

↓

{Common mode rejection Ratio}

5.4> Digital to Analog Converter

★ **D/A Characteristics**

↳ Most microcontrollers do not have a D/A Converter, but the function of the D/A Converter is approximated on microcontrollers using the PWM Output feature.

★ **D/A Operation**

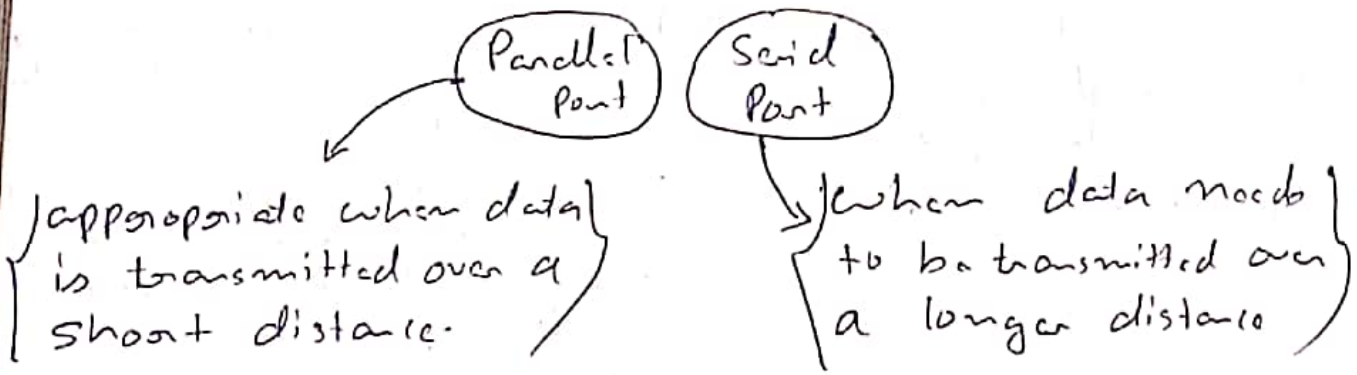
→ Weighted resistor Summing ~~op~~ amplifier circuit.

↳ R2R Ladder

5.5> Parallel Port

↳ A Connector for a device that sends or receives several bits of data simultaneously by using more than one wire.

5.7> USART Serial Port (Universal Synchronous Asynchronous Receiver Transmitter)



⇒ Serial Connection normally require fewer wires than a parallel connection.

↳ In Serial port, the data is transmitted one bit at a time.

⇒ The speed of transmission or baud rate refers to number of bits per second that can be transmitted.

⇒ Serial data can be transmitted in a asynchronous or in a synchronous fashion.

⇒ **Asynchronous** → Used when transmitter & the receiver operate independently each using its own clock signal.

Synchronous → Used when transmitter & receiver have a common clock signal.

⇒ Asynchronous transmission is the default on PC's.

⇒ In asynchronous transmission, means must be provided to inform the receiver of the start & end of a data packet, since the timing of the transmission of the packet is not known in advance.

⇒ This a accomplished by structuring the data packet to include :

→ **Start bit** → { at beginning to inform receiver of the start of the packet }

→ **Stop bit** → { at the end to indicate its completion }

→ **Parity bit** → { can be used to provide a crude method of error checking }

⇒ The different Parity method are listed here:-

* Even: Means that the total number of one bits in the packet is even.
  ↓
  Parity bit is set to 1 or 0 to make the total number of one bits even.

Odd: Means the total number of one bits in the Packet is even.
  ↓
  Parity bit is set to 1 or 0 to make the total number of one bits odd.

Mark: Parity bit is always set to logical 1

* Space: Parity bit is always set to logical 0

None: No parity bit is sent at all.

Full-duplex mode → Data can be transmitted simultaneously in both direction.

Half-duplex mode → Data is transmitted in one direction at a time, but the direction can be changed

⇒ There are several protocols for Serial interface.
  ↳ Most common is RS-232C protocol.

⇒ RS-232 Stands for recommended Standard number 232, and C is the latest revision of the standard.

- A Subset of RS-232C protocol is used in the Serial ports on most computers.
- It has limits on speed, cable distance & device support.

⇒ RS-422 permits longer cable distances at higher cost, since each signal is carried by two wire due to use of differential mode in signal transmission.

⇒ To prevent overflow of the buffer that receives the data, handshaking or flow control method can be used.

- Software based flow Control
- Hardware based flow control
- Combination of two

→ XOnXOff (Transmit on/Transmit off)

- If the receiver is ready to accept characters, it will send an XON character to the transmitter.
- If the receiver buffer is full, it will transmit an XOFF character to the transmitter to stop the transmission of data.

Hardware based

→ Request to Send (RTS) & Clear to Send (CTS)

→ If the input buffer is not full, the RST line will be set to true indicating that the receiver can accept characters.

→ If the input buffer becomes full, the RTS line will be set to false.

⇒ Both RTS & XON/XOff Control can also be used at the same time.

⇒ Common method of using USART on a PICMCU is to implement full duplex asynchronous serial communication using the RS-232 protocol.

PIC16F690

→ USART has → 2 char input buffer
→ 1 char output buffer

→ It allows 8 or 9 bit char length

→ Has means to detect input buffer overrun errors & received char framing error.

→ Serial packet not in the expected format

⇒ The USART allows a range of baud rate setting that are dependent on the Oscillator clock frequency.

⇒ The SPBRG register Controls the period of the baud rate generator (BRG) which is implemented as a free-running, 8-bit timer.

⇒ PIC MCU allows two range of baud rates:
- Low
- High

⇒ BRGH bit of TXSTA register.
- Set to 1 for high range.
- Set to 0 for low range.

Desired baud rate (low speed) = $F_{osc}/64(X+1)$ {BRGH=0}

Desired baud rate (High speed) = $F_{osc}/16(X+1)$ {BRGH=1}

X → Value written into SPBRG register.
(0-255)

⇒ When using a high-level compiler, the user does not need to write to these register to set up the baud rate.
- Compiler provides function for this purpose.