Anjuman-i-Islam's

M. H. Saboo Siddik College of Engineering

8, Saboo Siddik Polytechnic Road, Byculla, Mumbai-8

Internal Assessment Examination –I (IAE-I)

August 2025

Blueprint for Students Information

Course Code:	2113114	Course Name: Computer Organization and Architecture [COA]	Sem: III

Table 1: Course objectives and Outcomes

Course Objectives	
CO1	To study the fundamentals of number system and arithmetic operations.
CO2	To equip students with the foundational knowledge of computer organization and architecture, fostering an understanding of how hardware and software components collaborate to execute tasks.
CO3	To prepare students to design and optimize computing systems for real-world applications.
Course Outcomes	
CO.1	To conceptualize basic computer structure with its models.
CO.2	To design algorithms to solve ALU operations.
CO.3	To comprehend processor organization with various control signal design methods of CPU with comparative analysis.
CO.4	To design memory systems with analysis of mapping techniques for cache memory.
CO.5	To explore different types of I/O buses, examine data transfer methods, and assess arbitration techniques for optimized system performance.
CO.6	To analyze different parallel organizations that includes pipelined and parallel processors.

Table 2: Detail Syllabus Modules for IAE-I

Module No.	Content/ Sub Modules	CO	No of Hrs in Syllabus	Marks Weightage	% of Syllabus	Marks Range (Including Options) [20-32]
1	**Computer Fundamentals**	**1**	**04**	**25%**	**10%**	**5 - 8**
	Number Systems: Binary. Octal and Hexadecimals. Binary Number representation: Sign Magnitude, 1's and 2's Compliment representation. Logic Gates: AND, OR, NOT, NAND, NOR, EX OR. Basic Organization of Computer, Von Neumann model.					
2	**ALU Operations**	**2**	**08**	**50%**	**21%**	**10 - 16**
	ALU Operation: Addition and Subtraction on Binary, Octal, Hexadecimal number. Booth's Algorithms, Restoring and Non restoring division algorithm. IEEE 754 Floating point representation and conversation.					
3	**Processor Organization and Control Unit Design**	**3**	**04**	**25%**	**10%**	**5 - 8**
	8086 Processor: Architecture of 8086 processor, Register Organization, Instruction formats, instruction cycle, addressing modes.					

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