Assignment for Week 2

IOT103TC

1. Consider a two-level memory hierarchy consisting of a cache memory M_1 and the main memory M_2. Suppose that the main memory is 8 slower than the cache. 20% of the times, processor misses to get data from the cache. Still, we believe that cache is useful. Can you find how much speedup do we gain by using the cache?
   Hint: lecture 8, part 2, slide 3

   Solution:
   $R = tA_2/tA_1 = 8$, $H = 1-0.2$
   $S = 1 / ((H/R) + (1-H)) = 3.33$

2. While learning memory for the first time, a student understands the importance of signal Read_Enable/Write_Enable (RE/~(WE)). However, (s)he learns that there is another signal named Chip_Select (~CS). (S)he thinks that this signal is not required at all. How can you say if (s)he is wrong and ~CS signal is very important?

   Solution:
   ~CS (Chip Select) signal enables or disables the memory chip to perform any operation. Once Chip Select signal is enabled, only then read or write operations can take place using RE/~(WE) signals.

3. Consider a case when you have a memory of with 4096 locations. Each location can hold 32-bit word. The CPU wants to fetch the data from the memory location 0x2012. What will be the binary value for this location's address? In which CPU register will this address be stored?
   Hint: Convert Hex address to the decimal if confused.

   Solution:
   The 0x2012 means 8210 in decimal. Since there are only 4096 locations available, and 8210 > 4096, hence the CPU cannot fetch anything from the memory because the required address is larger than the available memory.

4. What is the access time for a 5-level access cache considering the following H_{Lx} = Hit ratio of level x, t_{Lx} = access time of M_x, t_{MISS} = miss penalty, can also be considered as T_{L3} ?
   Hint: See Lecture 8, part 2, slide 6
   Solution:

5. You are given memory chips of 256M x 8 size. It is required of you to make 4GX8 memory unit. How can you do that?
   Hint: Lecture 7 Part 2

Solution:

Q5 Ans. 2

256M x 8 memory chips available. We need to make 4G x 8 memory.

Solution

=> To make 4G x 8 memory from 256M x 8 memory chips, we need:

$$(256M \times 8) \times n = 4G \times 8$$

$$n = \frac{4G}{256M} = \frac{4M \times 1024}{256M} = 16$$

$$n = 16$$

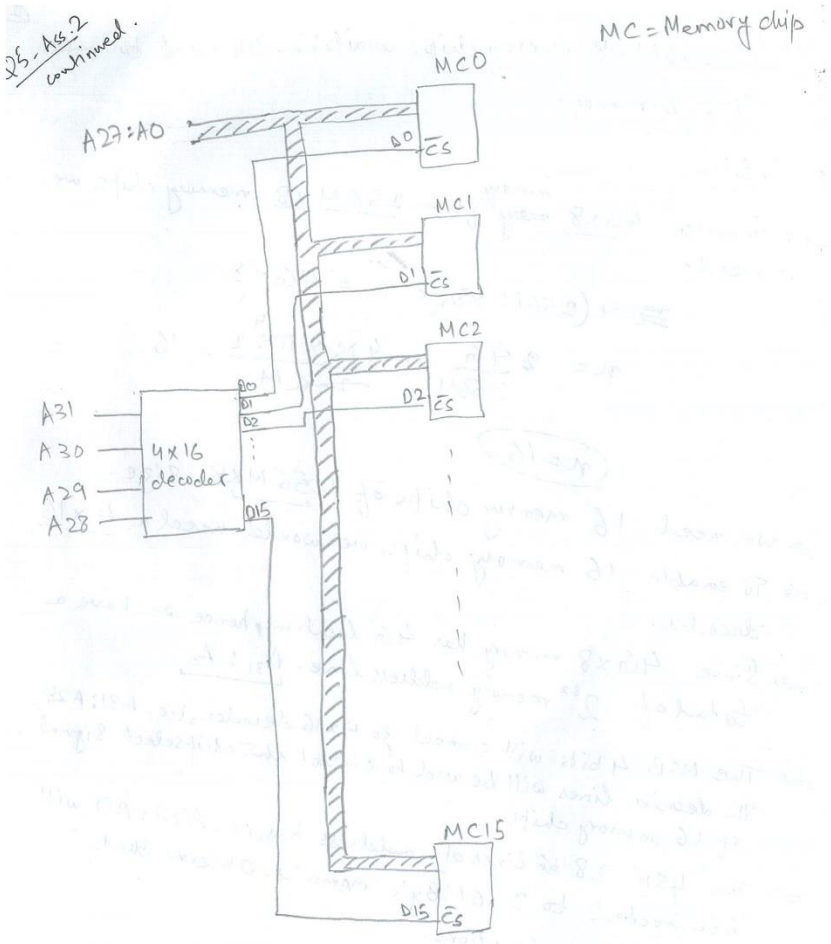
=> we need 16 memory chips of 256M x 8 size.

=> To enable 16 memory chips, we would need a 4 x 16 decoder.

=> Since 4G x 8 memory has 4G locations, hence we have a total of 2^{32} memory address line. $A_{31} : A_0$

=> The MSB 4 bits will connect to 4 x 16 decoder, i.e. A31 : A28. The decoder lines will be used to control the chipselect signal of 16 memory chips.

=> The LSB 28 lines of address bus, i.e. A27 : A0 will be connected to 256MByte memories. Observe that 2^{28} = 256 Mega locations.



6. Consider a 4-level memory hierarchy in which CPU is connected to L1-Cache, which is connected to L2-Cache. The L2-Cache is connected to the memory, and the memory is connected to the hard drive. If the hit-ratio (or hit-percentage) of level L1 is H1, for L2 it is H2, for Memory it is H3, for hard drive it is H4. Which level would have highest and lowest hit ratio, and why?

   Answer:
   The highest level of the cache, i.e. hard-drive have the highest hit ratio, i.e. $H_{hard\text{-}drive} = 1$. L1 cache has the lowest hit-ratio. It is because, if CPU require some data or instruction, it will first search in L1 cache, if the information is not found in L1 cache, it is looked at in the higher level, i.e. L2 cache. If the information is absent even in the L2 cache, then it will be looked at in memory. In case even if memory does not have the information, then the hard-drive must have the information which means if CPU access hard-drive, it will never be a MISS and a 100% hit ratio.

7. Continuing Q3, what would the expression of access time of all levels in terms of H1? Furthermore, What would be the total access time in terms of H1?

8. A CPU has a 16 bit memory address register (MAR). What is the maximum size of memory that this CPU can support?

   Solution:

   16-bit MAR means that the largest value MAR can have is 2^{16}-1 = 64 Kilo – 1. Hence, the maximum size of memory that CPU can support can have 64K locations.

9. A CPU has an address line of 22-bits. What maximum size of memory can this CPU support?

   Solution:

   22-bit address line means 2^{22} = 4 Mega locations are accessible by CPU.

10. A student knows that there are two special purpose registers inside the CPU that can store addresses of memory locations, namely program counter (PC) and Memory Address Register (MAR). However, the student is confused about how these two registers are different from each other. Do they have same task? If yes, then why do we need two of them? Can you solve his/her problem by explaining in simple words about these two registers and the difference they may have?

11. What is the significance of control signals?

    Answer: As the name suggest, control signals are used to control operations of CPU, Memory, or I/O devices and modules. Some example of control signals are Chip Select (CS) signal, which activates the chip, Read/Write Enable signal, which allow either, read or write operation on the memory etc.