Final Assignment for IOT103TC
Computer Architecture Part

1. Give the relationship that represents the dual of the Boolean property A + 1 = 1? (Note: * = AND, + = OR and ' = NOT)
   i. A * 1 = A
   ii. A * 0 = 0
   iii. A + 0 = A
   iv. A * A = A
   v. A`* 1 = A`
   vi. A+A` = 1
   vii. A` + 1 = 1

2. Given inputs A, B, C, D. How can you represent the De-Morgan's laws for 3-input system and 4-input system?

3. Simplify the Boolean expression (A+B+C)(D+E)' + (A+B+C)(D+E) and choose the best answer.
   i. A + B + C
   ii. D + E
   iii. A'B'C'
   iv. D'E'
   v. None of the above

4. Given the function f(X,Y,Z) = XZ + Z(X'+ XY), the equivalent most simplified Boolean representation for F is: (Also show how you come to the conclusion).
   i. Z + YZ
   ii. Z + XYZ
   iii. XZ
   iv. X + YZ
   v. Z
   vi. None of above

5. Simplification of the Boolean expression (A + B)'(C + D + E)' + (A + B)' yields which of the following results? (Also prove how you come to the conclusion)
   i. A + B
   ii. A'B'
   iii. C + D + E
   iv. C'D'E'
   v. A'B'C'D'E'

6. Given that F = A'B'+ C'+ D'+ E', which of the following represent the only correct expression for F'? (Also prove how you come to the conclusion)
   i. F'= A+B+C+D+E
   ii. F'= ABCDE
   iii. F'= AB(C+D+E)

iv. F'= AB+C'+D'+E'
v. F'= (A+B)CDE

7. Simplification of the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF yields which of the following results? (Also show how you come to the conclusion).
   i. ABCDEF
   ii. AB
   iii. AB + CD + EF
   iv. A + B + C + D + E + F
   v. A + B(C+D(E+F))

8. You are given memory chips of 1 Mega x 16 size. (This is a typing mistake. It is not 1 Mega, but 1 Giga x 16 memory)
   a- What will be the width of address and data buses for memory chips of 1 G x 16?
   Address bus width for 1Giga locations = 30 bits (because 2^{30} = Giga.)
   Data bus width = 16 bits.
   b- How many total bits of data can 1 G x 16 size chip store?
   Total bits 1G x16 memory can store = 2^{30} x 2^4 = 2^{34} bits = 16 Giga bits.
   c- How to make $8G \times 16$ memory unit from multiple 1G x 16 memory chips? How many 8G x 16 memory chips will be required? MUST Show with the diagram, and also explain in words. (This answer is similar to previous assignments and hence its solution is not provided here)

   d- What will be the width of address and data buses for the memory of $8\ G \times\ 16$?
   Address bus width for 8Giga locations = 33 bits (because 2^3 = 8 and 2^{30} = Giga.)
   Data bus width = 16 bits.

9. If caches are fast memories, why cannot we have ONLY large sized cache instead of SDRAM or hard drive as memory storage?

   Answer: (First of all, use internet to find the answer to this question. A smaller version is presented in the following)
   Because caches are expensive in terms of cost as well as space. Caches are made from static memory technology which have higher cost per bit as well take more space on the chip.

10. Von-Neumann machines have a popular and robust architecture. However, what benefit you can think of while considering Harvard architecture? What are negatives of having Harvard architecture instead of Von-Neumann?

    Answers: (First of all, use internet to find the answer to this question. A smaller version is presented in the following)
    One benefit of Harvard architecture is that it has less congestion on channels since there are different channels (paths) for instruction and data. The side-effect of having such an architecture is that we will need more space on the chip for separate instruction and data lines. Due to separate lines, Harvard architecture may consume more energy as compared to Von-Neumann which has shared lines/buses for both data and instructions.

11. A 16-bit wide memory has its addresses starting from 0x0000 and ending at 0x100000000.
    i. What is to the total size of memory?
        4 Giga x 16 memory size or 64 Gigabits.
    ii. What is the total size of memory in terms of Bytes?
        4 Giga x 16 memory => 4 Giga x 2x8 memory => 8GigaByte memory => 8GB.
12. If addresses from 0x0000 to 0x0400 are reserved for system use, how much memory is available for the user?
    Memory available for users = 0x100000000 – 0x400 (Hexadecimal operation)
    = 0xFFFFFC00
    = 4294966272 (in decimal)
    divide by 2^{30}, we get 3.99 Giga memory locations for user
    i. How much memory size in terms of Bytes (e.g. Mega Bytes) is reserved for system?
    0x0000 to 0x0400 reserved for system which is equal to 1024 locations of 16 bit each.
        ⇨ 1024 x 16 => 1024 x 2 x 8 = 2 KiloByte = 2KB.
    ii. What is the size of address bus for the memory?
    Address bus size = 9 bits

    iii. What is the size of data bus for the memory?
    Data Bus size 16 bits

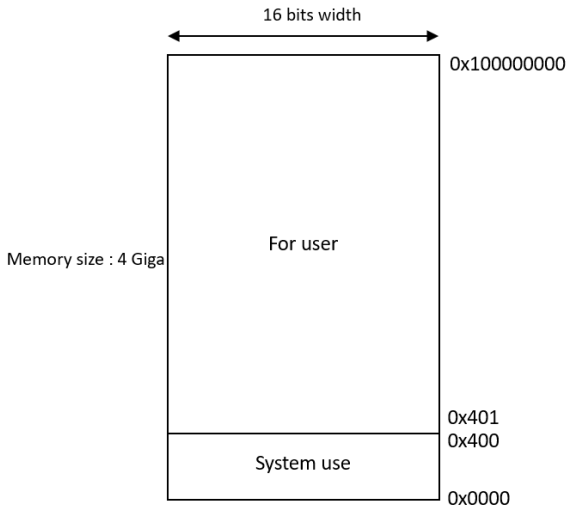


Figure 1 memory representation for Q. 11

13. Given the memory diagram as shown in Figure 1 below, answer the following questions.

i. What is the size of the memory and address buses, respectively?

Address bus size : 33 bits
Data bus size : 16 bits

ii. What is the width of each memory location?

16 bits

iii. What is the total size of memory?

Total memory size = $2^{33} \times 16 = 2^{33} \times 2^4 = 2^{30} \times 2^3 \times 2^4 = 2^7\ Giga = 128\ Gigabits$

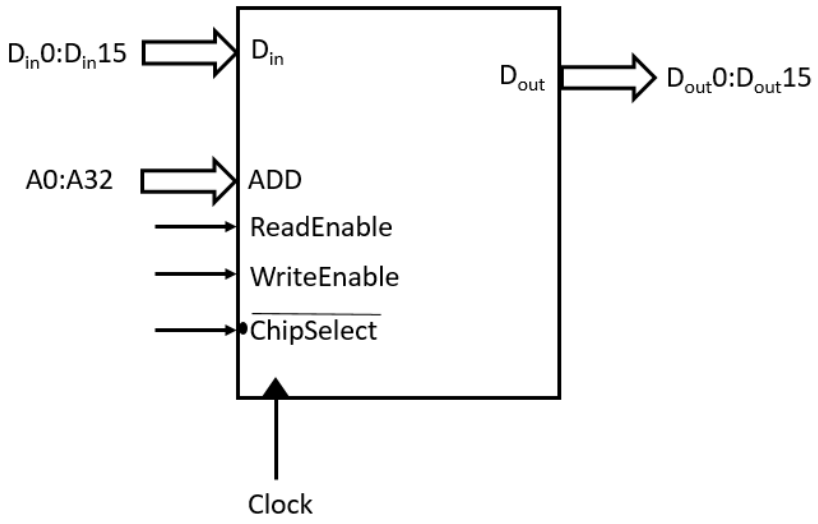
iv. The memory in Figure 1 is positive-edged triggered, ChipSelect signal is Active Low, ReadEnable, and WriteEnable signals are Active HIGH. What should be the state of ReadEnable, WriteEnable, and ChipSelect when we want to perform:

a. Read operation.
ReadEnable = HIGH
WriteEnable = LOW
Chipselect = LOW

b. Write operation.
ReadEnable = LOW
WriteEnable = HIGH
ChipSelect = LOW

c. No operation.
ReadEnable = LOW
WriteEnable = LOW
ChipSelect = HIGH

Hint for Q.12: Active High means that the PIN is activated when its value is HIGH or '1' and deactivated otherwise. Active LOW means that the pin is activated when the value is LOW or '0' and deactivated otherwise.



14. The specifications for memory in Figure 1 are mentioned in Question 12. For the same memory, draw the timing diagram for the following operations.
    i. Memory Write Operation.
    ii. Memory Read Operation.
    iii. No OP (No operation) state.

See the attached PDF file for solution to Q14

(3) (1)

$(A+B+C)\overline{(D+E)} + (A+B+C)(D+E)$

$= (A+B+C)\left[\overline{D+E} + D + E\right]$ (taking $(A+B+C)$ as common term)

using property $\bar{A} + A = 1$, above expression can be simplified as

$= A+B+C\,(1)$

$= A+B+C$

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(4) $f = XZ + Z(X' + XY)$

taking Z as Common term

$f = Z(X + X' + XY)$ (using $A + A' = 1$)

$= Z(1 + XY)$ (using $1 + A = 1$)

$= Z(1)$ (using $A \cdot 1 = A$)

$= Z$

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(5) $\overline{(A+B)}\,\overline{(C+D+E)} + \overline{A+B}$

Take $\overline{A+B}$ as common term

$= \overline{A+B}\,(\overline{C+D+E} + 1)$

$= \overline{A+B}\,(1)$ (using property $A + 1 = 1$)

$= \overline{A+B}$

$= A' \cdot B'$ (De'Morgan's property)

(6)

$\Rightarrow F = A'B' + C' + D' + E'$

$\Rightarrow F = \bar{A}\bar{B} + \bar{C} + \bar{D} + \bar{E}$ ↙ using DeMorgan's law $\begin{cases} \bar{A}.\bar{B} = \overline{A+B} \\ \bar{A}+\bar{B} = \overline{AB} \text{ (same for 3-variable)} \end{cases}$

$\Rightarrow F = \overline{A+B} + \overline{C.D.E}$

$\Rightarrow F = \overline{(A+B).C.D.E}$

Now taking inverse on both side to get $\bar{F}$ or F'.

$\Rightarrow \bar{F} = \overline{\overline{(A+B).CDE}}$ { using property $\overline{\bar{A}} = A$

Double inverse of $A = A$

$\Rightarrow \bar{F} = (A+B)CDE$

or

$\Rightarrow F' = (A+B)CDE$

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(7) $AB + ABC + ABCD + ABCDE + ABCDEF$

we have 6-variables for this expression. But AB is a common factor in all.

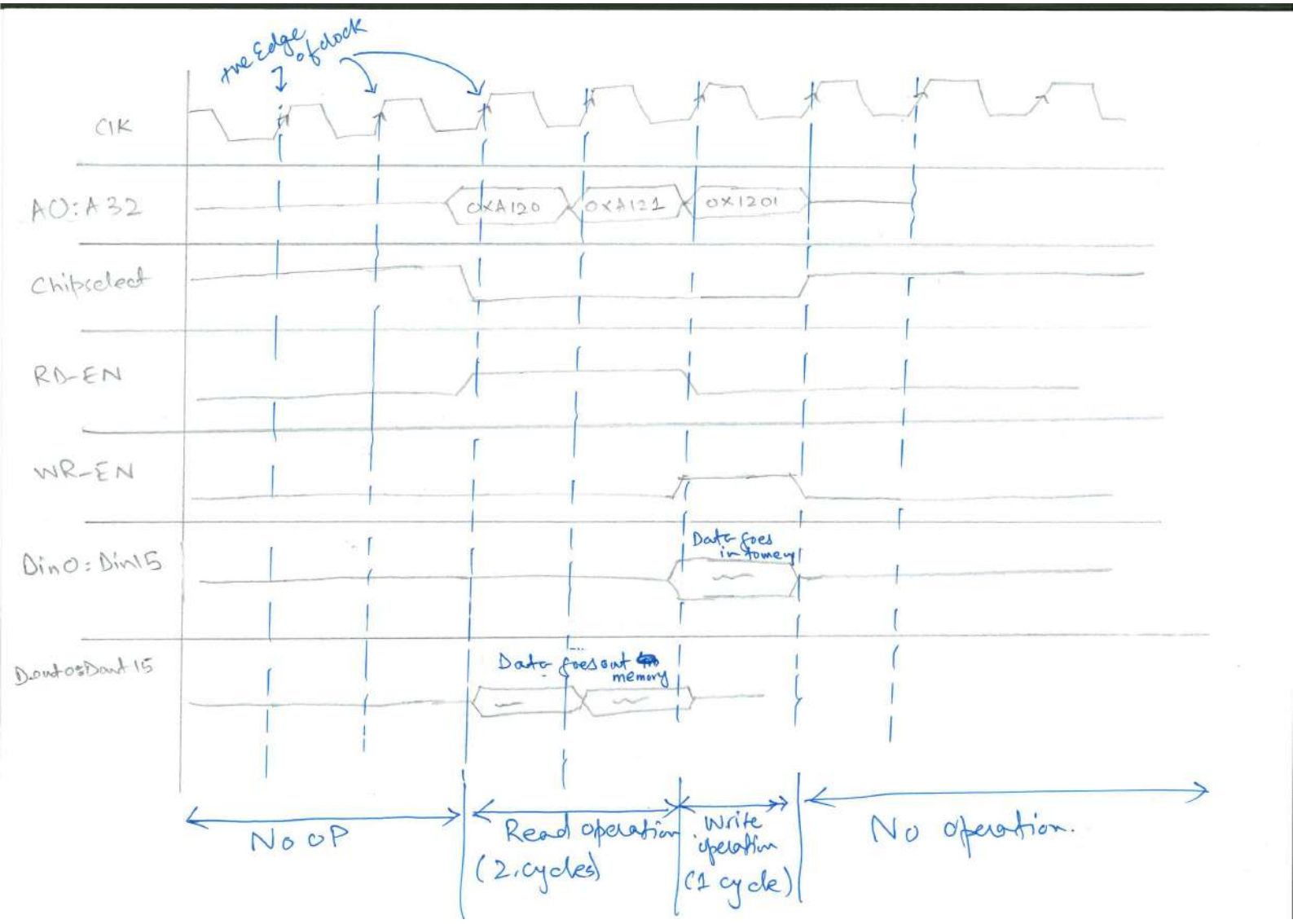
$= AB(1 + C + CD + CDE + CDEF)$

Since in Boolean algebra "1 + Anything = 1", so we get

$= AB(1)$

$= AB$

[Fun fact, the inputs C, D, E, F are called "Don't care" inputs as their states do not affect the actual outcome of the logic circuit]


+ve Edge of clock
CLK
A0:A32
0XA120
0XA121
0X1201
Chipselect
RD-EN
WR-EN
Din0:Din15
Data goes in to memory
Dout0:Dout15
Data goes out of memory
No OP
Read operation
(2 cycles)
Write operation
(1 cycle)
No operation.