Assignment for Week 2

IOT103TC

1. Consider a two-level memory hierarchy consisting of a cache memory M_1 and the main memory M_2. Suppose that the main memory is 8 slower than the cache. 20% of the times, processor misses to get data from the cache. Still, we believe that cache is useful. Can you find how much speedup do we gain by using the cache?
   Hint: lecture 8, part 2, slide 3

2. While learning memory for the first time, a student understands the importance of signal Read_Enable/Write_Enable (RE/~(WE)). However, (s)he learns that there is another signal named Chip_Select (~CS). (S)he thinks that this signal is not required at all. How can you say if (s)he is wrong and ~CS signal is very important?

3. Consider a case when you have a memory of with 4096 locations. Each location can hold 32-bit word. The CPU wants to fetch the data from the memory location 0x2012. What will be the binary value for this location's address? In which CPU register will this address be stored?
   Hint: Convert Hex address to the decimal if confused.

4. What is the access time for a 5-level access cache considering the following H_{Lx} = Hit ratio of level x, t_{Lx} = access time of M_x, t_{MISS} = miss penalty, can also be considered as T_{L3} ?
   Hint: See Lecture 8, part 2, slide 6

5. You are given memory chips of 256 x 8 size. It is required of you to make 4GX8 memory unit. How can you do that?
   Hint: Lecture 7 Part 2

6. Consider a 4-level memory hierarchy in which CPU is connected to L1-Cache, which is connected to L2-Cache. The L2-Cache is connected to the memory, and the memory is connected to the hard drive. If the hit-ratio (or hit-percentage) of level L1 is H1, for L2 it is H2, for Memory it is H3, for hard drive it is H4. Which level would have highest and lowest hit ratio, and why?

7. Continuing Q3, what would the expression of access time of all levels in terms of H1? Furthermore, What would be the total access time in terms of H1?

8. A CPU has a 16 bit memory address register (MAR). What is the maximum size of memory that this CPU can support?

9. A CPU has an address line of 22-bits. What maximum size of memory can this CPU support?

10. A student knows that there are two special purpose registers inside the CPU that can store addresses of memory locations, namely program counter (PC) and Memory Address Register

(MAR). However, the student is confused about how these two registers are different from each other. Do they have same task? If yes, then why do we need two of them? Can you solve his/her problem by explaining in simple words about these two registers and the difference they may have?

11. What is the significance of control signals