Final Assignment for IOT103TC
Computer Architecture Part

1. Give the relationship that represents the dual of the Boolean property A + 1 = 1? (Note: * = AND, + = OR and ' = NOT)
   i. A * 1 =
   ii. A * 0 =
   iii. A + 0 =
   iv. A * A =
   v. A' * 1 =
   vi. A+A' =
   vii. A' + 1 =

2. Given inputs A, B, C, D. How can you represent the De-Morgan's laws for 3-input system and 4-input system?

3. Simplify the Boolean expression (A+B+C)(D+E)' + (A+B+C)(D+E) and choose the best answer.
   i. A + B + C
   ii. D + E
   iii. A'B'C'
   iv. D'E'
   v. None of the above

4. Given the function f(X,Y,Z) = XZ + Z(X'+ XY), the equivalent most simplified Boolean representation for F is: (Also show how you come to the conclusion).
   i. Z + YZ
   ii. Z + XYZ
   iii. XZ
   iv. X + YZ
   v. Z
   vi. None of above

5. Simplification of the Boolean expression (A + B)'(C + D + E)' + (A + B)' yields which of the following results? (Also prove how you come to the conclusion)
   i. A + B
   ii. A'B'
   iii. C + D + E
   iv. C'D'E'
   v. A'B'C'D'E'

6. Given that F = A'B'+ C'+ D'+ E', which of the following represent the only correct expression for F'? (Also prove how you come to the conclusion)
   i. F'= A+B+C+D+E
   ii. F'= ABCDE
   iii. F'= AB(C+D+E)

iv. F'= AB+C'+D'+E'
v. F'= (A+B)CDE

7. Simplification of the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF yields which of the following results? (Also show how you come to the conclusion).
   i. ABCDEF
   ii. AB
   iii. AB + CD + EF
   iv. A + B + C + D + E + F
   v. A + B(C+D(E+F))

8. You are given memory chips of 1 Mega x 16 size.
   a- What will be the width of address and data buses for memory chips of 1 G x 16?
   b- How many total bits of data can 1 G x 16 size chip store?
   c- How to make $8G \times 16$ memory unit from multiple 1G x 16 memory chips? How many 8G x 16 memory chips will be required? MUST Show with the diagram, and also explain in words.
   d- What will be the width of address and data buses for the memory of $8\ G \times\ 16$?

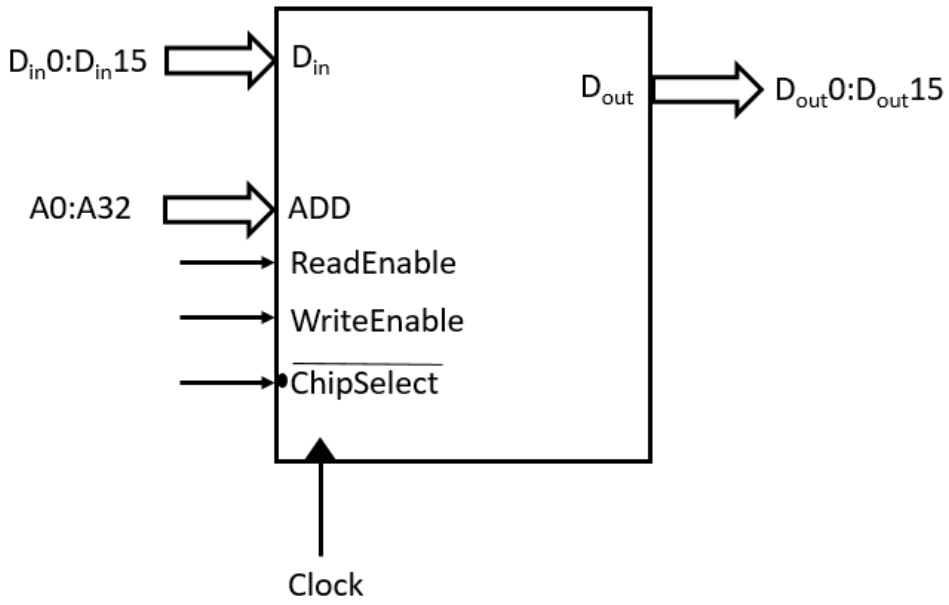
9. If caches are fast memories, why cannot we have ONLY large sized cache instead of SDRAM or hard drive as memory storage?

10. Von-Neumann machines have a popular and robust architecture. However, what benefit you can think of while considering Harvard architecture? What are negatives of having Harvard architecture instead of Von-Neumann?

11. A 16-bit wide memory has its addresses starting from 0x0000 and ending at 0x100000000.
    i. What is to the total size of memory?
    ii. What is the total size of memory in terms of Bytes?
    iii. If addresses from 0x0000 to 0x0400 are reserved for system use, how much memory is available for the user?
    iv. How much memory size in terms of Bytes (e.g. Mega Bytes) is reserved for system?
    v. What is the size of address buss for the memory?
    vi. What is the size of data bus for the memory?

12. Given the memory diagram as shown in Figure 1 below, answer the following questions.
    i. What is the size of the memory and address buses, respectively?
    ii. What is the width of each memory location?
    iii. What is the total size of memory?
    iv. The memory in Figure 1 is positive-edged triggered, ChipSelect signal is Active Low, ReadEnable, and WriteEnable signals are Active HIGH. What should be the state of ReadEnable, WriteEnable, and ChipSelect when we want to perform:
        a. Read operation.
        b. Write operation.
        c. No operation.

Hint for Q.12: Active High means that the PIN is activated when its value is HIGH or '1' and deactivated otherwise. Active LOW means that the pin is activated when the value is LOW or '0' and deactivated otherwise.



13. The specifications for memory in Figure 1 are mentioned in Question 12. For the same memory, draw the timing diagram for the following operations.
    i. Memory Write Operation.
    ii. Memory Read Operation.
    iii. No OP (No operation) state.