Week 5: Assignment Solutions

1. How many address and data lines will be there for a 16M x 32 memory system?
    a. 24 and 5
    b. 20 and 32
    c. 24 and 32
    d. None of the above

    Correct solution is (c).
    Since there are 16M words, the number of address lines will be 24, since 2^{24} = 16M. Also since the word size is 32 bits, the number of data lines will also be 32.

2. What is the function of the chip select line (CS') in a memory chip?
    a. Power supply is applied to the chip when CS' is activated.
    b. The data bus is put in the high impedance state when CS' is deactivated.
    c. It prevents two or more subsystems from using the memory simultaneously.
    d. None of the above.

    Correct answer is (b).
    When a memory system consists of a number of memory chips, typically the data lines of the memory chips are connected together. For example, all the D0 data lines will be connected, all the D1 data lines will be connected, and so on. When a number of data output lines are tied together, exactly one output must be active at a time and all the others must be in the high impedance state. The chip select signal forces all the data outputs of a chip to go into the high impedance state if it is deactivated.

3. Which of the following statements are false?
    a. The main memory of a computer system must be non-volatile.
    b. The main memory of a computer system provides random access.
    c. The data memory can be built using either ROM or RAM.
    d. None of the above.

    Correct answers are (a) and (c).
    (a) is false because main memory is typically built using semiconductor RAM that is volatile.
    (b) is true as RAM provides random access; access time does not depend on the location being accessed.
    (c) is false as data memory should support both read and write and hence it cannot be built using ROM.

4. Which of the following statements are true?
    a. The main objective for using cache memory is to increase the effective speed of the memory system.
    b. The main objective for using virtual memory is to increase the effective capacity of the memory system.
    c. The size of main memory is larger as compared to cache memory.

d. Main memory is faster as compared to cache memory.

Correct answers are (a), (b) and (c).

(a) is true since the average memory access of a memory system using cache is close to the access time of the cache. And cache is faster than main memory.

(b) is true since in virtual memory the size of a program can be as large as the size of the secondary memory.

(c) is true since cache memory is more expensive and hence its capacity is smaller than main memory.

(d) is clearly false.

5. For a 2K x 16 memory system that uses a decoder to select a word, the total number of external connections to the memory system (including address, data, control, and power signals) will be at least ……..

   Correct answer is 31.

   There will be 11 lines for the address (2^{11}=2K), 16 lines for the data, 2 lines for the power supply, and 2 RD and WR lines. The total is 31.

6. Which of the following are true for Static RAM (SRAM)?
   a. Power consumption is higher than Dynamic RAM (DRAM).
   b. Packing density is higher than Dynamic RAM (DRAM).
   c. It is faster than Dynamic RAM (DRAM).
   d. It is non-volatile.

   Correct answers are (a) and (c).

   This follows from the properties and characteristics of SRAM and DRAM. In SRAM, storage cells are built using cross-coupled inverters that are faster and also draw more power. Since the number of transistors per cell in SRAM is higher than DRAM, its packing density is less. Also, both SRAM and DRAM are volatile.

7. Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be:
   a. 20 and 10
   b. 30 and 1
   c. 2^{20} and 2^{10}
   d. None of the above

   Correct answer is (a).

   Since there are 1M rows, the number of row address lines will be 20, as 2^{20} = 1M. Also, for selecting one of the 1K columns, the number of column address lines will be 10, as 2^{10} = 1K.

8. Which of the following statements are true?
   a. SDR RAM can transfer one word of data in a single clock cycle.
   b. DDR RAM can transfer two words of data in a single clock cycle.
   c. For DDR2 RAM, the internal clock is 133 MHz and bus clock is 266 MHz.
   d. None of the above.

   All of (a), (b) and (c) are true.

9. To build a 1G x 16 memory system, the number of 256M x 8 memory modules required will be ……
   Correct answer is 8.
   4 x 256 M = 1G, and 2 x 8 = 16.
   Hence the number of memory modules required will be 4x2 = 8.

10. Which of the following are true for memory interleaving?
    a. The lower order address lines are connected to the address lines of the memory chips.
    b. Consecutive memory addresses are mapped to consecutive memory modules.
    c. Permits faster data transfer for word-aligned data.
    d. None of the above.

    Correct answers are (b) and (c).
    In memory interleaving, the high-order address lines are connected to the address lines of the memory chips, and the low order bits select the memory modules. Thus consecutive memory addresses get mapped to consecutive modules, which permits faster multi-byte data transfers.

11. Consider a memory system that takes 25 nsec to service the access of a single 64-bit word. The bandwidth of the processor-memory interface will be …….. Mbytes per second.
    Correct answer is 320.
    8 bytes of data can be accessed in 25 nsec.
    So in 1 second, number of bytes accessed = 8 / 25 x 10^9 bytes = 320 Mbytes.

12. A RAM chip has a capacity of 1024 words of 8 bits each. The number of 2-to-4 decoders with enable lines needed to construct a 16K x 16 RAM system will be ……..
    Correct answer is 5.
    To construct a memory system with 16K words using 1024x8 RAM chips, we have to connect 16 such chips in parallel. The decoder will have to select one of the 16 chips. To construct a 4x16 decoder, we require 5 2x4 decoders.