A SHORT SURVEY OF FREQUENCY SYNTHESIZER TECHNIQUES

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Introduction

Frequency synthesizers are the work horses of precise time and frequency. It is the job of frequency synthesizers to translate the performance of a reference oscillator to frequencies useful to the user. Frequency translators fall into two general classes: (fixed) reference generators and (adjustable) frequency synthesizers. In this paper, we will discuss the architectures and design techniques used in the construction of the second class, (adjustable) frequency synthesizers (though many of the techniques discussed are also used in the construction of reference generators). This paper is not meant to be an exhaustive treatment of frequency synthesizers, but only a brief and qualitative description of the basic frequency synthesizer architectures and techniques. Readers are referred to the bibliography at the end of the paper for more in depth material and for a quantitative analysis of the various architectures.

Frequency Synthesizer Design and Performance Parameters

Tables 1 and 2 summarize the important parameters which characterize the design and performance of frequency synthesizers. The tables are somewhat arbitrarily broken up into basic synthesizer parameters (Table 1) and other important parameters (Table 1). The basic synthesizer parameters in Table 1 are the obvious performance parameters that come to mind when defining the performance of a frequency synthesizer and need no further explanation.

TABLE 1. BASIC SYNTHESIZER PARAMETERS

Frequency range (maximum and minimum frequency)
Frequency resolution
Settling time
Phase/frequency stability (time domain)
Spectral purity (noise, harmonics, spurious sidebands)

TABLE 2. OTHER IMPORTANT SYNTHESIZER PARAMETERS

Of Output type (sine, square, pulse, other)
Output level
Amplitude performance (flatness, stability, accuracy)
Phase continuity (when frequency is changed)
Phase synchronization (to external epoch)
Operating environment (temperature, humidity, shock)
Environmental stability/performance
Size, weight, power consumption, cost, complexity
Required references (number and type)
Number of independent output frequencies
Manual or remote control (command format)

The other important parameters listed in Table 2 are often equally as important as the basic parameters. Of course the type of output and the output levels required are important design parameters which often affect the complexity and type of design required. The amplitude performance of a frequency synthesizer, its flatness over the frequency range, its stability, and its accuracy are often as important as the basic phase and frequency performance parameters. The phase continuity, whether the signal must be continuous when the frequency is changed, and the phase synchronization requirements, whether the output must be synchronized to some reference epoch, are also of importance. The operating environment of the synthesizer is another important parameter. It is important in determining stresses the synthesizer must endure. The operating environment also affects the other parameters (environmental stability/performance).

Size, weight, power consumption, cost, and complexity constraints determine the type of designs that can be utilized. The number of required references strongly influences the overall complexity and size of the synthesizer because these references usually have to be generated with internal reference generators. The required number of independent output frequencies has great influence on the size penalty imposed by a complex set of reference generators; since one reference generator can drive many synthesizers, the size penalty imposed by complex reference generators becomes negligible as the number of required output frequencies grows. Last but not least, another important factor which affects circuit complexity is whether the output has to be controlled remotely or manually. For the remote case, the required command format also affects the complexity of the onboard command logic.

The above parameters together define the physical and performance constraints important in the design of frequency synthesizers. In the architectural description sections that follow, we will attempt to outline and compare the strengths and weakness of each architecture in terms of the above parameters along with the architectural descriptions. Ideally, one would like to quantitatively categorize the strengths and weaknesses of each architecture with a set of typical performance parameter values. We apologize for not presenting such charts in this paper, but we have not done so for two very good reasons. First, the state of the art of frequency synthesizers is so dynamic and the field is so diverse that such charts, even if they could be researched properly, would most likely be obsolete almost immediately. Second, and most important, the strengths and weakness of the various architectures are more properly defined in terms of tradeoffs between various competing parameters. One can, therefore, almost always increase the performance level of a particular parameter by sacrificing another, making a chart with fixed values impossible to create.

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Frequency Synthesizer Techniques

In the architectural description sections that follow, we have separated the various frequency synthesizer techniques into three general classes: direct analog synthesis, indirect synthesis, and direct digital synthesis. In direct analog synthesis, the frequency of the reference oscillator or oscillators are translated directly, using analog techniques, without the use of an internal voltage controlled oscillator (VCO). In indirect synthesis, a VCO, which is phase or frequency locked to the reference oscillators, is the source of the synthesizer output frequency. In direct digital synthesis (DDS), the output waveform is directly synthesized digitally from the reference oscillator which is used as a clock for the digital operation. Because some DDS techniques are used with indirect synthesis, we will postpone our discussion of DDS techniques until after we have discussed indirect synthesis.

Direct Analog Synthesis

In direct analog synthesis, the frequency of the reference oscillator or oscillators are translated directly, using analog techniques. The basic direct analog synthesis techniques consist of frequency division, mixing, multiplication, switching, and filtering. The use of the word analog here is somewhat of a misnomer since frequency switching and division can be accomplished digitally. We use the word analog here to distinguish these techniques from direct digital synthesis. The distinction between direct analog and direct digital synthesis will become apparent after the section on direct digital synthesis.

Frequency Division

Frequency division is described by the basic operation:

$$f_o = f_a/N$$

where f_o is the output frequency, f_a is the input frequency and N is the division ratio.

Frequency division is accomplished by using a digital counter, a regenerative divider, or an injection locked oscillator. Before the advent of large scale integration (LSI), regenerative dividers and injection locked oscillators were popular because, for large division ratios, they are much less complex than digital dividers. Regenerative dividers and injection locked oscillators, however, are relatively narrowband devices and are susceptible to cycle skipping. With the advent of LSI, complex digital counters could be implemented monolithically in very small and low power packages. Digital dividers or counters are wideband devices, operating from dc to a maximum frequency determined by the type of digital logic used. (The current state of the art is about 10 GHz.) They have the disadvantage of outputting only a pulse or square wave, which has high harmonic content.

There are three types of digital counters used as frequency dividers: asynchronous or ripple counters, synchronous counters, and dual modulus counters. Ripple counters are relatively simple low power counters which are generally used as fixed frequency dividers. However, because the signal ripples through each of the stages sequentially, these counters can have relatively high levels of phase instabilities. In certain applications, these instabilities can be cleaned up by using a flip flop clocked by both the counter output and the input frequency. Presettable synchronous counters are used as variable frequency dividers. These counters tend to have lower levels of phase instabilities, but higher levels of power consumption than ripple counters. A third type of counter used in variable division applications is called a dual modulus or swallow counter. This counter uses a high speed divide by N/N+1 counter which is controlled by lower speed presettable synchronous counters. It is used to produce very large variable division ratios with relatively low power consumption. (Lower than an equivalent high speed synchronous counter.) The dual modulus counter has the disadvantage of having a minimum division ratio as well as a maximum one, but this is not a problem in many applications.

All dividers, when used as frequency synthesizers, have the disadvantage of requiring a large N to achieve a fine frequency resolution. This means the reference frequency must be very large compared with the output frequency to achieve a high resolution.

Frequency Mixing

Frequency mixing is described by the basic operation:

$$f_o = f_a \pm f_b$$

where f_o is the output frequency and f_a and f_b are two input frequencies.

Frequency mixing is accomplished by using a non-linear element such as a diode or a transistor. The basic disadvantage of mixing is the presence of other mixing components of the form:

$$n f_a \pm m f_b$$

where n and m are integers. These generate spurious sidebands (spurs) in the desired signal. Frequency filtering can be used to eliminate these spurs, but at the price of narrowing the frequency range. A wideband solution to reducing unwanted spurs is to use single balanced, double balanced, triple balanced, and single sideband mixers. These mixers can reduce spurs to the -20 to -50 dBc level before filtering.

Frequency Multiplication

Frequency multiplication is described by the basic operation:

$$f_o = n f_a$$

where f_o is the output frequency, f_a is the input frequency, and n is an integer.

Direct analog frequency multiplication is accomplished using a non-linear element such as a diode, transistor, or varactor. The basic problem with frequency multiplication is the presence of spurs from the multiplication orders other than the desired one. These spurs can be on the order of or greater than the desired signal, and filtering is normally required to reduce them to acceptable levels. Balanced multipliers, such as full wave rectifiers, can be used to reduce the level of certain spurs before filtering. (For example, full wave rectifiers tend to suppress odd harmonic orders.)

Since a non-linear element produces both frequency mixing and multiplication, the two operations are sometimes combined in a single stage. This has the advantage of reducing circuit complexity, but usually produces higher spurs than the separated operations.

Frequency Switching

Frequency switching is the selection of one of sev-

eral input frequencies using switches. This operation is extremely straightforward, but requires as many references as output frequencies. The two basic parameters of importance in frequency switching are switch settling time and switch isolation in the open position. Switch settling time, of course, limits the synthesizer settling time. Switch isolation determines the level of spurs generated by the non-selected frequency sources leaking into the output. Three basic types of switches are used: mechanical, electromechanical, and electronic. Mechanical and electromechanical switches provide the highest degree of isolation, but are slow and bulky. Electronic switches can provide fast settling times and small size. However, in electronic switches, there tends to be a trade-off between size and power consumption and isolation. Monolithic FET switch arrays are extremely small and have very low power consumption, but have relatively low isolation. PIN and conventional diode switches have much higher levels of isolation, but are bulkier and have relatively high power consumption. Within the category of diode switches, there also tends to be a direct trade-off of isolation versus size and power consumption.

Frequency Filtering

Frequency filters are used to reduce the spurs and harmonics generated by the other techniques. Far away spurs and harmonics can be easily filtered using wide band filters without introducing many problems. Filtering nearby spurs, however, requires the use of narrow band filters. This can introduce the following problems:

1. The output frequency range is restricted to the pass band of the filter.

2. The settling time is inversely proportional to the pass band of the filter.

3. The phase stability, amplitude flatness, etc., can be affected by narrow pass bands.

4. Narrowband filters have large group delays which can cause instability in feedback paths.

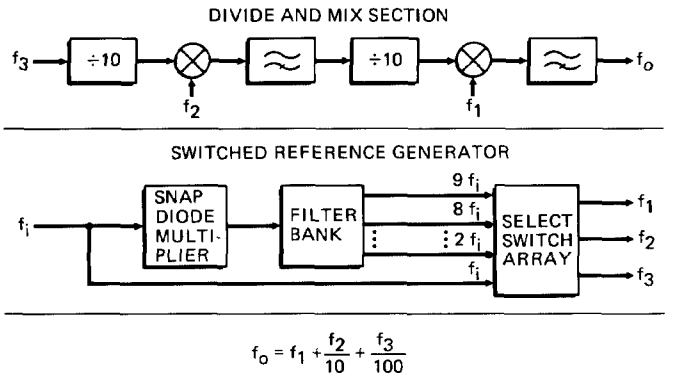
There are two classes of filters used in frequency standards, passive and active. Passive filters used in synthesizers range from simple RC filters to complex SAW, crystal, and cavity filters. Filters require no power, but their size and weight tend to go up with the Q or required attenuation vaues. SAW filters have revolutionized the filter industry because of their small size to performance ratio compared with other types of filters.

Active filters of course require power. For lower frequencies, operational amplifier active filters are very useful in producing exotic filter responses. For higher frequencies, phase and frequency locked loops are used as active filters. These filters are covered in detail in the section on indirect synthesis. Active filters can also generate noise and spurs and can have oscillation problems due to the noise figure, distortion, and gain of the active elements.

Hybrid Direct Output Designs

The direct analog techniques listed above are very powerful when combined together in groups. Figure 1 shows a typical direct analog synthesizer which uses all the above techniques. This type of synthesizer is sometimes called a switch, divide, and mix synthesizer.

The main part of the synthesizer is the divide and mix section. This section consists of a sequence of



$$f_o = f_1 + \frac{f_2}{10} + \frac{f_3}{100}$$

FIGURE 1. TYPICAL DIRECT ANALOG SYNTHESIZER

stages each containing a divider, a mixer, and a high pass filter. In each stage, an input frequency, such as f_3, is divided by a number such as 10 in the divider, mixed with a second frequency, such as f_2, in the mixer, and filtered to produce $f_3 + f_2/10$. This output frequency is input to the next divide, mix, and filter stage and so on as many times as desired to produce an output of the form:

$$f_o = f_1 + f_2/10 + f_3/100 + ...$$

The second part of the synthesizer, the selectable reference generator section, is used to generate f_1, f_2, f_3, etc. This section consists of a snap diode multiplier, a SAW filter bank, and a select switch array. The snap diode multiplier and the SAW filter bank are used to generate a bank of 9 reference frequencies: f_a, 2 f_a,..., 9 f_a. This bank of reference frequencies is sent to the select switch array which routes any one of the 9 reference frequencies to the outputs f_1, f_2, f_3, etc. Thus:

$$f_i = N_i\ f_a$$

where N_i is an integer. Using this, the output frequency becomes:

$$f_o = (N_1 + N_2/10 + N_3/100 + ...)\ f_a$$

Thus each reference frequency is used to select a digit in a decadic representation of the output frequency. In a practical design, additional switches are used to select zero possibilities for the digits, N_i, in the above formula.

Indirect Synthesis

Indirect synthesis utilizes an oscillator controlled by a phase lock loop (PLL) or a frequency lock loop (FLL) to generate its output frequency. The basic PLL/FLL is shown in Figure 2. It consists of the following:

1. A voltage controlled oscillator (VCO) which outputs a frequency f_o

2. One or more reference frequency inputs, f_a, f_b, etc.

3. A frequency translator defined by the function $T(f_o)$

4. A phase discriminator (PD) or frequency discriminator (FD) which generates an output determined by the difference in phase or frequency between f_a and $T(f_o)$

5. A loop filter which conditions the output of

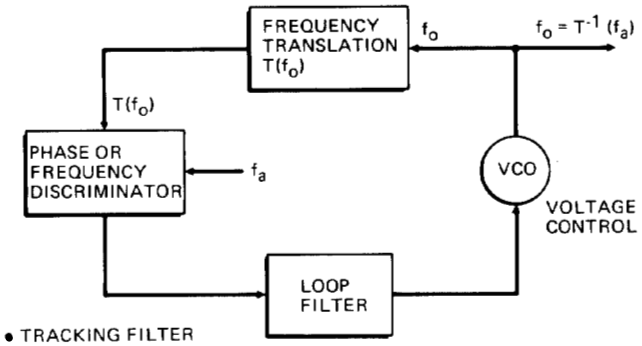


FIGURE 2. BASIC INDIRECT SYNTHESIZER

the phase or frequency discriminator before sending it to the voltage control input of the VCO

The FLL/PLL is a servo loop. When the loop locks, $T(f_o)$ becomes equal to f_a and the VCO output frequency is driven to:

$$f_o = T^{-1}(f_o)$$

where T^{-1} indicates the inverse function, not 1/T.

The PLL/FLL has two very important properties for frequency synthesis, as an operation inverter and a tracking filter.

PLL/FLL as an Operation Inverter

The FLL/PLL inverts the frequency translation operation $T(f_a)$. That is, its output is $T^{-1}(f_a)$. Figure 3 shows a typical frequency translation loop synthesizer. Here f_b is subtracted from f_o and the result is divided by N before it is sent to FD or PD. Since the loop inverts this process, the resultant output is:

$$f_o = f_b + Nf_o$$

PLL/FLL as a Tracking Filter

The VCO's output tracks $T^{-1}(f_o)$ within a loop bandwidth B around the lock frequency. Outside this bandwidth, the VCO's performance is determined by the free running properties of the VCO. Thus the loop filters out any spurs, harmonics, and noise generated by the reference or the translation process $T(f_o)$ outside the loop bandwidth. This process creates a filter centered around the output frequency regardless of the value f_a or the translation function, T(f), and thus effectively tracks with the output when fa or T(f) change. (Because T(f) is inside the loop, care must be used when tracking changes in T(f) since changing T(f) also affects the loop response function as well as the center frequency.)

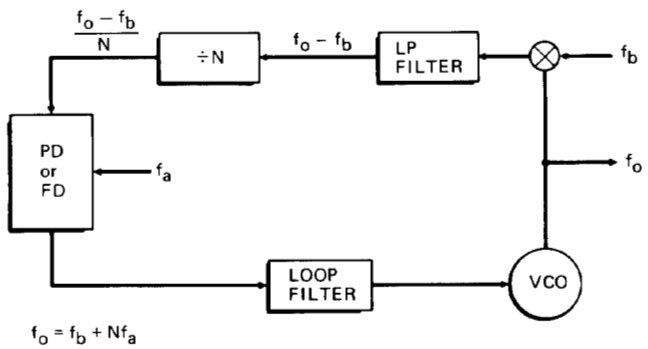


FIGURE 3. FREQUENCY TRANSLATION LOOP

Effects of Loop Bandwidth on Synthesizer Performance

Setting the loop bandwidth frequency to the Fourier frequency (offset from the carrier) where the sum of the unfiltered phase noise spectral density from the reference and the loop electronics equals the free running VCO phase noise spectral density minimizes the total (integrated) phase noise. Also the loop bandwidth must be substantially lower than the reference frequency into the phase or frequency discriminator to keep harmonics of this reference frequency from generating spurious sidebands in the output frequency.

However, the settling time of a loop is inversely proportional to the loop bandwidth. Thus a settling time requirement sets a minimum loop bandwidth which can be used. This minimum loop bandwidth may be larger than the loop bandwidth required to minimize the phase noise, so the settling time requirement may force an increase in phase noise. This minimum loop bandwidth also constrains the lowest reference frequency which can be used at the phase or frequency discriminator without generating output spurs since this reference frequency must be substantially higher than the loop bandwidth. To minimize the constraints imposed by the settling time requirement, much effort has gone into reducing the loop settling time-to-bandwidth ratio. We will discuss this in more detail in a later section.

Phase vs Frequency Lock Loops

PLL's are much more popular in synthesizer applications today than FLL's for several reasons:

1. Good wideband PD's are relatively easy to make using digital techniques and balanced mixers, while FD's tends to be narrowband devices.

2. Loop instabilities and noise in an FLL are converted to frequency instabilities and noise, while the loop instabilities and noise in a PLL are only converted to phase instabilities and noise.

3. Tighter lock is maintained on the VCO by PLL's because a PLL locks the phase of the VCO to the phase of the reference input, while an FLL only locks the frequency of the VCO to the frequency of the reference input.

Since PLL's are by far the most popular of the two loops in frequency synthesizers, for the remainder of this section, we will limit our discussion to PLL's. Bear in mind, however, that many of the comments we will be making about PLL's also apply to FLL's.

Analog and Digital PLL's

PLL's in use today fall into two general groups: analog and digital loops. An analog PLL is shown in Figure 4 and a digital PLL is shown in Figure 5. In the analog PLL shown in Figure 4, the phase detector or phase discriminator outputs an analog voltage which depends on the phase difference between the reference and the feedback VCO signal. This analog voltage is processed in an analog loop filter and then used to control the VCO.

In the digital PLL shown in Figure 5, a phase error quantizer, outputs a digital word which depends on the difference in phase between the reference and the feedback VCO signal. This quantized phase error word is sent to a hardware or software digital loop filter which processes the error word and outputs a VCO control word to a digital-to-analog converter (DAC).

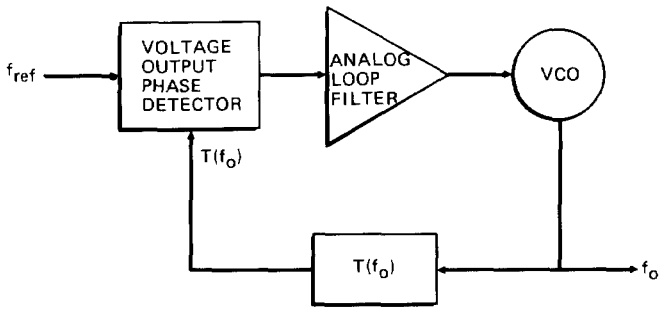


FIGURE 4. ANALOG PHASE LOCK LOOP

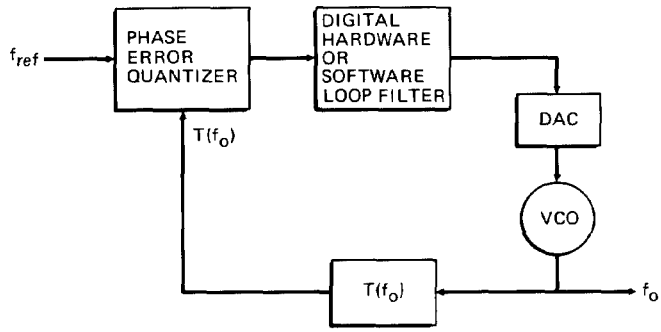


FIGURE 5. DIGITAL PHASE LOCK LOOP

The DAC then turns the control word into a control voltage for the VCO.

We will compare the pros and cons of analog versus digital loops in a later section, but before we do, it is important to explain about the techniques used to improve the settling time of PLL's.

Fast Loop Settling Techniques

As mentioned previously, because it is important to minimize the constraints imposed by settling time on loop bandwidth, much design effort has gone into developing techniques which reduce the settling time of a loop for a given loop bandwidth. Figure 6 outlines some of these techniques as used in an analog loop. A short discussion of each of the techniques, as applied in an analog PLL follows. Each technique has an equivalent form in a digital PLL.

Pretune DAC. The settling time of a loop is directly related to initial frequency offset of the VCO when the frequency of the loop is changed. Since the VCO frequency output versus control voltage input curve is known to some level, the initial frequency offset

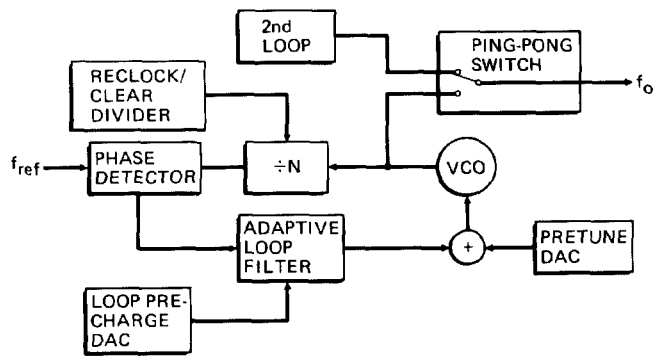


FIGURE 6. FAST LOOP SETTLING TECHNIQUES

can be reduced drastically by using a digital to analog converter (DAC) to pretune the VCO to approximately the right frequency when the loop frequency is changed.

Loop Precharge DAC. A related technique is the loop precharge DAC. In a second order loop, the voltage output of the loop filter, which generates the control voltage for the VCO, is determined by the charge on a capacitor in the loop filter. In order to reduce the initial frequency offset of the VCO when the loop frequency is changed, one can use a DAC to precharge this loop capacitor. The advantage of using the precharge DAC over the pretune DAC is that the precharge DAC is disconnected from the system once it has charged the loop capacitor. This means that the DAC voltage noise does not increase the synthesizer steady state phase noise in the case of the precharge DAC. The principal disadvantage of the precharge DAC is that it is much more complicated to implement than a pretune DAC.

Reclock/Clear Divider. Reclocking and clearing the divider is a technique which improves settling time by reducing the initial phase error in the loop when the loop frequency is changed. When the loop is locked in the steady state condition, the divide by N counter clears and outputs a pulse to the phase detector at the same instant that the reference frequency supplies a pulse to the phase detector. This is another way of stating that there is zero phase error between the reference frequency and the divided down VCO frequency. Thus the size of the divider count at the reference clock epoch is a measure of the phase error in the loop at that instant. In the initial stages of changing the frequency of the loop, the divide by N counter usually accumulates a large random count due to the fact that the VCO frequency is varying widely. This random count represents an initial phase error which the loop must track out before it settles. Also since N is usually quite large, this initial phase error can be equivalent to many cycles of phase error at the VCO frequency, which can take a long time to track out. One way of minimizing this initial phase error is to reclock and clear the divider with the reference frequency some time after the initial stages of loop settling. This greatly reduces the initial phase error of the loop, and thus reduces the loop settling time significantly.

Adaptive Loop. A wideband loop settles faster than a narrowband loop. If one were to use a wideband loop in the early stages of loop settling and somehow switch to a narrowband loop as the loop settles, one could speed up the settling process. This is called an adaptive loop. One way the switchover from wideband to narrowband filtering is accomplished is by putting diodes in the loop filter which change their impedance with loop error.

Ping-Pong Loop. One can completely side step the settling time problem by putting two loops in a synthesizer and switching between them. This is called a ping-pong loop. In a typical ping-pong sequence, the ping-pong switch changes over to a new loop after it has had time to settle. The old loop then is immediately changed to a new frequency and the ping-pong switch is again switched after the loop settles. In a ping-pong loop, the loop settling time now limits the switching period rather than the settling time itself.

Pros and Cons of Digital and Analog Loops

Now let us proceed with a discussion of the pros and cons of analog versus digital loops. One disadvantage of analog loops is the fact that $T(f_o)$ must be equal to the reference frequency for the loop to lock. This is because a dc voltage must be output out of the

phase detector for an analog loop to be in a steady state locked condition. Conversely, in a digital loop, a changing phase error word out of the phase quantizer can be corrected for by subtracting a changing word in the digital loop filter. This means a digital loop can lock with $T(f_o)$ not equal to the reference frequency. Because of this, a digital loop can:

1. Track multiple independent reference frequencies in a single loop just by adding extra phase error quantizers

2. Perform part of the frequency translation in the digital processor of the loop filter

Another disadvantage of analog loops is that they are susceptible to burst error. Burst error is a large noise spike or other effect which causes the loop capacitor to discharge. The problem with this is two fold. First, this causes the VCO frequency to go to its maximum or minimum frequency. Second, it now takes the full settling time of the loop to recover to its original state. In a digital loop, this susceptibility to burst error can be made virtually nil by using limit algorithms which limit the rate of change of the equivalent loop capacitor and by using special memory to store the equivalent of the capacitor charge state.

A third disadvantage of analog loops is that fast loop settling techniques are very hardware intensive. In digital loops, many of these techniques can be implemented very easily with software algorithms or digital hardware.

One big advantage of digital loops is that processing time limits the maximum loop bandwidth. This problem is more severe in software loops, which have lower operating speeds than hardware loops.

A final disadvantage of digital loops occurs because the control DAC quantizes the voltage used to control the VCO frequency. This means there is a minimum frequency step size that the loop can implement. When this minimum step size is larger than the RMS frequency jitter of the loop, the digital loop can undergo limit cycle oscillations which generate large spurious sidebands. This limit cycle problem, however, can be eliminated by dithering the loop with a high frequency error signal, causing the DAC to jump between two adjacent states at the high frequency. This high frequency jitter can then be filtered out before the DAC voltage goes to the VCO by adding an analog low pass filter in between the DAC and the VCO, so the digital loop behaves like a switching regulator.

Direct Digital Synthesis

Direct digital synthesizer (DDS) designs in the technical literature fall into six major categories: pulse output DDS's, fractional divider or pulse snatching DDS's, sine output DDS's, triangle output DDS's, phase interpolation DDS's, and jitter injection DDS's. A brief discussion of each category follows.

Pulse Output DDS

The pulse output DDS (Kodanev, 1981; Peters, 1982) is the simplest of the five DDS categories. As shown in Figure 7, it merely consists of an N bit accumulator set up to add a frequency word, K, in an accumulator once every clock period, T_c. That is, if the current accumulator register value is R, once every T_c, the accumulator performs the operation:

$$R + K \rightarrow R$$

in modulo 2^N arithmetic. Note that for this addition

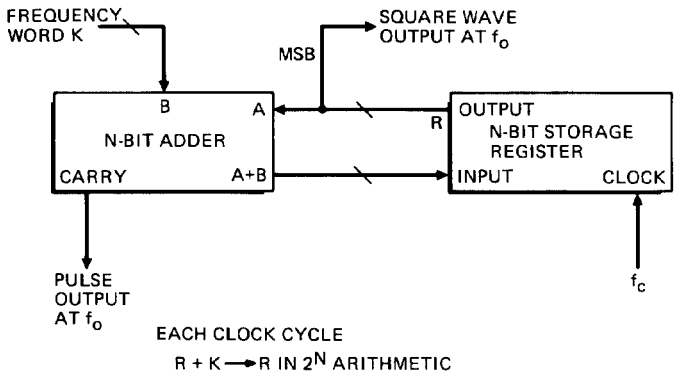


FIGURE 7. PULSE OUTPUT DIRECT DIGITAL SYNTHESIZER

process, the accumulator will overflow, on average, once every $2^N/K$ clock periods, so the average frequency of overflows will be:

$$f_o = F\, f_c$$

where f_c, the clock frequency, is $1/T_c$, and where the fractional output frequency, F, is given by:

$$F = K/2^N$$

The frequency output of this synthesizer is merely the carry output of the accumulator for a pulse output or the most significant bit (MSB) of the accumulator for an approximate square wave output. A typical example of the output of a pulse output DDS is shown in Figure 8.

The basic problem with this architecture is that it has very high levels of spurs and phase jitter.

Fractional Divider or Pulse Swallowing DDS

The fractional divider (Hassun, 1984; Nazarenko, 1982; Nissonevitch, 1978; No Author, 1982; Schineller, 1982; Rohde, 1981; Rohde. 1983) or pulse swallower

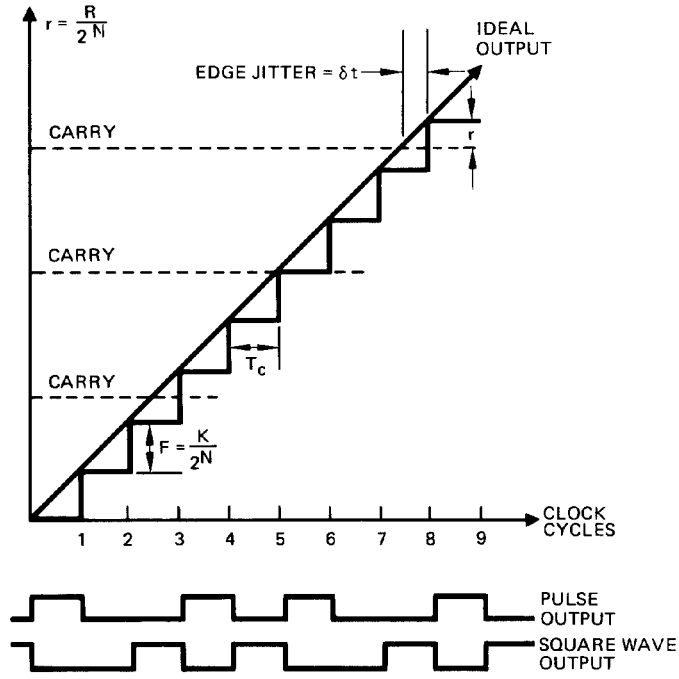


FIGURE 8. TYPICAL PULSE OUTPUT DIRECT DIGITAL SYNTHESIS WAVEFORM

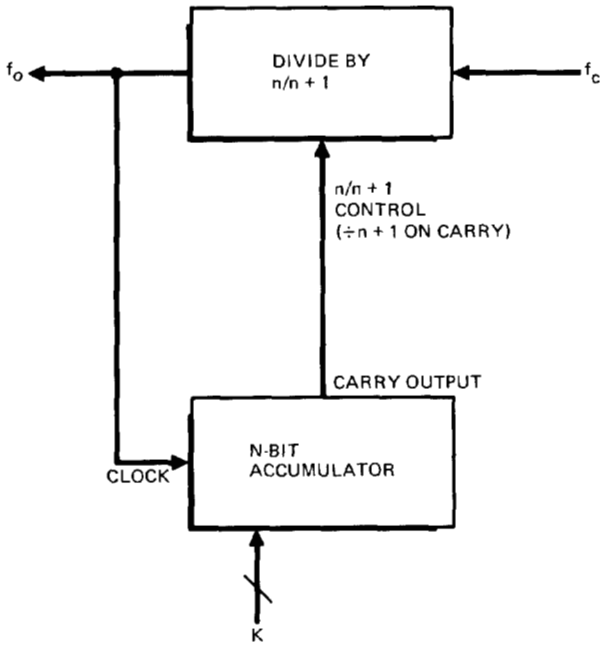


FIGURE 9. FRACTIONAL DIVIDER OR PULSE SWALLOWING DIRECT DIGITAL SYNTHESIZER

(Kohler, 1983) is a variation on the pulse output DDS. A block diagram of the fractional divider DDS is shown in Figure 9. In this type of DDS, the accumulator carry output is used to drive the n/n+1 control line of a divide-by-n/n+1 counter so that n+1 division occurs on a carry. The accumulator, in this case, is clocked by the output of the divider, f_o. The divider is clocked by the f_c input, and the output of the DDS is f_o. One can show that on average, the output frequency is:

$$f_o = f_c/(n+F)$$

(Notice that, in this case, F determines the fractional part of the division.) A typical example of the output of a fractional divider DDS is shown in Figure 10.

This type of DDS also has high levels of spurs and phase jitter.

Sine Output DDS

The sine output DDS produces a smoother, more sine-like signal by adding a sine look-up table and a digital to analog converter (DAC) to the pulse type DDS (Tierney, 1971; Gorski-Popiel, 1975; Rabiner, 1975; Galbraith, 1982; Hoppes, 1982; Kaiser, 1985; Crowley, 1982; Rohde, 1983). A block diagram of the sine output DDS is shown in Figure 11. The sine look-up table computes $\sin(2\pi R/2N)$ to the resolution of the sine table. The output of the sine-table is then sent to a DAC which outputs a voltage proportional to the sine table value to the M-bit resolution of the DAC. The result of this process is to produce a stepped sine wave output which has very low levels of spurs and phase jitter when low pass filtered. Figure 12 shows a typical stepped output of a sine output DDS.

The levels of spurs and phase noise in this DDS are directly related to the accuracy and resolution of the sine table and DAC. Generating a high resolution sine value directly from a single table usually requires a prohibitively large ROM, so techniques have been developed to reduce the ROM requirements by computing the sine value from several lower resolution tables (Sunderland 1984).

Phase Interpolation DDS

A phase interpolation DDS (Hassun, 1984; Kochemasov, 1982; DesBrisay, 1970; Crowley, 1982; Schineller, 1982; Rohde, 1981; Rohde, 1983; Gillette, 1969; Nossen, 1980; Bjerede, 1976a; Bjerede, 1976b) is similar to the sine output DDS in that it produces

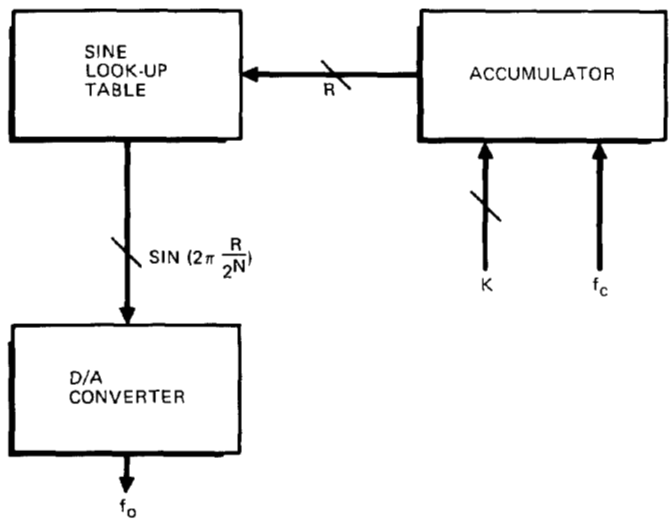


FIGURE 11. SINE OUTPUT DIRECT DIGITAL SYNTHESIZER

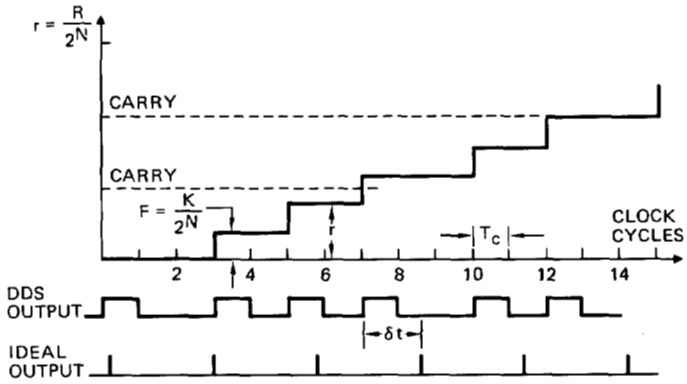


FIGURE 10. FRACTIONAL DIVIDER TYPICAL OUTPUT WAVEFORM

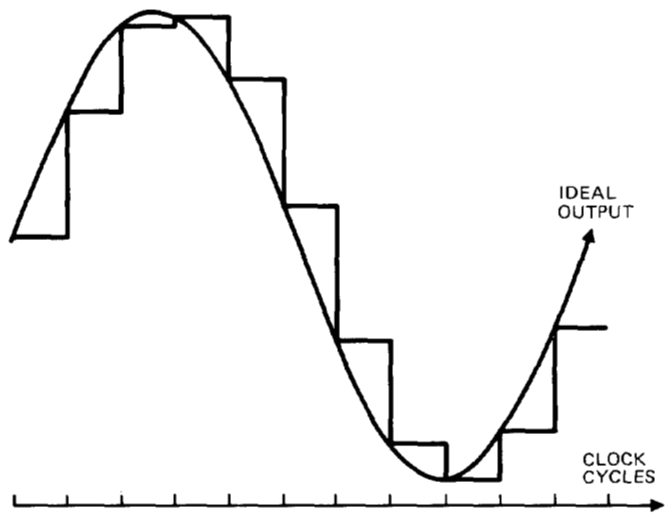


FIGURE 12. TYPICAL SINE OUTPUT DIRECT DIGITAL SYNTHESIS WAVEFORM

lower spurs, but it does not require a sine look-up table. Two versions are shown in Figures 13 and 14. The phase interpolation DDS utilizes the fact that, whenever an output transition occurs in a pulse output DDS or a fractional divider, the accumulator register value R is proportional to the time or phase difference between the output transitions of the DDS and that of an ideal frequency generator. Thus if R is used to phase shift or delay the output of a pulse output or fractional divider DDS, lower phase is jitter and spurs will result. In Figure 13, the output phase shifted using a phase lock loop (PLL) consisting of a linear phase detector, a differential loop amplifier, and a DAC driven by the DDS accumulator register (Hassun, 1984; Gillette, 1969; Nossen, 1980; Rohde, 1981; Rohde, 1983; Bjerede, 1976a; Bjerede, 1976b; Schineller, 1982; Crowley, 1982). In Figure 14 either a digitally controlled phase shifter (DesBrisay, 1970) or a digitally controlled delay generator (Kochemasov, 1982) driven by the DDS accumulator register are used to directly phase shift or delay the output. Figure 15 shows a typical output wave form from a digital phase shifter type of phase interpolation DDS. The phase jitter and spur level reductions that are achievable with phase interpolation DDS's are limited by the linearity, accuracy, and resolution of the digital-to-phase or delay conversion process.

A simplified version of the phase interpolation DDS with much narrower frequency range is the phase microstepper (Lavanceau, 1985; DesBrisay, 1970). This device uses a digitally controlled phase shifter operating off a single clock frequency to produce small variations in the clock frequency with extremely high resolution. A typical phase microstepper produces 5 MHz plus or minus one part in 1E-7 with a fractional frequency resolution of 1E-17 (Lavanceau, 1985).

Triangle Output DDS

A triangle output DDS is another variation of a

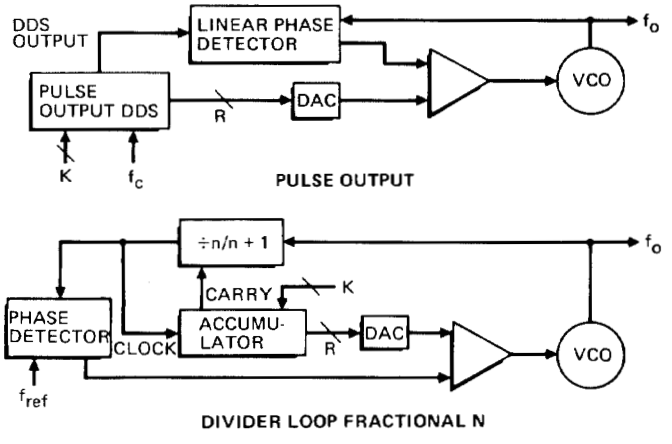


FIGURE 13. PHASE LOCK LOOP TYPE OF PHASE INTERPOLATION DIRECT DIGITAL SYNTHESIZER

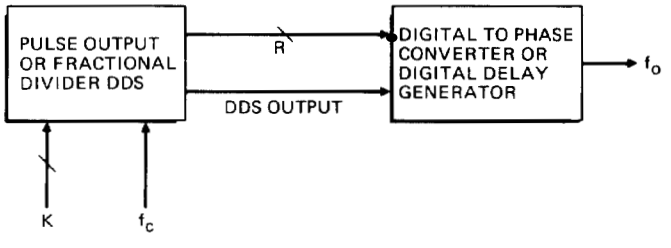


FIGURE 14. DIRECT OUTPUT TYPE OF PHASE INTERPOLATION DIRECT DIGITAL SYNTHESIZER

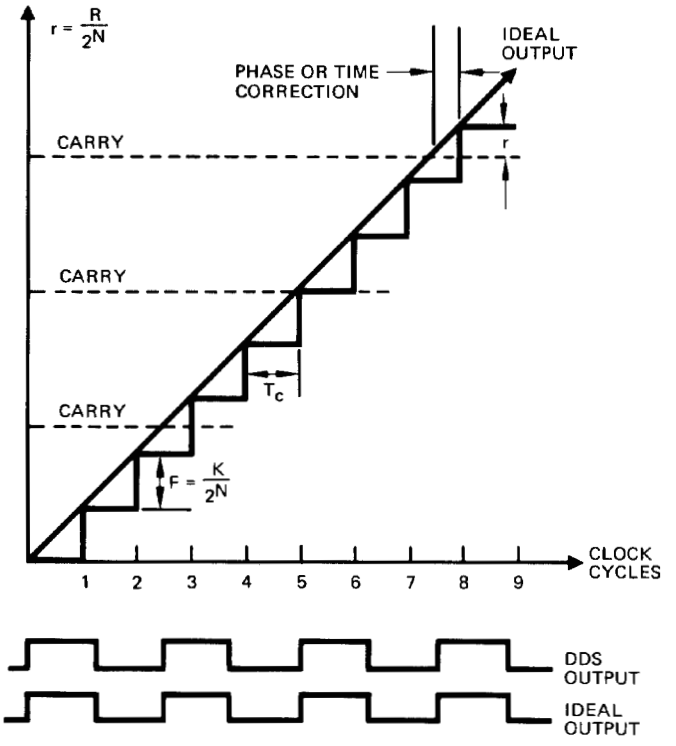


FIGURE 15. TYPICAL PHASE INTERPOLATION DIRECT DIGITAL SYNTHESIS OUTPUT

sine output DDS which does not require a sine table (DesBrisay, 1984). Its block diagram is shown in Figure 16 along with a typical output. In this type of DDS, the accumulator register value R of a pulse output DDS is used to drive a DAC directly after passing through a bit complement logic circuit. This produces a stepped triangle wave output. This triangle wave output has lower spurs than the outputs of a fractional divider or pulse output DDS.

Jitter Injection DDS

Wheatley has patented (Wheatley, 1983) a random jitter injection technique for use on a pulse output DDS which reduces the size of the spectral spurs in the output. This technique reduces the spurs by destroying the periodicity of the phase deviation patterns of the output transitions (Wheatley, 1981). The technique has two embodiments as shown in Figures 17 and 18. The periodicity in both embodiments is destroyed by randomizing the accumulation process with a digital random word. In doing so, one trades off spur levels for

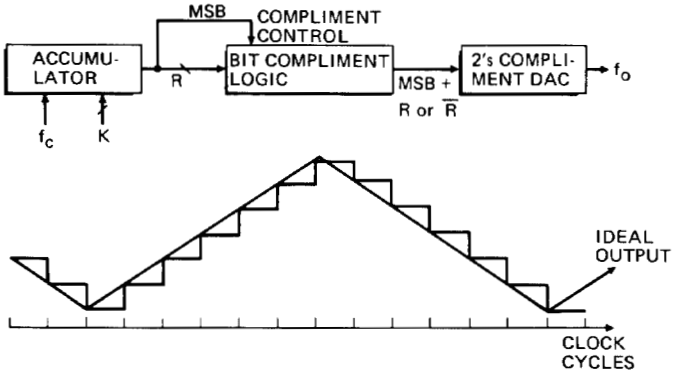
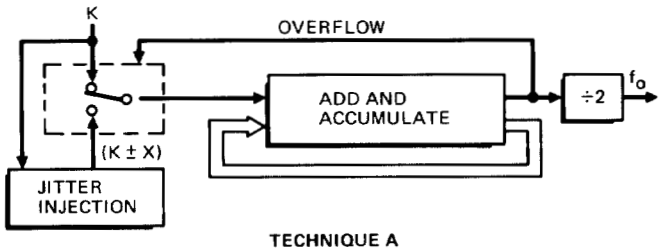


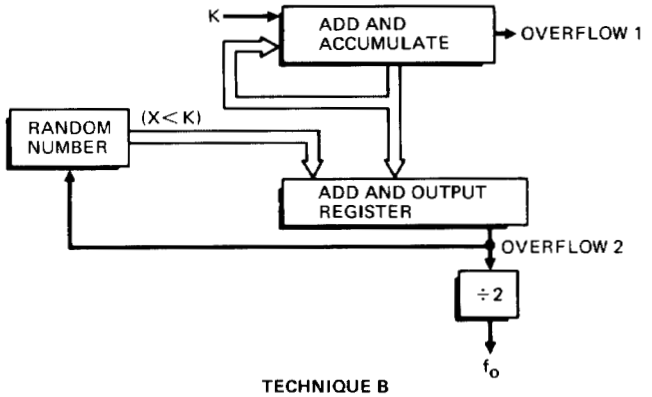
FIGURE 16. TRIANGLE OUTPUT DIRECT DIGITAL SYNTHESIS AND TYPICAL OUTPUT

increased random phase noise. Figure 19 shows a sample spectrum of a pulse output DDS with and without the Wheatley technique.



TECHNIQUE A

FIGURE 17. WHEATLEY RANDOM JITTERING TECHNIQUE A



TECHNIQUE B

FIGURE 18. WHEATLEY RANDOM JITTERING TECHNIQUE B

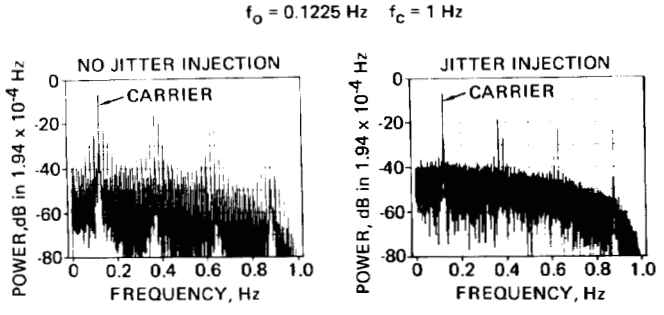


FIGURE 19. SIMULATION OF TYPICAL JITTER INJECTION DIRECT DIGITAL SYNTHESIS OUTPUT*

*COURTESY OF J. DAMIR, A. STRODTBECK, AND M. FASHANO, HUGHES AIRCRAFT COMPANY

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