

near 1 kHz, the receiver has at least 10 dB sideband suppression over much of the 300 Hz to 3 kHz speech range. The receive signal sounds like it has rapid QSB—identical to the familiar Airplane scatter QSB often experienced by VHF SSB operators.

Wideband passive hybrid SSB transmit, DSB receive. Better still—not bad at all. Probably quite acceptable for speech. The hybrid provides 15 to 20 dB of sideband suppression across most of the audio range. Rapid QSB can still be easily heard on music, but at nearly 20 dB down, the amount of QSB is only a few dB.

Wideband passive hybrid SSB transmit, single-hybrid receive. Very good. The combined sideband suppression of more than 25 dB across the audio range is good enough that it is hard to detect any effects from the inadequately suppressed sidebands.

Later experiments using a single-hybrid on both the receiver and exciter worked well for voice. Fig 9.19 is a complete schematic of a simple voice exciter. Adding a low-noise, high-gain audio amplifier and switching results in a simple SSB transceiver, as shown in Fig 9.20.

The passive SSB modulator and demodulator with modest performance are significantly simpler than “serious” phasing receivers and excitors, and may be appropriate for some applications. Fig 9.21 illustrates a modulator-demodulator circuit using a dual quadrature hybrid that provides 20 dB of opposite sideband suppression over a reasonable portion of the audio range. While over-simplified for most applications, its advantages are significant:

1. It is passive and bi-directional
2. There are no adjustments
3. Component values are not critical

The simple phasing systems described above do not provide the sideband suppression performance we have come to expect from conventional superheterodyne filter systems. We usually require better performance from the radios we design and build.

Good performance is available from pairs of 2nd-order networks, using common op-amp circuitry or RC networks like the classic B&W 2Q4. 2nd order networks are capable of providing sideband suppression of more than 30 dB across a voice bandwidth. Pairs of 3rd order networks

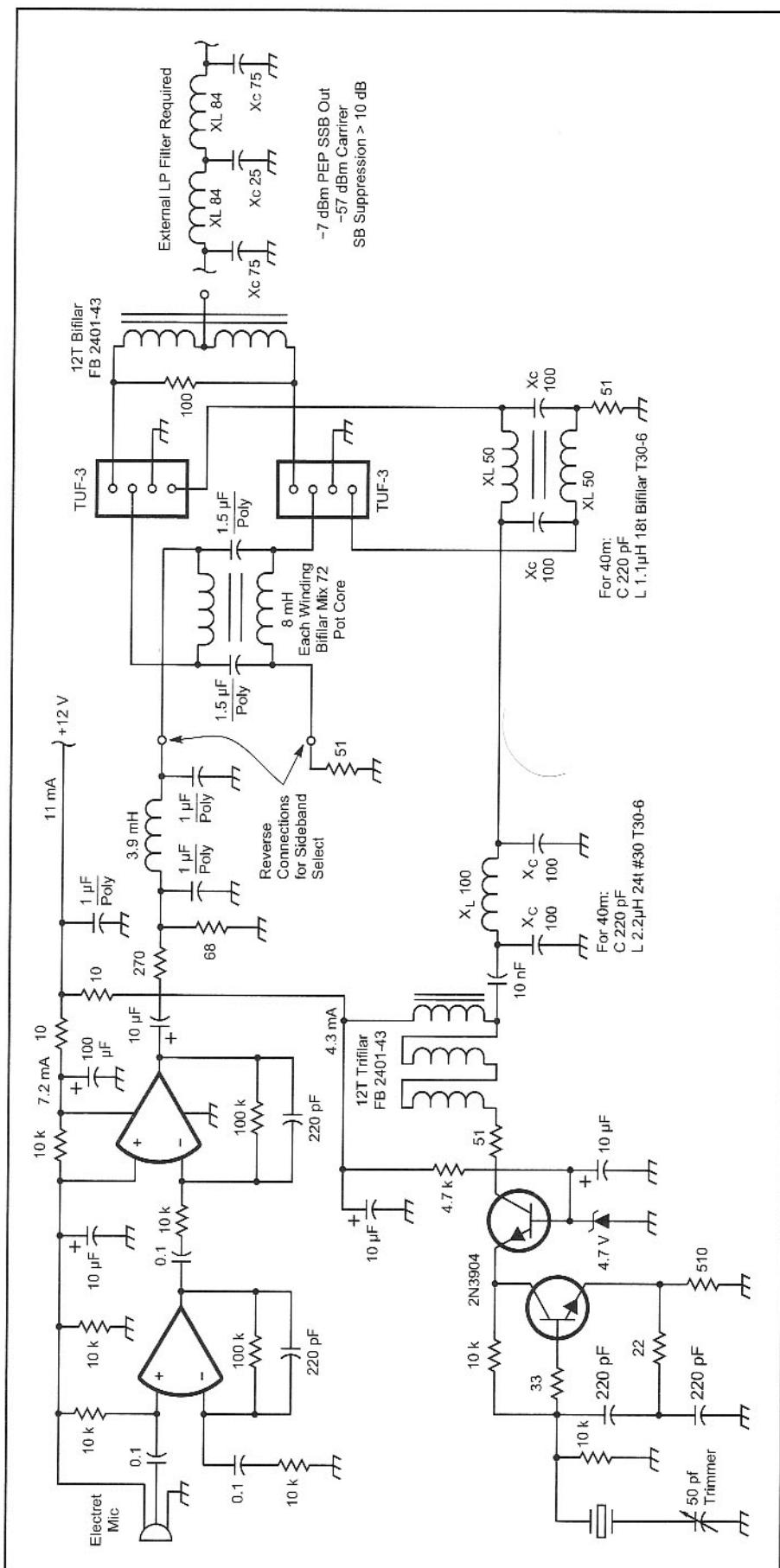


Fig 9.19—A complete schematic of a simple SSB exciter.

using op-amps easily provide more than 40 dB. Since op-amps, resistors and capacitors are all very inexpensive, the cost saving from relaxing the sideband suppression specification from 40 to 30 dB is seldom worthwhile. On the other hand, there is interest and value in revisiting classic circuitry, and a design using modern discrete components and a classic passive audio phase-shift network is appealing. As an aside—not every design should be built. There is tremendous value in notebook designs that work the problem without making it to the bench, and experiments on the bench that are never connected to the antenna.

Opposite Sideband Suppression in Receivers

For receivers, arguments can be made for almost any level of audio image suppression, from 100 dB to none at all. It is hard for a receiver with any degree of useful selectivity to compare with the sonic appeal of a wide-open direct conversion receiver or properly adjusted Regen. On the other hand, CW operators during a contest often try to copy weak signals at the noise floor in the presence of signals 90 dB stronger only a few kHz away. There is no easy “40 dB is enough” answer for receivers. Instead, there is a complex relationship between receiver topology, spectral purity, dynamic range, circuit complexity, expense, difficulty of adjustment, the need for AGC, operating habits, audio distortion, LO phase noise...the list is long enough that virtually every receiver experimenter will come up with a different requirement. There is, however, one piece of advice that has been distilled from several generations of SSB and CW receiver experimenters: time spent experimenting with a good, straight DSB direct conversion receiver connected to an antenna is part of your receiver education. You can't be a gourmet if you have never set foot in a kitchen, and there is a significant knowledge gap in your receiver background if you haven't performed the fundamental experiment of collecting radio signals on a wire, converting them to audio with a mixer and oscillator, amplifying them with a few transistors, and listening to them on headphones. This basic experience is the common ground shared by receiver experimenters.

Since there is no easy sideband suppression number, we will take a different approach to receiver opposite sideband suppression: how difficult it is to meet a particular spec. The simplest receivers have no provisions for reducing the oppo-

site sideband, and they are so simple that the question “is additional selectivity desirable enough to warrant significant additional circuitry?” must always be asked. For many portable, emergency, and casual listening requirements, the answer is no. Furthermore, the simple receiver is such an important standard of comparison that it is useful to periodically design and build simple receivers for applications where relaxed selectivity requirements or better sounding audio are the goal.

Receivers Designed for Less than 20 dB Opposite Sideband Suppression

Having built and experimented with the “no selectivity” variant, a simple drop-in image-reject mixer can make a useful improvement in the performance of basic CW and SSB receivers. The circuit in Fig 9.22 can replace the diode ring mixer in a 40-meter direct conversion rig. Opposite sideband suppression will be moderately good at a single frequency, near 800 Hz, and will degrade rapidly as the receiver is tuned away in either direction. The receiver response sounds very much like that of a 1940's classic receiver with a single crystal filter and front panel phasing control—with a single deep notch in the opposite sideband. The performance of this circuit is disappointing on the test bench, but it can sound very good on bands with few signals close to the noise level. It is primarily useful for CW, when combined with a narrow audio CW filter. Besides the obvious advantage of being a drop-in replacement for a diode ring mixer in a DSB receiver, this circuit is also attractive because it is entirely passive.

Receivers Designed for more than 30 dB Opposite Sideband Suppression

The next level of circuit complexity involves the use of a matched pair of product detectors and audio preamplifiers, driving a classic passive RC phase-shift network. This is appealing for historical reasons, particularly if discrete FETs are used to replace the standard vacuum tube functions. Simple direct conversion receiver circuits with good opposite sideband suppression—30 dB across a SSB bandwidth or 40 dB across a CW band—may be designed by optimizing for reduced parts count. Numerous examples of such receivers have appeared in European journals such as *Sprat* over the years. Once again,

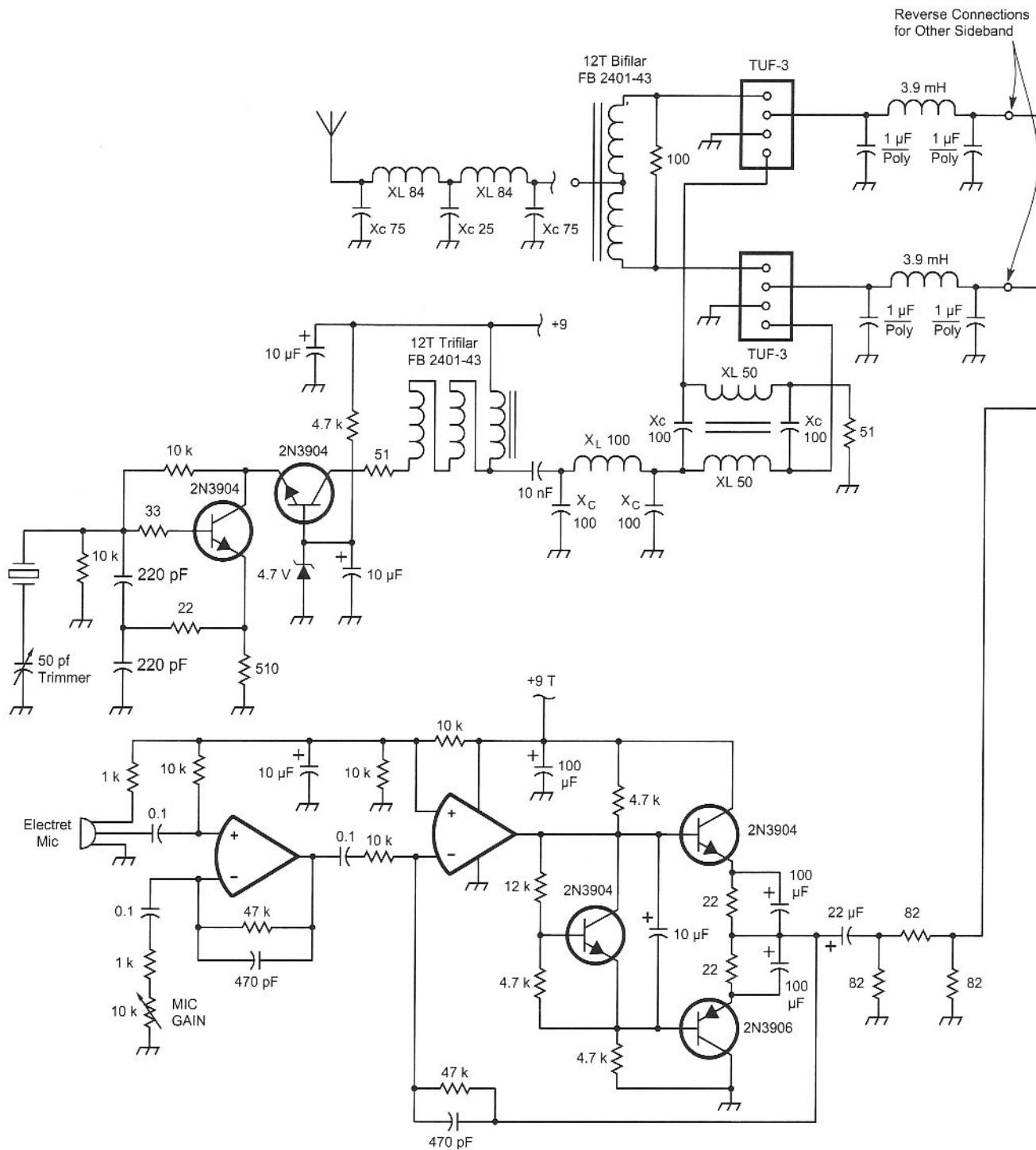
these receivers are appealing as design projects revisiting the classic homebrew projects of the past century. The drawback to these discrete transistor receivers is that they don't take advantage of the remarkable properties of operational amplifiers. Op-amps are little analog mathematical processors, and even if you skipped the math, it is important to remember that op-amps do math with fewer errors and approximations than discrete components.

Receivers Designed for more than 40 dB Opposite Sideband Suppression

If op-amps are to be used in a receiver, there is little point in restricting the audio phase-shift networks to 2nd order, and almost nothing to be gained by going to 4th order. Standard 3rd order networks can reliably provide more than 40 dB of opposite sideband suppression, the point at which limitations other than audio phase shift network phase and amplitude accuracy begin to dominate. The miniR2 block diagram shown in Fig 9.23, is an example of a good basic design for an image-reject direct conversion receiver. For a receiver without AGC, 40 dB of opposite sideband suppression sounds astonishingly good. CW signals simply disappear when a good phasing receiver is tuned through zero beat. This is a revelation to experimenters familiar with conventional superhet designs using SSB bandwidth filters, or simple CW crystal filters. The 40 dB opposite sideband range is the most practical realm for direct conversion phasing receivers. Receivers at this opposite sideband suppression level sound very good, can be reliably reproduced, provide more than enough selectivity for most HF and virtually all VHF applications, and will perform without adjustment indefinitely.

Receivers Designed for more than 50 dB Opposite Sideband Suppression

A well-designed 3rd order op-amp all-pass network built with selected components can provide more than 50 dB of opposite sideband suppression. 4th order networks can provide more than 70 dB of opposite sideband suppression, on paper. Large polyphase networks are capable of similar numbers. The difficulty is that very small differences in the phase-versus-audio frequency and amplitude-versus-audio frequency between the two channels puts a limit on sideband suppression. For 40 dB



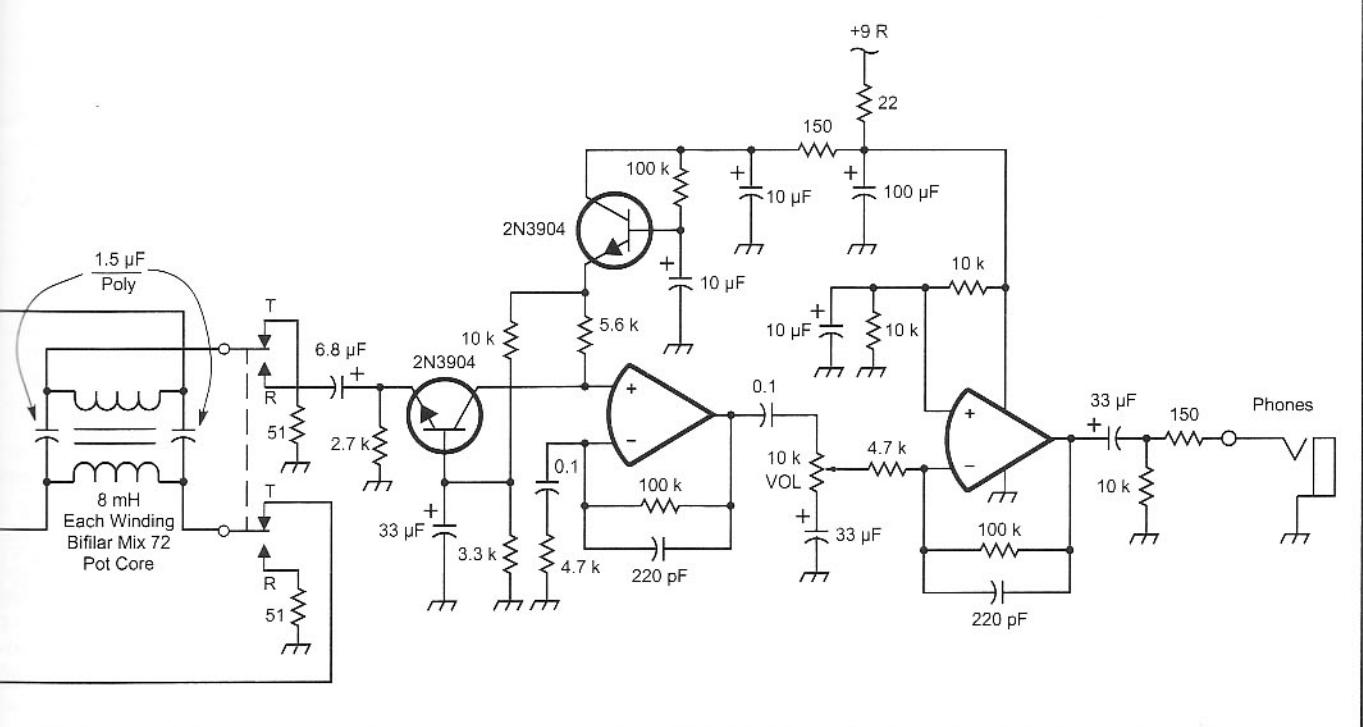


Fig 9.20—SSB transceiver schematic.

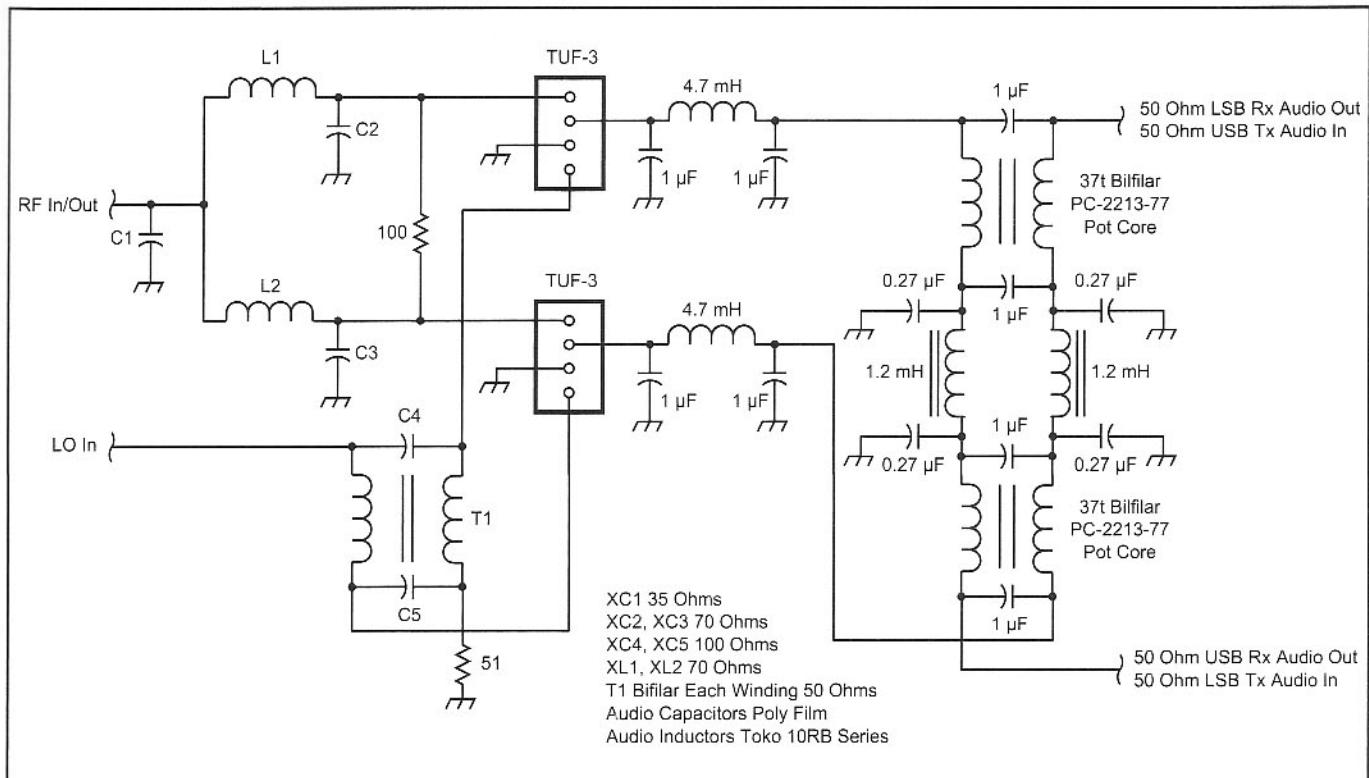


Fig 9.21—A modulator-demodulator circuit using a dual quadrature hybrid that provides 20 dB of opposite sideband suppression over a reasonable portion of the audio range.

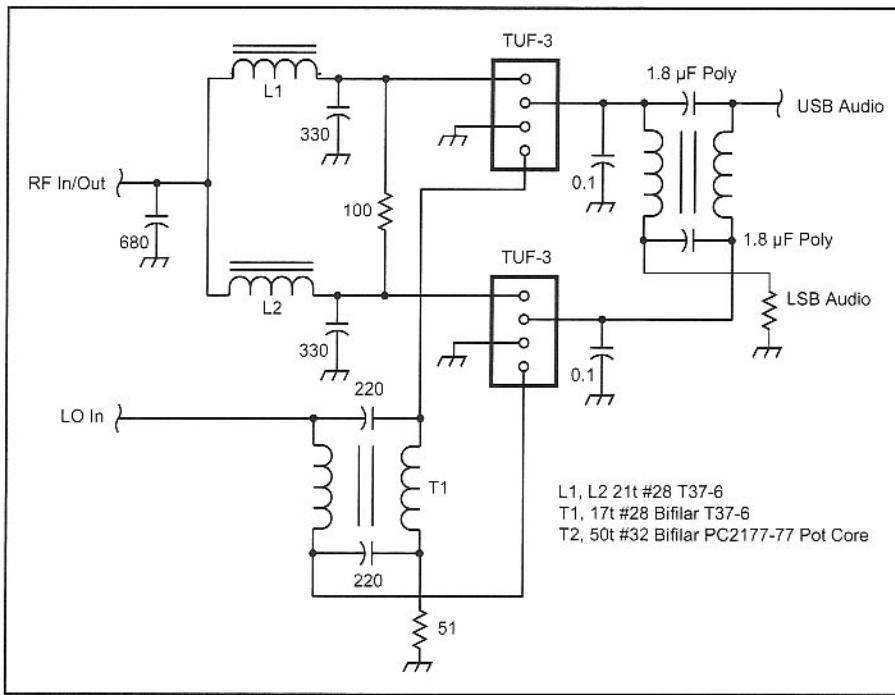


Fig 9.22—A simple drop-in 40-m band image-reject mixer can make a useful improvement in the performance of basic CW and SSB receivers.

of suppression, differences must be less than one degree or 0.1 dB across the whole audio range. For 60 dB suppression, differences between channels must be less than 0.1 degree or 0.01 dB. The errors can occur anywhere in the system from the point where the I and Q channels split to the point where they are summed. Much attention has been given to the design of audio phase shift networks with arbitrarily small phase and amplitude errors, but the rest of the circuitry in the receiver I and Q channels needs to be perfect as well. Simply replacing the op-amp third order audio phase shift network in the January 1993 *QST* receiver (hereafter referred to as the “R2”) with a nearly perfect DSP version does not significantly improve opposite sideband suppression.

If the R2 circuit is built using carefully matched (within 0.1%) components throughout, the opposite sideband suppression will be limited by differences in bandpass diplexer driving point impedance between the I and Q channels. Fig 9.24 shows the complete schematic of the bandpass diplexer used in the R2. This is a doubly terminated network, intended for 50 Ω input and output terminations. The input termination is provided by the IF port impedance of the diode ring mixer. The output termination is provided by the input impedance of the grounded base amplifiers, which is determined primarily by the biasing. For 50 dB opposite sideband suppression, even the bias resistors must be matched to within 1%. The IF port impedance of a diode ring mixer varies

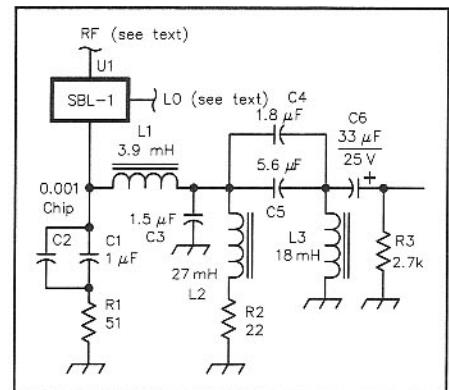


Fig 9.24—The complete schematic of the bandpass diplexer used in the R2.

with LO drive, which often changes across the receiver tuning range when using a quadrature hybrid in the LO signal path. The PSPICE simulation result in Fig 9.25 shows the variation in phase across the audio passband when the driving impedance is 50, 75, and 100 Ω. For opposite sideband suppression of more than 40 dB across the 300 – 3000 Hz audio band the I and Q channel IF port impedances should differ by no more than 6 Ω. For 60 dB opposite sideband suppression, the I and Q port mixer IF impedances must be matched to within 0.6 Ω. This tight control of IF port impedance is more than we can expect from diode ring mixers.

Fig 9.26 shows the simplified diplexer networks used in the miniR2. Note that the 300 Hz High-Pass LC circuit has been eliminated, and the Low-Pass corner frequency has been moved up to 10 kHz. The miniR2 diplexer circuit is a little more tolerant of differences between mixer IF port impedances. Fig 9.27 is a PSPICE simulation result showing miniR2 diplexer phase differences when the driving point impedance is 50, 75, and 100 Ω. This network is more tolerant of driving point impedance variations: plus or minus 9 Ω for 40 dB and 0.8 Ω for 60 dB opposite sideband suppres-

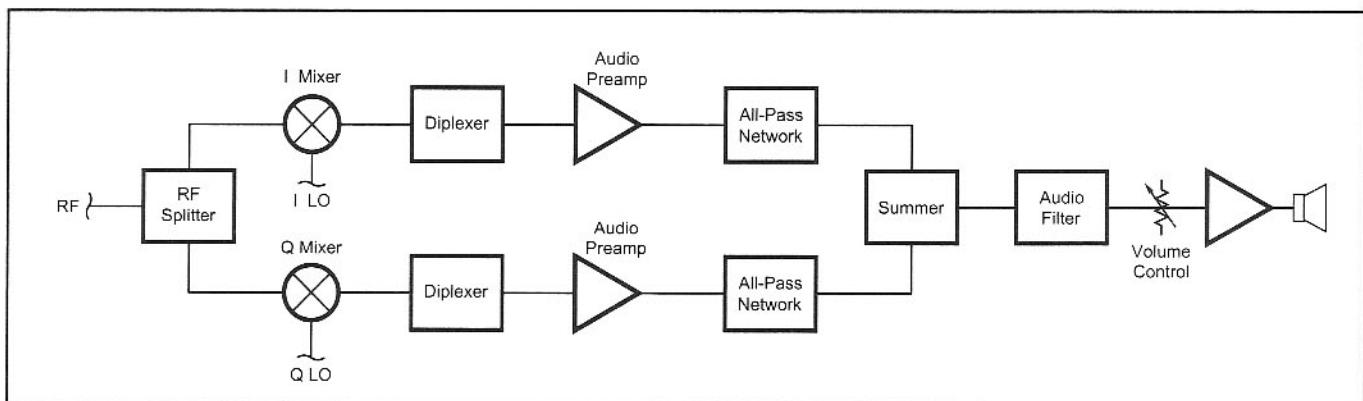


Fig 9.23—An example of a good basic design for an image-reject direct conversion receiver.

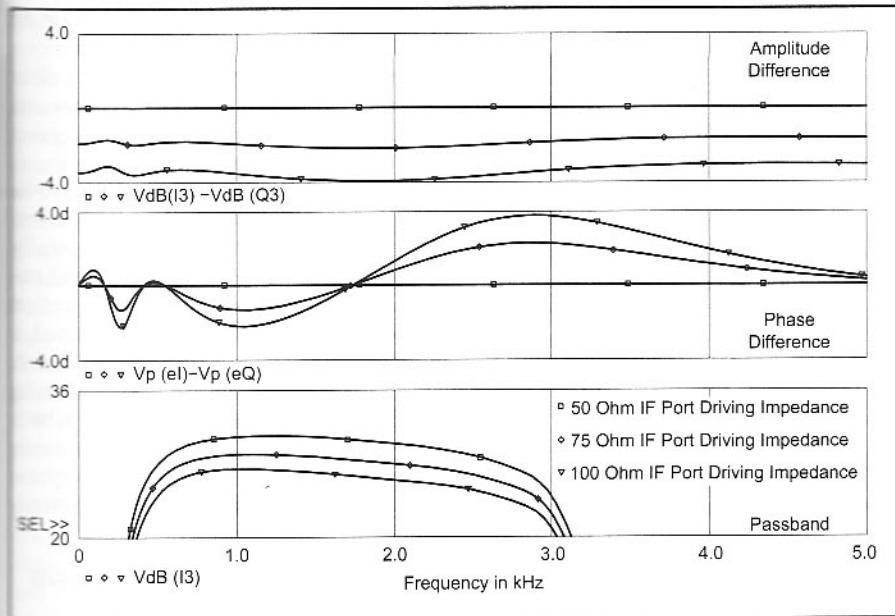


Fig 9.25—A PSPICE simulation shows the variation in phase and amplitude across the R2 audio passband when the driving impedance is 50, 75, and 100 Ω .

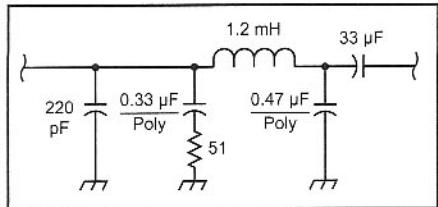


Fig 9.26—The simplified diplexer networks used in the miniR2.

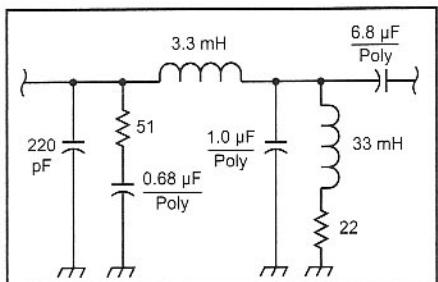


Fig 9.28—To reduce sensitivity to mixer IF port impedance and remove loose tolerance electrolytic capacitors from the I and Q signal paths, a new bandpass diplexer network was designed.

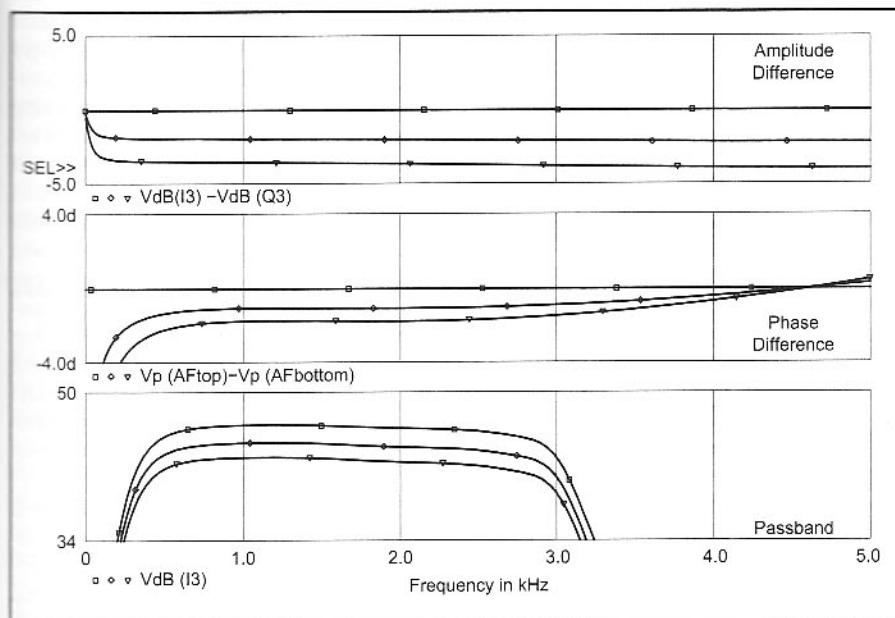


Fig 9.27—A PSPICE simulation result showing miniR2 diplexer amplitude and phase differences when the driving point impedance is 50, 75, and 100 Ω . This network is more tolerant of driving point impedance variations.

sion, if everything else in the receiver is perfect.

R2 receivers routinely exhibit 41 dB of opposite sideband suppression across the band, while miniR2 receivers typically are a few dB better. This indicates that sensitivity to mixer IF port impedance is well balanced with the errors obtained from using 1% tolerance components in the I and Q audio channels. Improving either just the phase shift network performance or just the IF port match will not signifi-

cantly improve receiver opposite sideband suppression, because the other source of error will then limit performance.

To reduce sensitivity to mixer IF port impedance and remove loose tolerance electrolytic capacitors from the I and Q signal paths, a new bandpass diplexer network was designed. The new network is shown in Fig 9.28. It is simpler than the R2 network by 1 inductor, and the AC-coupled output eliminates the need for a blocking capacitor on the input to the audio preamp.

Diplexer Driving Point Impedance Measurements

An experimental receiver to study the effect of mixer IF impedance was built using the new diplexer circuit and all components matched to within 0.1%. LO drive at 14 MHz was provided by a Kanga Universal IQ VFO with the outputs carefully adjusted for equal amplitude and 90-degree phase shift. An independent phase trimmer was used on one mixer RF port. This receiver provided 43 dB of opposite sideband suppression across the 300 to 3000 Hz audio band. Then, the mixer IF ports were isolated from the diplexer inputs with 50- Ω 10-dB instrumentation attenuators. After readjusting the amplitude and phase trimmers, opposite sideband suppression improved to more than 50 dB across the 300 to 3000 Hz audio band. Switching from 10-dB to 20-dB attenuators and readjusting made a further small improvement—however at more than 53 dB opposite sideband suppression, all adjustments are an order of magnitude more critical than at the 40 dB level.

PSPICE simulations show that adding 6-dB pads between the mixer IF ports and diplexer inputs permits the experimental receiver circuit with carefully matched components to achieve 50 dB of opposite sideband suppression with a IF port impedance mismatch of up to 10 Ω . Following standard engineering practice, we

would avoid adding attenuation at this point, assuming that it would degrade receiver sensitivity, but standard practice is incorrect in this case. In fact the proper use of attenuation may permit us to redistribute receiver gain to improve both sensitivity and dynamic range.

Effect of Mixer IF Port Attenuation on Receiver Noise Figure

First we need to examine receiver noise figure. The techniques for measuring, calculating and even defining mixer noise figures are still evolving. A rigorous treatment is beyond the scope of this text. Standard practice calls for us to measure the audio amplifier noise figure (typically 5 to 6 dB for the R2 and miniR2 circuits) and add mixer conversion loss to obtain receiver noise figure. The resulting 12 dB noise figure is usually optimistic in practice, in part because mixers have excess noise when used with low frequency IFs. The excess noise has a 1/f character, but it is a mistake to assume that we should be able to observe a smooth 1/f spectrum in the noise output of a mixer. Low frequency diode noise mechanisms are not well understood, and the noise output varies widely between devices—even of the same part number and cut from the same semiconductor wafer. Furthermore, the noise output may have spectral peaks and dips that vary considerably from a smooth 1/f curve. Measurements of a small sample of TUF-1 mixers revealed excess baseband noise in an SSB bandwidth of between 1 dB and 7 dB. If a mixer has excess noise, attenuation after the mixer reduces the mixer noise along with the desired signal. Thus the signal-to-noise ratio changes by less than the attenuator value.

Adding an attenuator to the IF port of a diode ring mixer has an additional benefit. Mixer distortion is measured with perfect broadband 50 Ω terminations on all ports of the mixer. It is well known that the IF port termination can have a large effect on mixer dynamic range. By adding an attenuator to the mixer IF ports, dynamic range may be improved, and the expected mixer performance will be similar to the numbers in the Mini-Circuits data book. If mixer dynamic range is improved, then additional RF preamp gain may be added before the mixers. Careful selection of RF preamp gain, noise figure, and intercept performance may permit improved third-order performance and lower noise figure than the receiver without attenuators can provide.

Receivers Designed for more than 60 dB Opposite Sideband Suppression

Even if everything can be perfectly matched, baked in, trimmed, and then operated in a stable temperature controlled environment, it is still difficult to obtain more than 60 dB of opposite sideband suppression in a pure phasing receiver, because of distortion in the I and Q channel audio gain. A miniR2 has 50 dB of audio gain between the inputs to the I and Q preamps and the summing point. The gain control is after the summer, so this 50 dB gain is always in the system. With a 5 dB audio amplifier noise figure and no excess mixer noise, the noise floor at the summing point is:

$$-204 \text{ dBW/Hz} + 5 \text{ dB Noise Figure} + 34 \text{ dB SSB Bandwidth} + 50 \text{ dB gain} = -115 \text{ dBW}$$

Using a 50-Ω reference voltage, this is an RMS noise voltage of 13 μV. For an HF application, it is common for the band noise to be 20 dB above the noise floor of the receiver. At VHF, at least 20 dB of LNA gain is likely to be used. In either case, the noise at the summing point would be about 100 μV RMS. Peaks could be much higher. A signal 60 dB above the band noise would be 0.1 V at the summing point. On the desired side of zero beat, this signal would be passed on to the volume control. On the other side of zero beat the 50 mV I channel signal would add to the –50 mV Q channel signal for a sum less than 100 μV. This means that the I and Q channels have to amplify signals 60 to 80 dB above the noise floor without distortion or compression. Harmonics and intermod products generated in the I and Q audio channels have different relative phase. It is also unreasonable to expect the two channels to have identical distortion characteristics. Distortion asymmetry is also an issue in phasing systems. Harmonic distortion is familiar to audio engineers. For harmonics more than 60 dB down, the total harmonic distortion (THD) specification is: THD < 0.1%. A receiver with THD 0.1% I and Q channels could handle an undesired signal 60 dB above the noise floor, but it would have no head room. As soon as a signal was strong enough to measure on the opposite sideband, distortion would begin to dominate. A better receiver would provide 60 dB of attenuation to a signal 80 dB above the noise floor, and no audible distortion products in the wrong sideband. Such signals are encountered on 20 meters during contests. This would require THD of 0.01% for undes-

ired 1-V signals at the op-amp summing point. While this is possible using serious audio engineering techniques, it is clear that the quest for ever-higher opposite sideband suppression in phasing receivers has a practical limit. As in phasing transmitters, very low distortion is needed in the I and Q channels of a phasing receiver. The benefit for the user is that a carefully designed phasing receiver will sound exceptionally good. If the ultimate rejection to close-in interfering signals is desired, a different receiver architecture is needed. A superhet with a fixed IF and a carefully designed combination of crystal filters and/or phasing and/or DSP can provide over 100 dB of opposite sideband suppression across the entire 300 – 3000 Hz band.

Special considerations for CW

Many phasing direct conversion receivers have been built by dedicated CW operators who have no interest whatever in SSB bandwidths. Would such receivers benefit from redesigned audio phase shift networks? No. Remember that selectivity is improved by doing a better job of *rejecting* signals in the *stopband*, not passing signals in the passband. Thus it can be argued that the optimum phase shift network for a high performance CW receiver is exactly the same as the optimum network for SSB. In addition, a good CW receiver has several bandwidths, from narrow contest filters to wide open ones used for tuning around sparsely occupied bands. One major benefit of phasing receivers is the ease of making changes to the selectivity. It is easy to add filter options if frequencies from 200 Hz to 4000 Hz on the opposite side of zero beat are suppressed.

However, some receivers are optimized for simplicity, and there are other applications of simplified phasing method image-reject circuitry. If the audio band is limited to 300 – 1200 Hz, it is possible to obtain more than 50 dB of opposite sideband suppression with a pair of second order networks. An op-amp 2nd order network optimized for a CW-only receiver is shown later in this chapter. One application for CW bandwidth image-reject mixers is as the product detector following a simple CW filter. The combination of a crystal filter and image-reject product detector circuitry can provide better performance than either is capable of alone, as is demonstrated by the radios such as the Kenwood TS-570. By distributing the selectivity between a crystal filter before IF gain and a phasing product detector, the need for a “tail end” filter is generally avoided.

9.5 BINAURAL RECEIVERS

In a Binaural IQ receiver the I and Q channels are preserved all the way to the headphones. Fig 9.29 (see next two pages) is a binaural receiver circuit from March 1999 *QST*. Sorting out the signals and interference is done using the ear-brain processor. As illustrated in the experiment described earlier, an outboard network built around an audio phase-shift network may be used to further process the I and Q channels. The network shown in Fig 9.30 provides some sideband suppression and CW selectivity. The network in Fig 9.31 provides ISB headphone output. Phasing circuitry and recombining are normally performed at low signal levels in receivers, to keep the amount of circuitry that must be precisely matched between the I and Q channels to a minimum. Binaural receivers built with standard tolerance components do not provide the I Q phase and amplitude precision needed to achieve high levels of opposite sideband suppression with outboard networks. Binaural receivers are a delightful way to listen, and also have many uses on the experimenter's bench. For example, a binaural receiver tuned across a CW signal from a crystal oscillator is a precise, low-distortion audio signal generator with matched I Q outputs—just the ticket for making circles on an X-Y oscilloscope.

Adjusting Phasing Rigs

One of the difficulties that renewed interest in phasing excitors and receivers has raised is that the lore of phasing rig adjustment has literally died out with the '40s and '50s generation of radio experimenters. Although modern components and modern component tolerances permit us to build phasing rigs that perform well beyond the capability of the classics, aligning them requires an unfamiliar set of skills. Some techniques, particularly those familiar to George Grammer at the ARRL, were well documented, but others are only preserved as vague recollections of observing the masters at work in their radio labs. Those of us who now experiment with phasing rigs have had to start from scratch and design new adjustment techniques, while remaining painfully aware that we are recreating a lost art.

In the math section, we found that we could combine all of the amplitude errors into a single term, and all of the phase errors into a single term. These two error terms are orthogonal—no amount of tweaking on the amplitude trimpot can correct a phase error, and vice versa. The situation is very much like shooting at a target. The

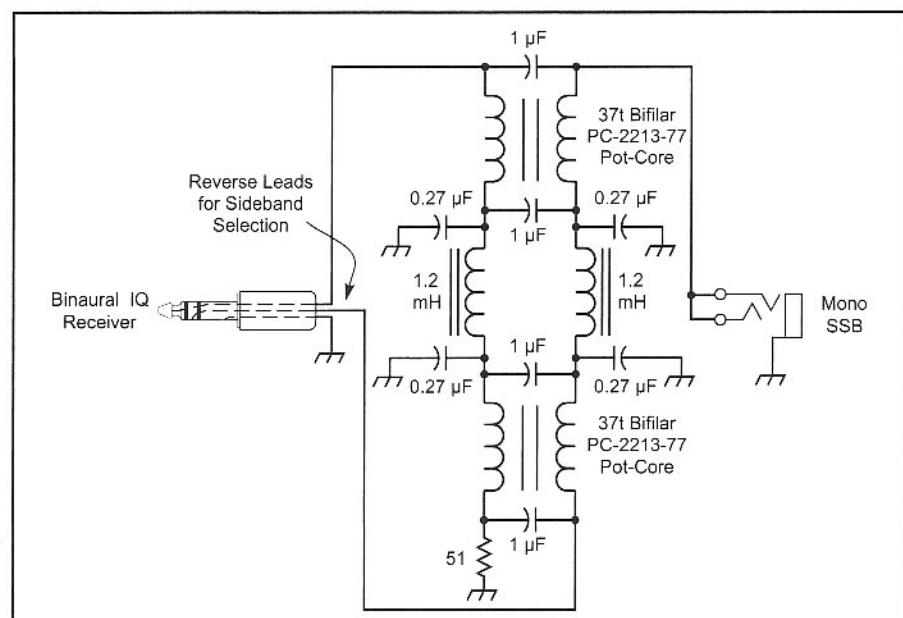


Fig 9.30—This outboard binaural network provides some sideband suppression and CW selectivity.

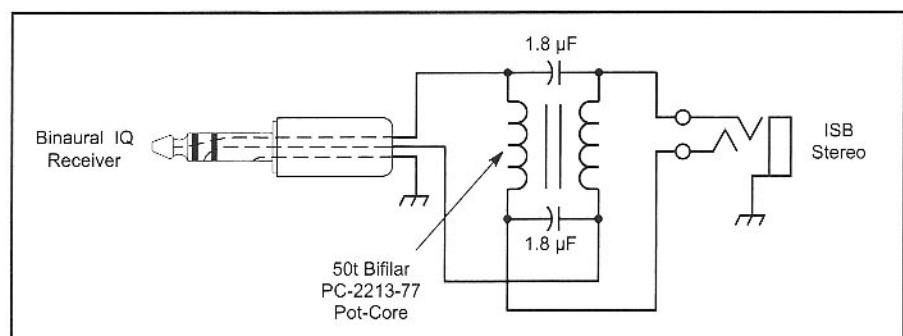


Fig 9.31—This outboard binaural network provides ISB headphone output.

sights have two adjustments: windage (or azimuth); and elevation. Both have to be properly adjusted to hit the center.

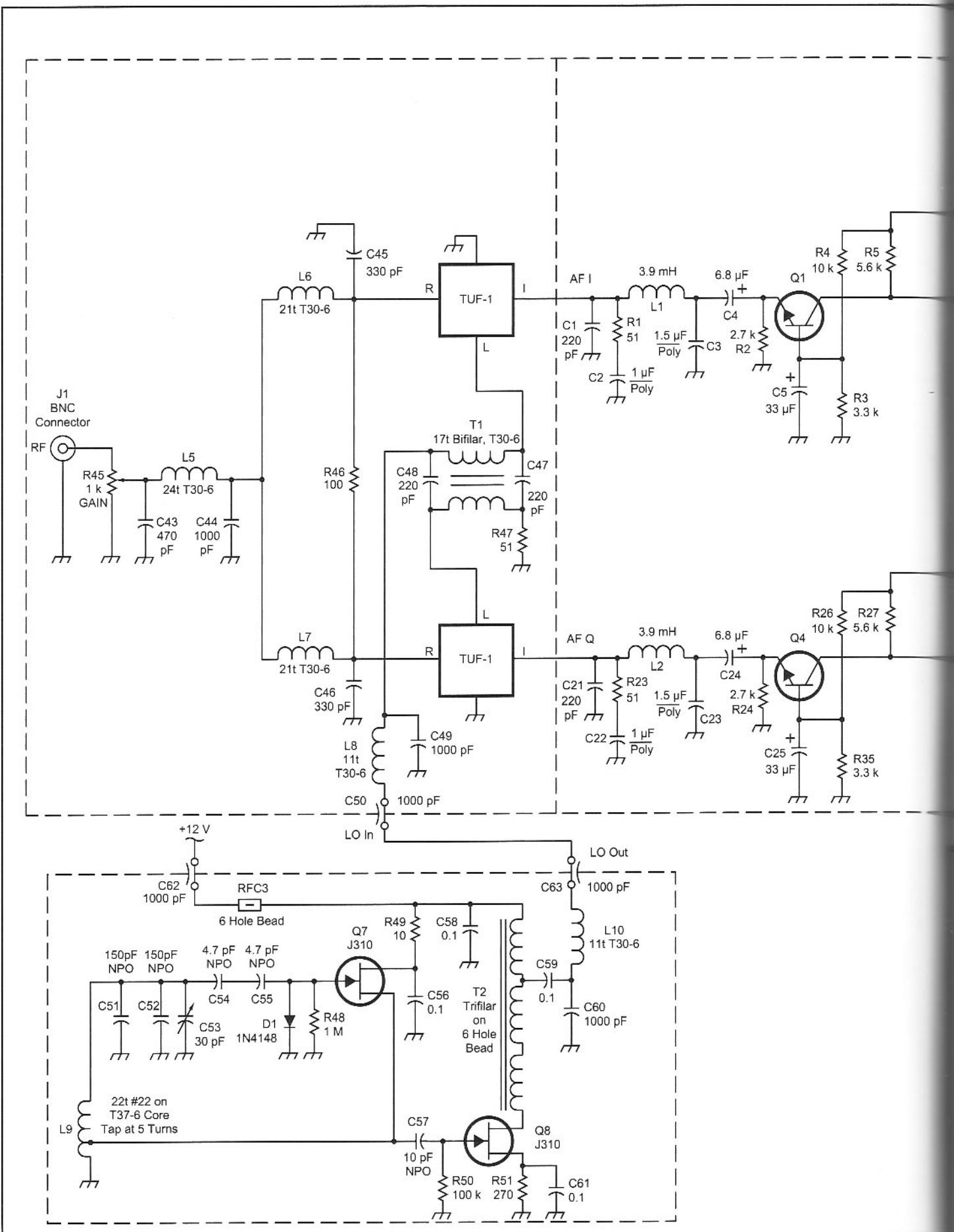
With two orthogonal error terms, a phasing rig needs two adjustments for opposite sideband suppression. This is a critically important point: no matter how many small amplitude errors we have in the system, we can tune them out with just a single amplitude balance adjustment. Similarly, all of the small phase errors in the system may be tuned out with just a single phase adjustment. We need precisely two adjustments in a phasing rig to null the opposite sideband.

The strategy for designing and building a successful phasing rig comes directly from the mathematics: design the system so that all the amplitude and phase errors are small; and include a single amplitude

balance adjustment and a single phase trim adjustment to reduce the effect of the respective errors to zero.

Unlike most other tweaks in Amateur Radio, phasing adjustments cannot be tuned for maximum smoke. The easiest way to adjust a phasing receiver is to tune across a steady CW tone from an external signal generator, adjusting the phase and amplitude trimmers for minimum response on the undesired sideband. The signal generator must have adjustable output level so that the test signal can be kept between the receiver noise floor and distortion level on both the desired and undesired sidebands. The receiver and signal generator both need to be well shielded, to prevent signals from the generator leaking into the I or Q channel.

The easiest way to adjust a phasing ex-



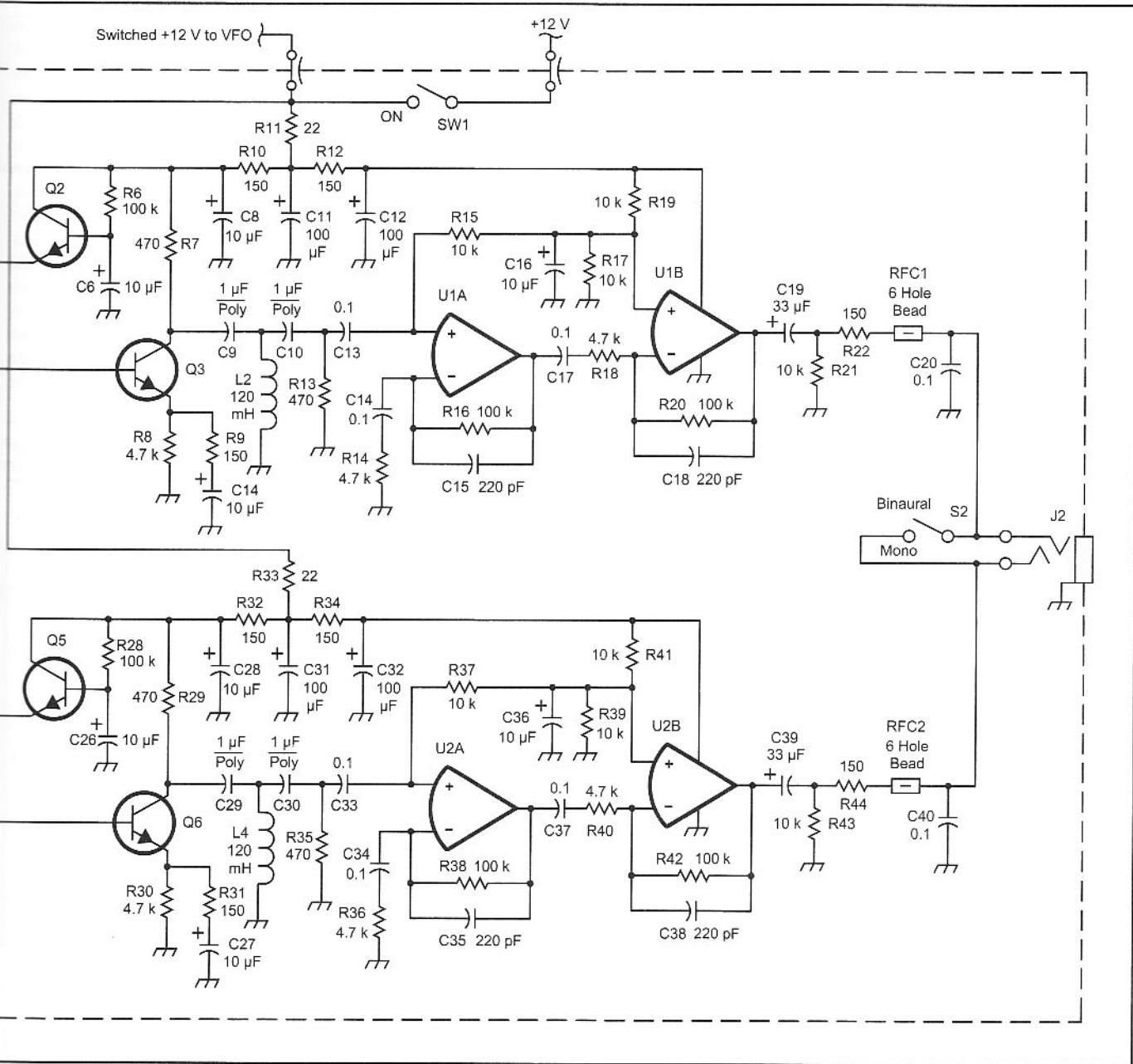


Fig 9.29—A binaural receiver circuit from March 1999 QST.

citer is to tune its low level output on a receiver with low distortion, very good selectivity, and selectable sidebands. Inject a pure sine wave audio tone into the microphone input and switch back and forth between the desired and undesired sidebands while adjusting the exciter phase and amplitude trimmers. Then sweep the audio tone frequency from 300 to 3000 Hz to verify that sideband suppression holds across the desired audio passband.

An SSB exciter with a pure sinc wave audio tone into the microphone input generates a sine wave RF output. Residual carrier and opposite sideband energy amplitude modulates the desired sine wave RF output. The SSB exciter output may be

observed on an oscilloscope, and phase and amplitude trimmers adjusted to reduce the audio amplitude variations in the output waveform. It is difficult to reduce spurious outputs by more than 40 dB while observing the exciter output on an oscilloscope, because the carrier, opposite sideband, distortion products, harmonics on the audio input tone, and power supply hum and noise all contribute to amplitude modulation of the desired sine wave RF output.

There is a clever old technique for adjusting opposite sideband suppression that does not require a good receiver or oscilloscope. The exciter output is connected through a suitable attenuator into a diode detector with headphones. With a low-

level 1000-Hz sine wave tone injected into the microphone input, the SSB exciter will have a little output at the suppressed carrier frequency f_c ; a desired sideband output 1000 Hz away; a suppressed opposite sideband 1000 Hz on the other side of the carrier frequency; and distortion products. The distortion products can be made arbitrarily small by reducing the audio tone level at the microphone input. The desired sideband, carrier, and opposite sideband all beat together in the diode detector, and the audible beats may be heard on the headphones. Imperfect carrier suppression results in a 1000-Hz audio tone, and poor opposite sideband suppression results in a 2000-Hz audio tone. The SSB exciter phase and amplitude trimmers may

be adjusted for minimum 2000-Hz tone. If the exciter has carrier balance adjustments, they may be trimmed for minimum 1000-Hz tone.

Amplitude Balance Adjustment

The amplitude balance adjustment may be a variable gain element in either the I or Q channel anywhere from the point where the two paths separate to the point where they are summed together. It is usually easier to use a variable resistor at baseband, particularly if op-amp gain blocks are included in the system. A con-

venient amplitude trimmer for receivers is a ten-turn trim pot connecting the I and Q audio channels to the inverting input of the summing amplifier. If sideband switching is implemented by interchanging the I Q connections at the input to a precise audio phase shift network pair, balancing the amplitudes before the switch results in a system that has nearly equal sideband suppression on either sideband.

A significant point to watch for is that the variable gain element does not unbalance the drive or load impedance of bandpass or all-pass networks. An amplitude adjustment that behaves differently at low audio frequencies than at high audio fre-

quencies, or that introduces phase errors across the audio frequency range, will make it impossible to obtain good opposite sideband suppression across the whole audio range. In exciters it is best to include a separate op-amp variable gain stage, to avoid upsetting either the mixer diplexer impedances or the op-amp all-pass network drive impedances. **Fig 9.32** shows possible locations for the amplitude balance adjustment in receivers, and **Fig 9.33** shows locations for exciters. Remember that only one amplitude adjustment is needed. The amplitude adjustments shown have no appreciable affect on phase. When DSP is used, it may be useful to do the

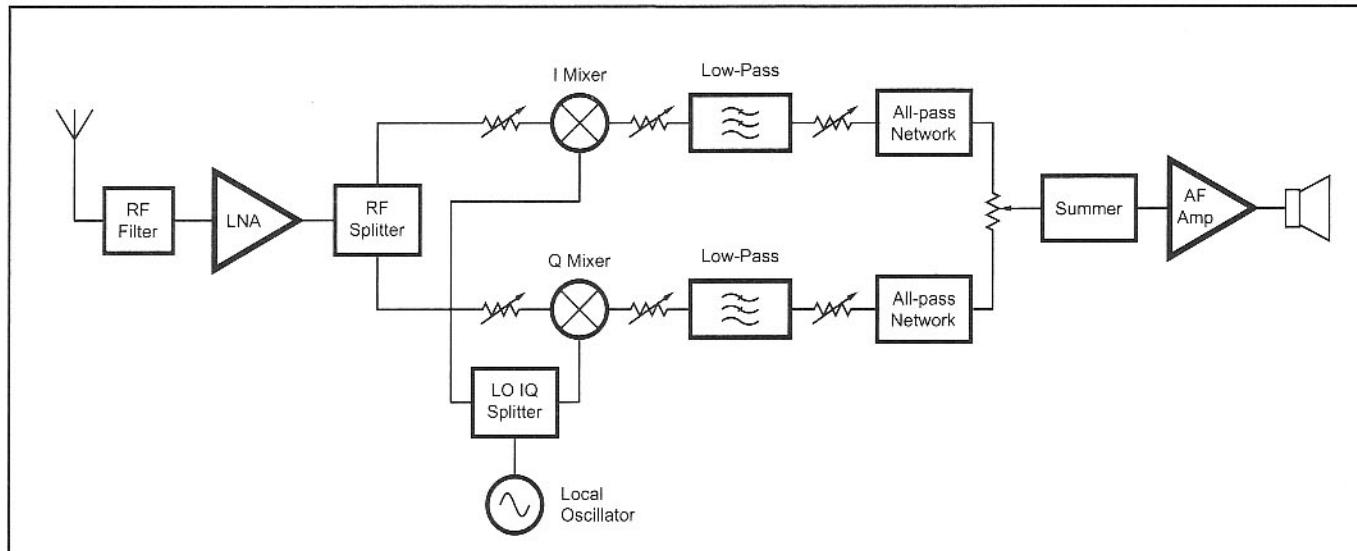


Fig 9.32—Possible locations for the amplitude balance adjustment in receivers.

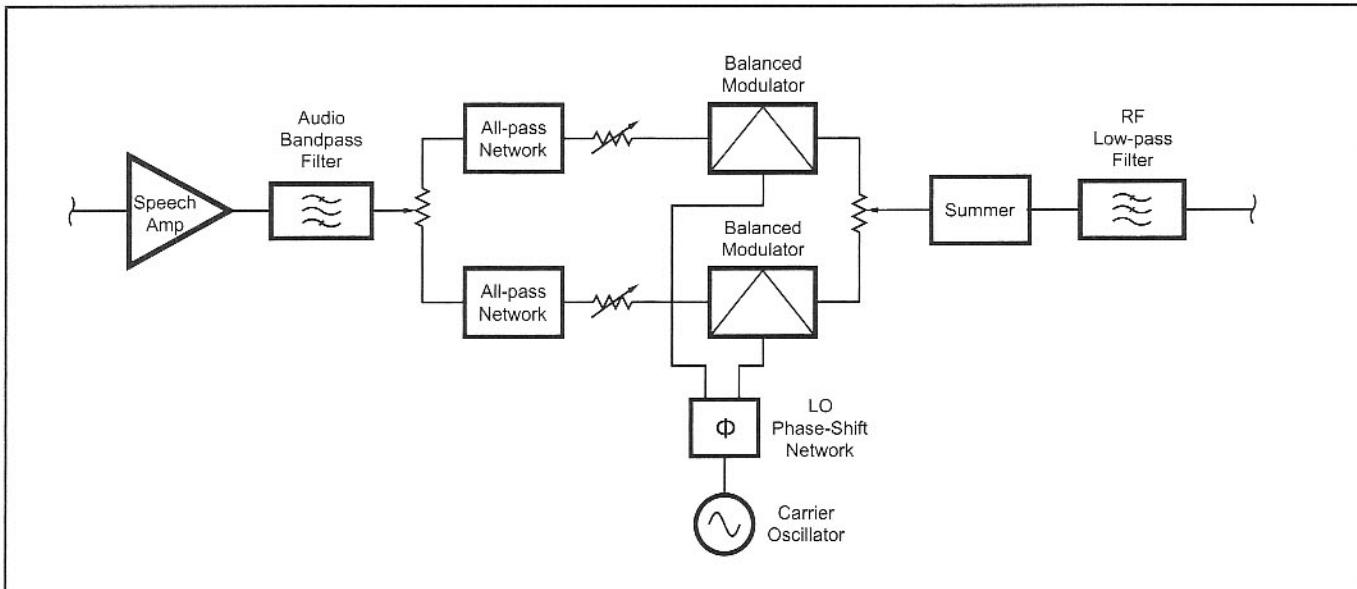


Fig 9.33—Possible locations for the amplitude balance adjustment in exciters.

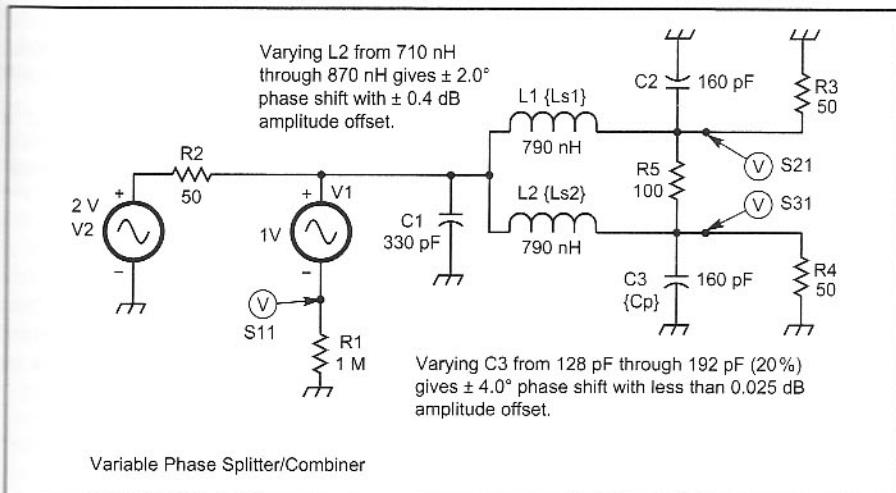


Fig 9.34—A variable phase splitter/combiner network for a 20-meter receiver or exciter. The PSPICE signal generators allow extraction of S11.

amplitude balance trimming in software.

Phase Trim Adjustment

There are many possibilities for the location of the phase trimmer. Phase may be trimmed in the I and Q signal path anywhere after the audio phase-shift network in exciters and anywhere before the audio phase-shift network in receivers. LO Phase may also be trimmed at either the I or Q mixer LO port. As long as the phase errors in the system are small, only a single phase trim adjustment is needed, and it may be anywhere in the system. Some locations for the phase trim adjustment are better than others. The amplitude balance and phase balance in a phasing rig are

mathematically independent, but it is not trivial to adjust phase without affecting amplitude as well. When mixers with saturating LO drive (for example, diode rings and Gilbert cells) are used, small changes in LO amplitude do not have a large effect on mixer performance. For this reason, including the phase trim adjustment in the mixer LO drive rather than in the RF or baseband path is good practice. On the other hand, low-pass filtering is needed at the output of phasing exciters and at the input to direct conversion receivers. A low-pass Wilkenson splitter is a useful RF splitter or combiner for a phasing rig, and using a variable capacitor for one element allows smooth adjustment of phase. Fig 9.34 illustrates a network for a 20-meter

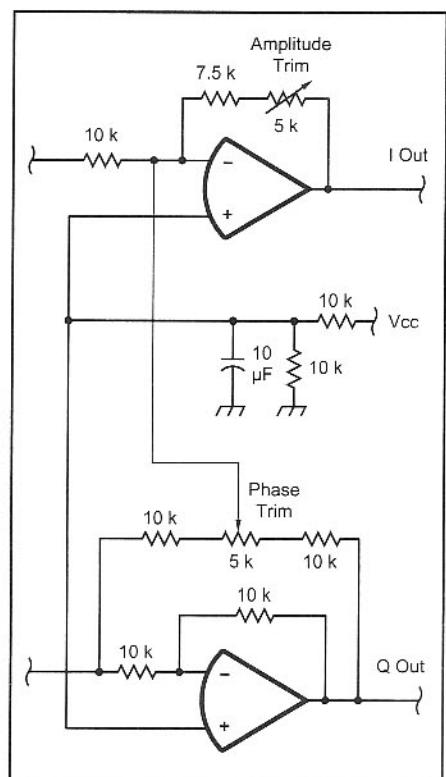


Fig 9.35—The op-amp circuit permits a small amount of Q-channel signal to be either added or subtracted to the I-channel signal.

receiver or exciter. The variable capacitor trims the phase over a plus or minus 4-degree range with 0.025 dB variation in amplitude.

It is possible to do the phase trimming at baseband, either in DSP or using op-amps. For complete suppression of the undesired

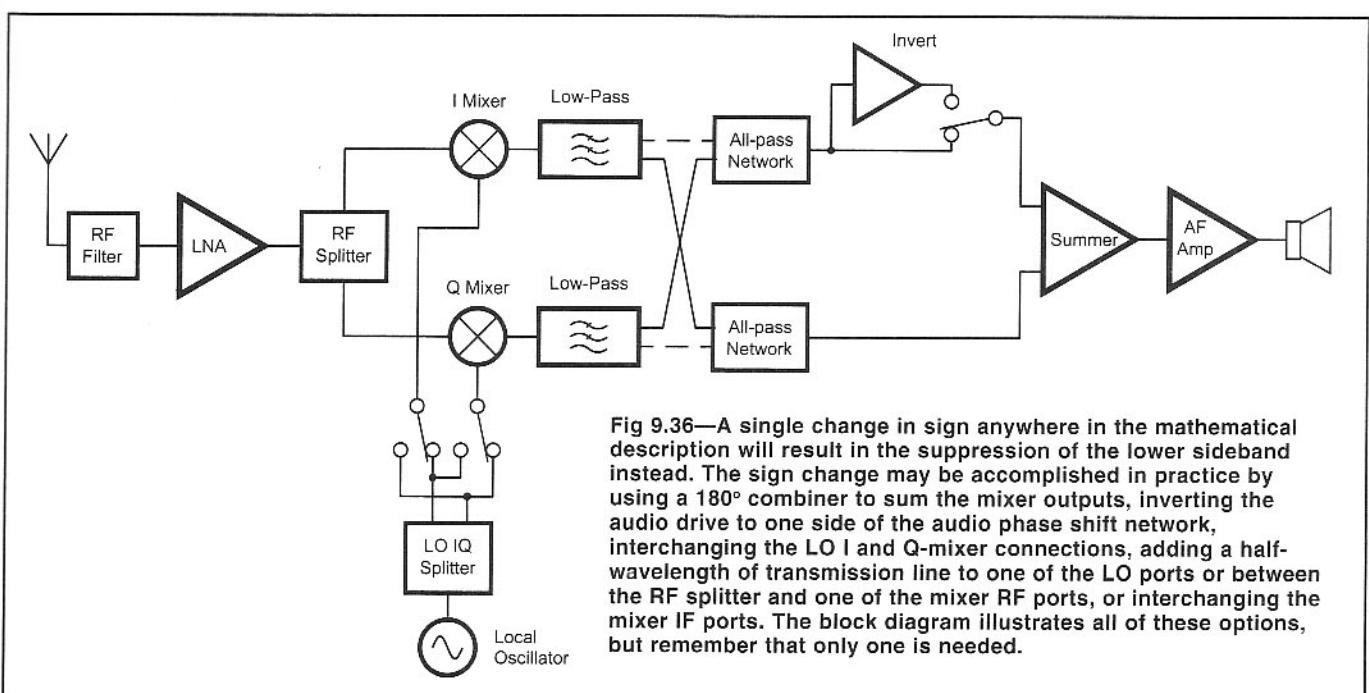


Fig 9.36—A single change in sign anywhere in the mathematical description will result in the suppression of the lower sideband instead. The sign change may be accomplished in practice by using a 180° combiner to sum the mixer outputs, inverting the audio drive to one side of the audio phase shift network, interchanging the LO I and Q-mixer connections, adding a half-wavelength of transmission line to one of the LO ports or between the RF splitter and one of the mixer RF ports, or interchanging the mixer IF ports. The block diagram illustrates all of these options, but remember that only one is needed.

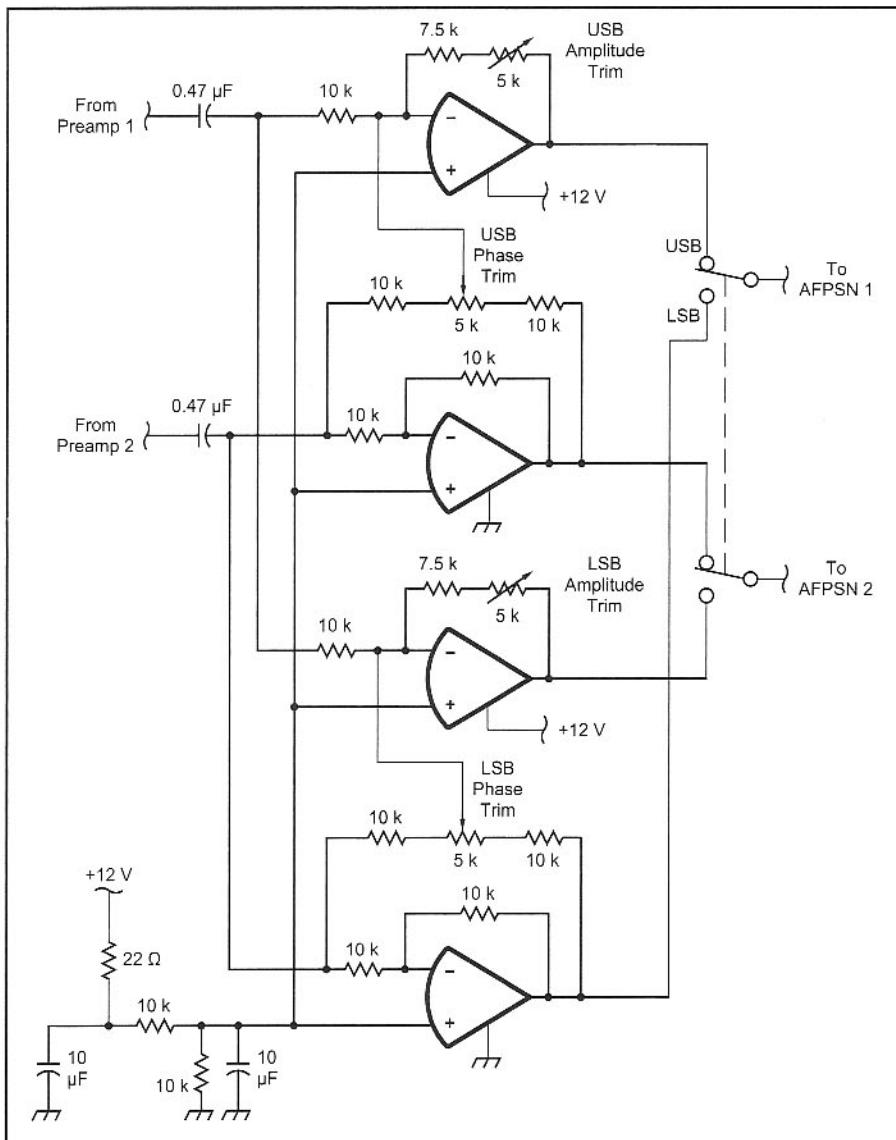


Fig 9.37—For systems that need to perform equally well on either sideband, the phase and amplitude adjustments may either be front panel mounted and adjusted every time the other sideband is selected, or an independent set of phase and amplitude adjustments may be used for each sideband.

tracted to the I channel signal. The same principle may be applied to receivers. It is necessary to do the phase trimming at a point in the audio circuitry where the signals in the two channels are 90 degrees apart, that is, between the mixers and the audio phase shift networks in both receivers and excitors.

Sideband Selection

In the mathematical description of a phasing receiver, the lower sideband is suppressed when the 90° shifted audio is multiplied with the 90° shifted LO, and the outputs of the two mixers are added. A single change in sign anywhere in the mathematical description will result in the suppression of the upper sideband instead. The sign change may be accomplished in practice by using a 180° combiner to sum the mixer outputs, inverting the audio drive to one of side of the audio phase shift network, interchanging the LO I and Q mixer connections, adding a half-wavelength of transmission line to one of the LO ports or between the RF splitter and one of the mixer RF ports, or interchanging the mixer IF ports. The block diagram in Fig 9.36 illustrates all of these options, but remember that only one is needed. Switching sidebands will generally introduce a different set of amplitude and phase errors. For systems that need to perform equally well on either sideband, the phase and amplitude adjustments may either be front panel mounted and adjusted every time the other sideband is selected, or an independent set of phase and amplitude adjustments may be used for each sideband. Fig 9.37 shows one way this may be accomplished.

sideband, the I and Q channels after the audio phase-shift network in an exciter need to have the same signal, but 90 degrees out of phase. If there is a phase error, the angle between the I and Q channels will not be 90 degrees. It is possible to obtain exactly 90 degrees of phase shift by adding a small amount of the signal in the

Q channel to the I channel. If the phase error is in the opposite direction, then a small amount of the Q channel signal can be subtracted to achieve exactly 90 degrees phase shift. The op-amp circuit in Fig 9.35, similar to one published by Blanchard, permits a small amount of Q channel signal to be either added or sub-

9.6 LO AND RF PHASE-SHIFT AND IN-PHASE SPLITTER-COMBINER NETWORKS

Numerous articles over the years have addressed the topic of LO phase shift networks for phasing rigs. The recent work by Blanchard is particularly recommended. In this section we will discuss the requirements and implications of different network selections, and present the networks that we have used extensively. Experimentation with other networks is

highly recommended, as the ones presented here are not necessarily optimum, they are just familiar.

The first topic to address is the question of where to put the 90° phase shift: in the RF path or the LO path. There is an easy answer to this question that is usually correct. The RF path contains signals that must be precisely matched in amplitude

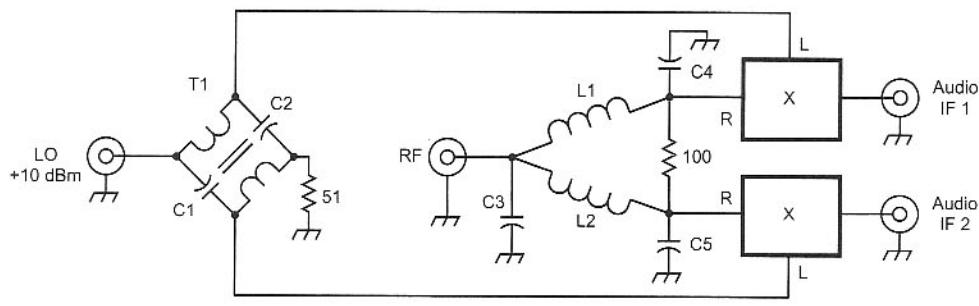
and phase between the I and Q RF channels. The LO path has a pair of sine waves with precisely defined phase, but we are usually not too concerned with LO amplitude, and we never need it to be matched to hundredths of a dB. Simple phase shift networks provide precise 90° phase shift over a wide bandwidth, but the amplitude is only balanced at a single frequency.

Equal amplitude I and Q LO may be obtained by following such a network with a limiter. Phase shift networks using splitters and lengths of transmission line, either actual coax or lumped element equivalents, have well matched amplitude over a wide frequency range, but 90° phase shift at only one frequency. It is difficult to build a passive network that provides both precise amplitude balance and a 90° output pair over a wide RF bandwidth. With wideband op-amps, we can use the same circuitry from 3 to 30 MHz that we

use from 300 to 3000 Hz, but we wouldn't want to use a wideband unity-gain op-amp circuit as the RF input stage of a receiver. On the other hand, there are many simple in-phase splitters that provide good phase and amplitude accuracy over a wide bandwidth. For this reason, we almost always put the 90° phase shift network in the LO path and an in-phase splitter in the RF path.

One reason that we might choose to use in-phase LO and quadrature RF is that the RF ports of diode-ring mixers are often better behaved than the LO ports. Experi-

menters who build their first phasing rigs are often amazed at how much different an LO phase shift pair works when connected to mixers than when it is observed with 50-Ω loads on an oscilloscope. It is common for the phase adjustment range to be too small, and additional capacitors often need to be tacked on the bottom of the circuit board at one mixer LO port or the other. In many applications, the phasing receiver or exciter only needs to operate at a single frequency or over a very narrow band—for example, when following a



Minimum Component Receiver Front-End

Design Equations

$$C_1, C_2 = 100\Omega \text{ Capacitive Reactance } C_1, C_2 = \frac{1}{100\omega}$$

$$C_3 = 35 \Omega \text{ Capacitive Reactance } C_3 = \frac{1}{35\omega}$$

$$C_4, C_5 = 70 \Omega \text{ Capacitive Reactance } C_4, C_5 = \frac{1}{70\omega}$$

$$T_1 = 50 \Omega \text{ Inductive Reactance } T_1 = \frac{50}{\omega}$$

$$L_1, L_2 = 70 \Omega \text{ Inductive Reactance } L_1, L_2 = \frac{70}{\omega}$$

where $\omega = 2\pi F_0$ F_0 = Design Center Frequency

Notes: Wind T1 with a pair of enamelled wires side-by-side. The # turns for T1 is the number of times the pair is wound through the center of the core. The same core type is used for T1, L1 and L2.

Capacitors C1 and C2 are the nearest lower standard value, to help compensate for the capacitance between the windings of T1. Other capacitors are the nearest standard value.

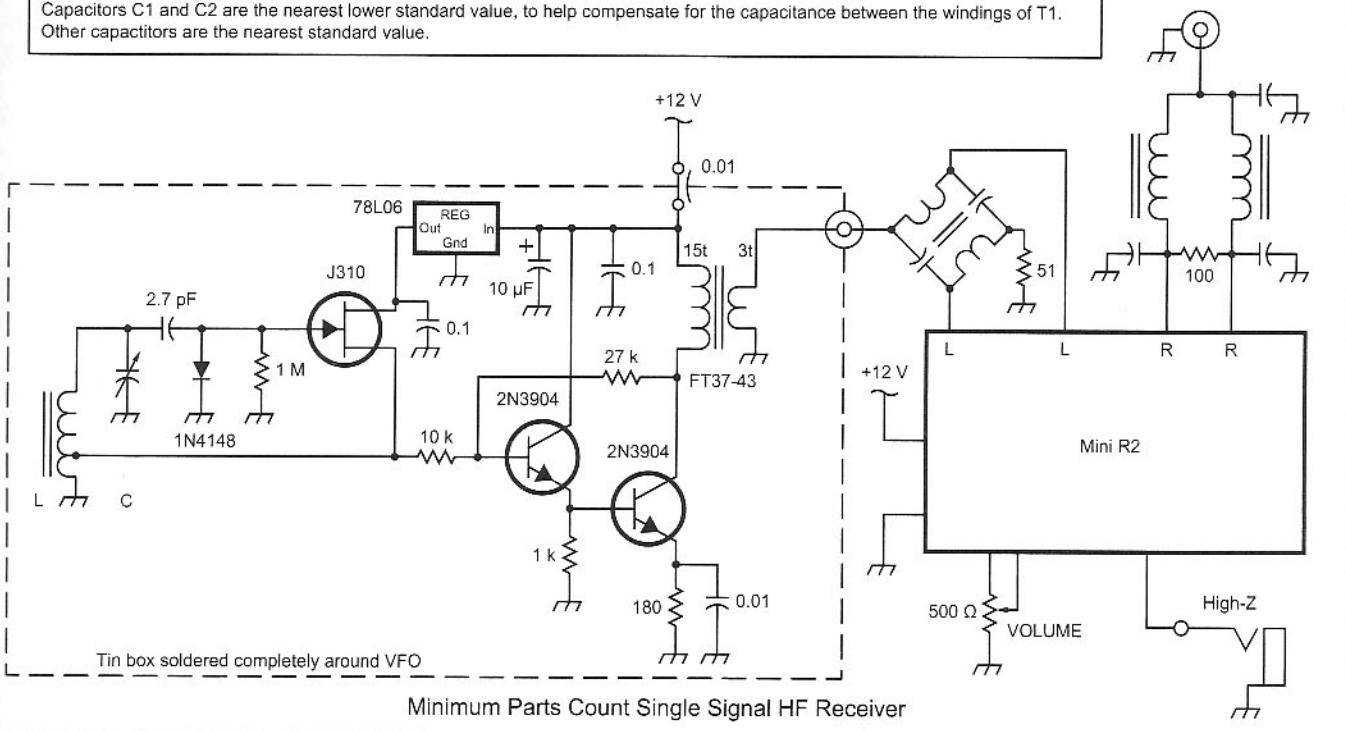


Fig 9.38—A good combination of LO quadrature network and RF splitter for HF and low VHF single-band receivers and exciters.

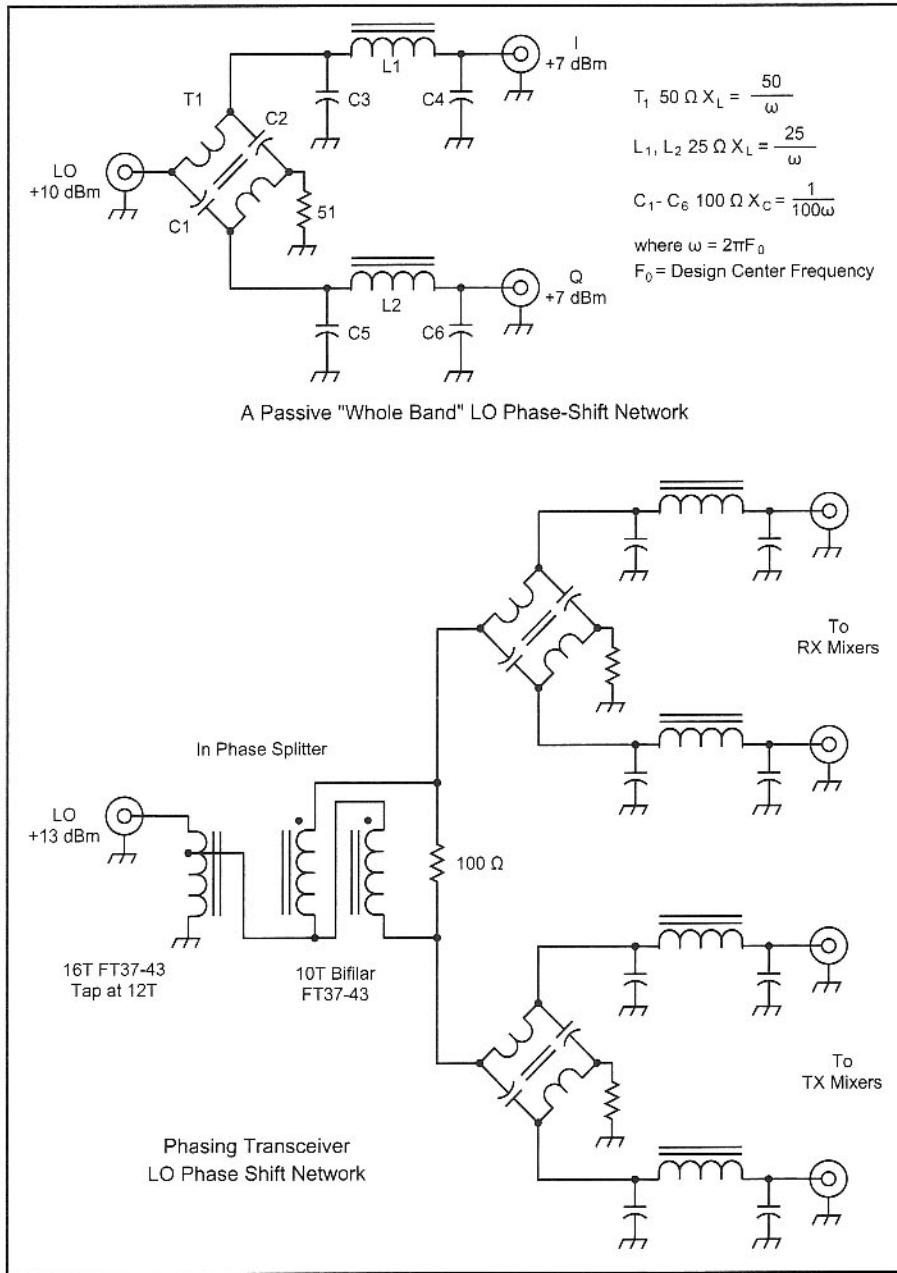


Fig 9.39—The LO quadrature network has wideband phase balance and acceptable amplitude balance over any amateur band, and the combined low-pass filter-splitter for RF provides a natural and well-behaved phase adjustment point. Here we move the phase adjustment to the LO path.

crystal filter or when used with a VXO as a tunable IF for microwaves. In this case the benefits of connecting the quadrature network to the RF ports instead of the LO mixer ports and using in-phase LO splitting may outweigh the bandwidth penalty.

A good combination of LO quadrature network and RF splitter for HF and low VHF single-band receivers and excitors is shown in **Fig 9.38**. The LO quadrature network has wideband phase balance and acceptable amplitude balance over any amateur band, and the combined low-pass filter-splitter for RF provides a natural and well-behaved phase adjustment point. **Fig 9.39** moves the phase adjustment to the LO path. This arrangement has been used extensively in amateur phasing excitors and receivers, and is attractive for band switched applications.

The bifilar toroid quadrature hybrid described in the reference by Fisher may be converted to a broadband structure by connecting a second network through a pair of transmission lines. The transmission lines are usually lumped element equivalents at frequencies below 50 MHz. The network shown in **Fig 9.40** is used in a receiver that covers 6.8 to 11 MHz without band switching. Front panel phase and amplitude trimmers are appropriate in such a receiver.

At VHF, a pair of transmission lines may be used, either with an in-phase splitter or just soldered together. It will be necessary to trim the length for maximum opposite sideband suppression. This is a tedious process, more so if connectors have to be unsoldered and resoldered every time the line length is trimmed. If anything in the system changes—any other transmission line length or the VSWR at any port—the line length will have to be readjusted. This brings up an interesting point: it is generally not appropriate to use modular construction and connectors between the

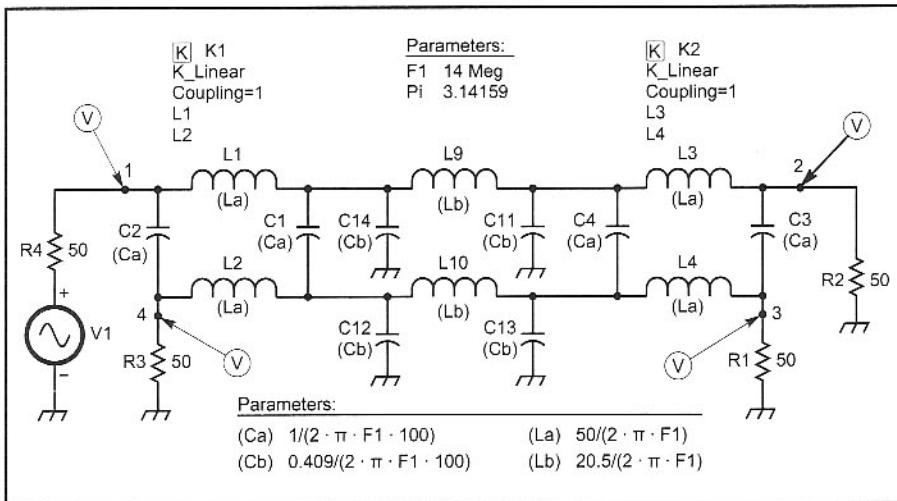


Fig 9.40—The bifilar toroid quadrature hybrid described by Fisher may be converted to a broadband structure by connecting a second network through a pair of transmission lines. The transmission lines are usually lumped element equivalents at frequencies below 50 MHz. This network is used in a receiver that covers 6.8 to 11 MHz without band switching.

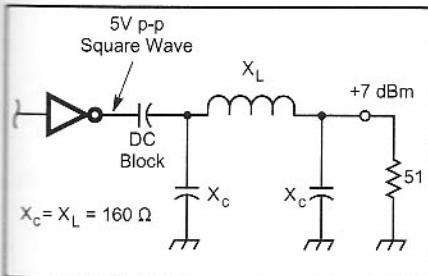


Fig 9.41—CMOS logic with a 5 V supply can drive +7 dBm into diode mixers using this circuit. The pi network converts the high-impedance IC square wave output into a sine wave and transforms the impedance down to drive a 50- Ω load.

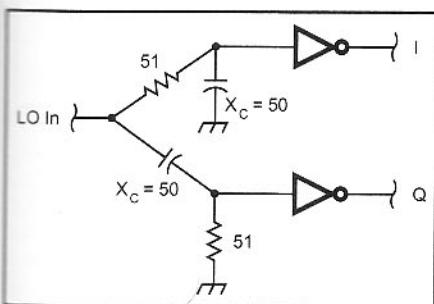


Fig 9.42—A simple logic LO phase-shift network.

stages of a phasing rig. It is much better to adjust it once, solder everything in place, and then leave it alone. If the rig has cables with connectors, they will eventually be needed for other projects and borrowed. Then new cables will have to be made up to get the phasing rig running again, and at 2 meters a few tenths of an inch makes a difference. Three of the most reliable rigs at KK7B use phase shift networks that were adjusted by squeezing turns on a toroid, and then the turns were locked in place with nail polish. All three still provide more than 40 dB of opposite sideband suppression after years of portable operation and world travel.

Digital ICs configured as frequency dividers can provide accurate 90° phase shift, and have often appeared in print. They have been used less often, partly because logic levels are not the appropriate drive for any of the more common mixers used in receivers and excitors, and partly because many more people have written about phasing rigs than have actually designed and built them. There may be parts of the brain that, once used to grasp fundamental digital concepts, are no longer capable of understanding basic RF. If so then the reverse is also probably true. Experiments with logic phase shift networks and commutating mixers are highly

encouraged. CMOS logic with a 5 V supply can drive +7 dBm into diode mixers using the circuit in **Fig 9.41**. The pi network converts the high-impedance IC square wave output into a sine wave and transforms the impedance down to drive the 50- Ω load. The pi network output capacitor is a convenient point to trim the phase. A simple logic LO phase-shift network is shown in **Fig 9.42**. Instead of a frequency divider to obtain the 90° output pair, an RC network is used. The inverters following the RC network act as hard limiters, and the networks on the output provide +7 dBm into 50 Ω and a convenient phase trim.

Some DDS ICs provide I and Q outputs. These may be used with a broadband RF splitter and switched RF low-pass filters to build simple general coverage phasing rigs, and experiments along these lines are encouraged. For wideband rigs, it is convenient to do both the amplitude and phase trimming at baseband, using the op-amp circuitry shown earlier. The phase noise performance of wide range DDS based Local Oscillators

is often not in the “high-performance receiver” category, and the miniR2 circuit provides more than enough signal processing performance. The extra design and construction time and expense to use the R2 and R2pro circuitry is wasted if receiver system performance is limited by the LO.

Digital LO generation, and LO buffer amplifier distortion generate LO signals that may be very rich in harmonics. Harmonics are important in phasing systems, because a phase shift in a harmonic will shift the phase of the composite waveform. Even if the I Q LO provides a perfect pair of sine waves, harmonics are generated in the mixer. A conservative approach to control of harmonic phase is to drive the mixer LO ports with wideband buffer amplifiers and resistive attenuators. For most applications, a more practical approach is to have a wide range available on the phase trim adjustment to compensate for harmonic phase effects.

If the phase trim adjustment does not have enough range, a common technique is to tack a small value (start with a few pF) capacitor from one mixer LO port to ground. If the opposite sideband suppression improves, leave the chip capacitor in place and readjust. If opposite sideband suppression degrades, move the capacitor to the other mixer. Add enough capacitance that the phase trim adjustment range permits the opposite sideband suppression to be nulled. It may be necessary to add a surprisingly large value capacitor before the phase is equalized. 100 pF will shift a 40-meter signal in a 50- Ω system about 10 degrees.

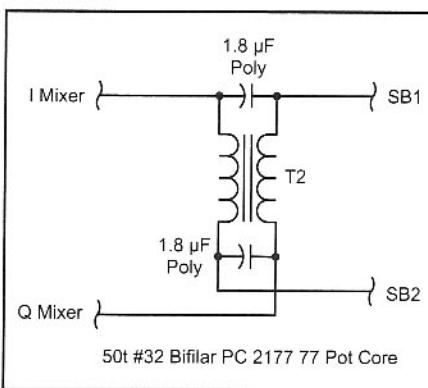


Fig 9.43—This simple quadrature hybrid circuit has good performance at only one audio frequency, but it is truly elegant in its simplicity and provides trivial sideband switching, draws no current, and offers the possibility of binaural independent sideband listening.

Audio Phase Shift Networks

A collection of audio phase-shift networks is shown in the next set of figures. The simple quadrature hybrid circuit in **Fig 9.43** has good performance at only one

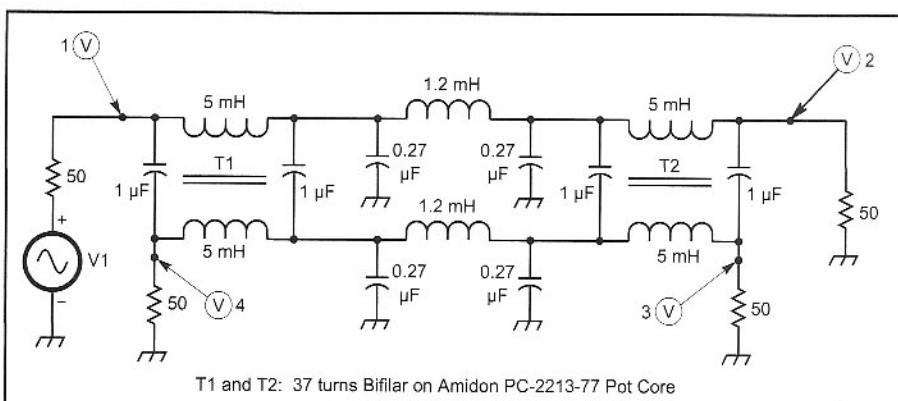


Fig 9.44—A broadband version of the circuit in Fig 9.43 provides marginal performance over a wider bandwidth, but good performance nowhere.

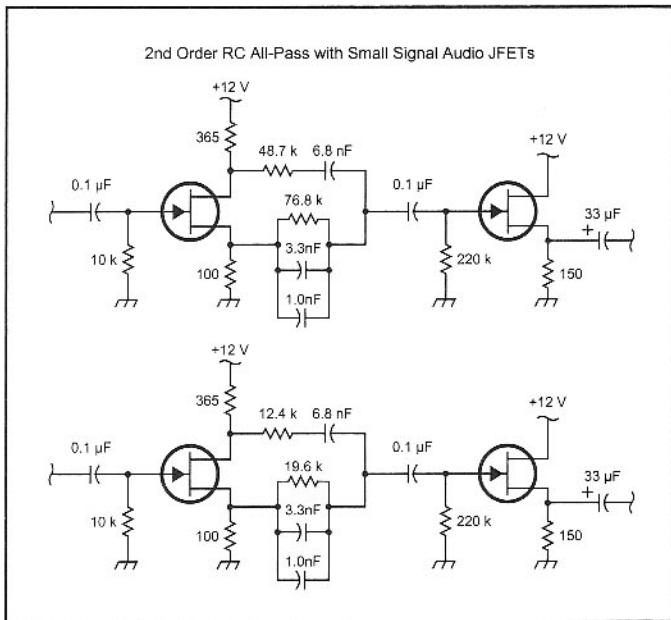


Fig 9.45—FET drive and load circuits for using classic second-order RC networks in excitors and receivers.

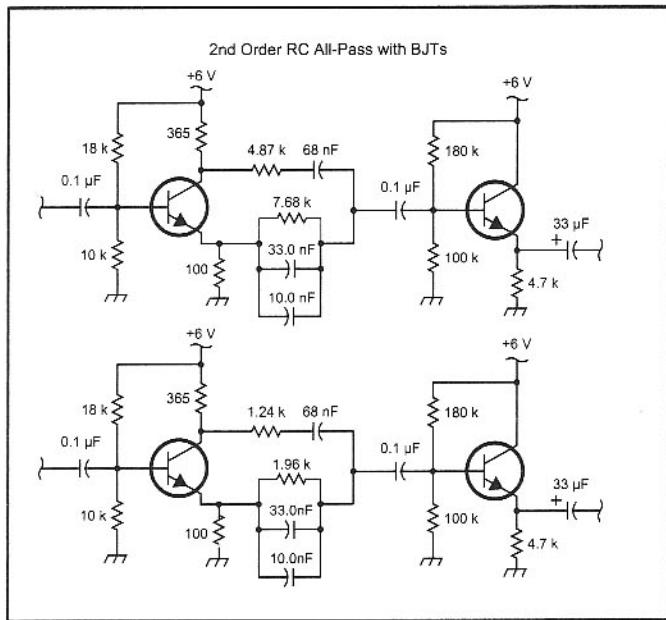


Fig 9.46—BJT drive and load circuits for using classic second-order RC networks in excitors and receivers.

audio frequency, but it is truly elegant in its simplicity and provides trivial sideband switching, draws no current, and offers the possibility of binaural independent sideband listening. It offers a real performance improvement over the simplest DSB direct conversion and regenerative receivers. The broadband version in Fig 9.44 provides marginal performance over a wider bandwidth, but good performance nowhere. One difficulty with passive LC audio quadrature hybrid networks using pot-core inductors is maintaining inductor tolerances. The inductance can vary over a wide range depending on the tightness of screw holding the pot core halves together, and a mechanical jolt can result in a big inductance shift.

Second-order RC audio phase-shift networks were used in the classic homebrew and commercial rigs of the '50s. They are

capable of good performance in both exciter and receiver applications, but will not provide the same level of performance as the common third-order op-amp networks or polyphase RC networks. Since networks with better performance are no more difficult to build, there is no obvious technical reason to use the classic circuitry in a rig with modern parts. There is, however, an appeal to simple circuitry, and even the solid-state circuits of the '60s are now old enough to be included in the classic category. A complete phasing transmitter using point-to-point wiring and only two and three terminal devices (no ICs) could be part of a '60s vintage homebrew station, and more importantly, could sound exceptionally good on the air. It is critical to remember that the drive and load impedances, and the relative drive levels, are part of the network. Figs 9.45 and 9.46 show several different drive and load circuits for using classic second-order RC networks in excitors and receivers. Components are standard 1% resistors and matched capacitors.

Fig 9.47 is a single stage op-amp all-pass network. This is such a common circuit in phasing rigs that it is useful to examine its behavior. At DC, C1 is an open circuit. The gain from Vi through the non-inverting input is +2. The gain from Vi through the inverting input is -1. These two add together for a net gain of +1 at DC. At high frequency, C1 effectively shorts the inverting input to ground. Then

the gain from Vi through the non-inverting input is 0, and the gain from Vi through the inverting input is still -1. The sum is -1. The frequency f_o occurs when $XC_1 = R_1$. The voltage at the non-inverting input at f_o is $0.5(1-j)$. The gain from Vi through the non-inverting input at f_o is $1-j$. The sum of the outputs from Vi through the inverting and non-inverting inputs is $-1 + (1-j) = -j$. Thus, the all-pass op-amp circuit has unity gain all the way from dc to high frequencies, and a phase shift of -90° at f_o . A phasing rig with just one op-amp all-pass network could have perfect opposite sideband suppression at one frequency f_o . By adding a second all-pass network in the other channel with a different frequency f_o , a phase difference of approximately 90° can be maintained over a small bandwidth. This might be useful for a simple CW receiver or a SSB transmitter with very relaxed (20 dB) opposite sideband suppression requirements. Fig 9.48 is a pair of all-pass networks with the 90° frequencies chosen for good suppression over an audio band from 470 to 900 Hz, and Fig 9.49 is a pair that provides at least 21 dB suppression from 360 Hz to 2050 Hz. Figs 9.50 and 9.51 show the phase errors from 0 to 4 kHz. The errors may be reduced by adding more sections and recalculating the all-pass network frequencies. Adding a second pair of op-amps allows us to achieve better opposite sideband suppression performance over wider bandwidths. Fig 9.52 illustrates a

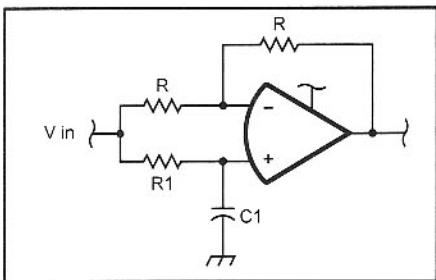


Fig 9.47—A single-stage op-amp all-pass network.

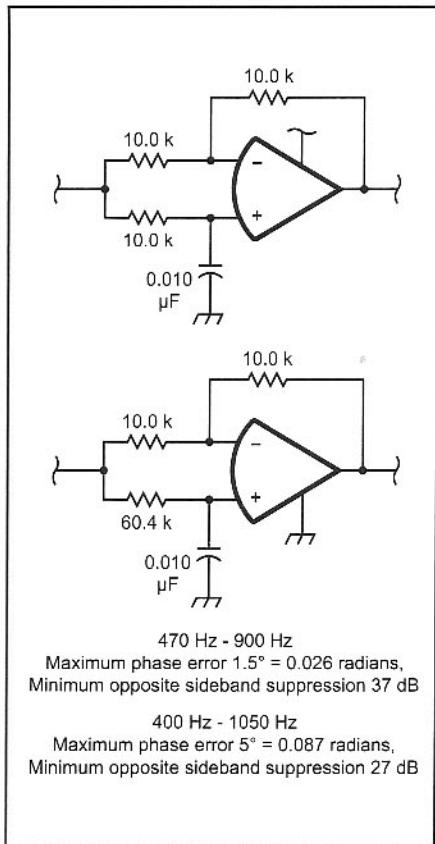


Fig 9.48—A pair of all-pass networks with the 90° frequencies chosen for good suppression over an audio band from 470 to 900 Hz.

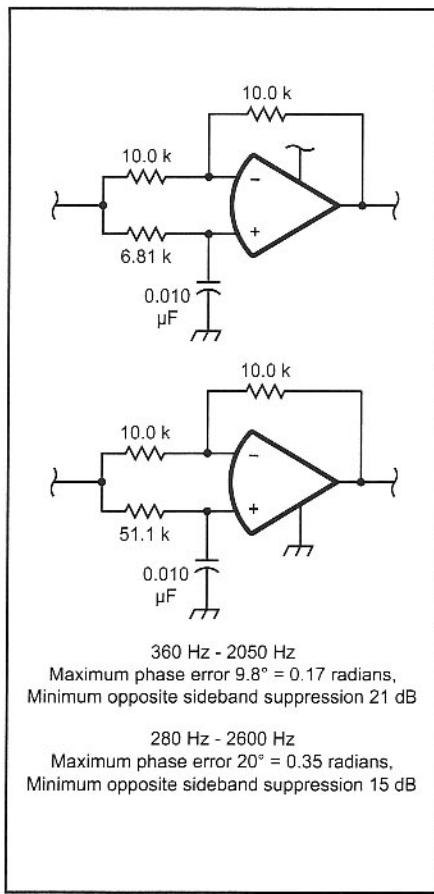


Fig 9.50—A pair of all-pass networks that provide at least 21 dB suppression from 360 to 2050 Hz.

second-order all-pass network pair for CW receivers that provides more than 50 dB of opposite sideband suppression from 300 Hz to 1120 Hz, and **Fig 9.54** is one that provides more than 36 dB of opposite sideband suppression from 250 Hz to 3650

Hz for SSB operation. **Figures 9.53 and 9.55** show the phase errors for these two networks.

Adding a third pair of op-amps allows us to build a network with small enough amplitude and phase errors that we could

achieve almost 60 dB of sideband suppression from 270 Hz through 3600 Hz, if the rest of the receiver were perfect. With this network, other receiver considerations will set the practical limit for sideband suppression. For most applications, the third-order all-pass network pair shown in Fig 9.56 is recommended. **Fig 9.57** shows the phase errors. Op-amps, resistors and capacitors are inexpensive, and this network has been widely duplicated. Note that one resistor value, $1.52\text{ k}\Omega$, is not a standard 1% component. A $1.50\text{-k}\Omega$ and a $20\text{-}\Omega$ resistor in series will stand side-by-side on the PC board.

Phase Shift Network Component Tolerances

With 1% tolerance resistors and capacitors right out of the bag, the network in Fig 9.56 will reliably provide more than 40 dB opposite sideband suppression. **Fig 9.58** is a simulation of the phase error when components values vary by 1% or less. Selecting the resistors and capacitors by hand using an accurate ohm and farad meter will improve performance. **Fig 9.59** is a simulation with 0.5% errors, and **Fig 9.60** is a simulation with 0.2% errors. More precise matching beyond 0.1% does not provide any practical benefit with 3rd order networks, because the design errors in the network are then larger than the component tolerance errors, as shown in **Fig 9.61**. Note that the capacitors and 10.0 k resistors all have the same value, and may be matched to each other, rather than an absolute standard. 1% resistors are cheap—it may be easiest to just measure a bunch of the 6 values needed and select those that are closest to the design value.

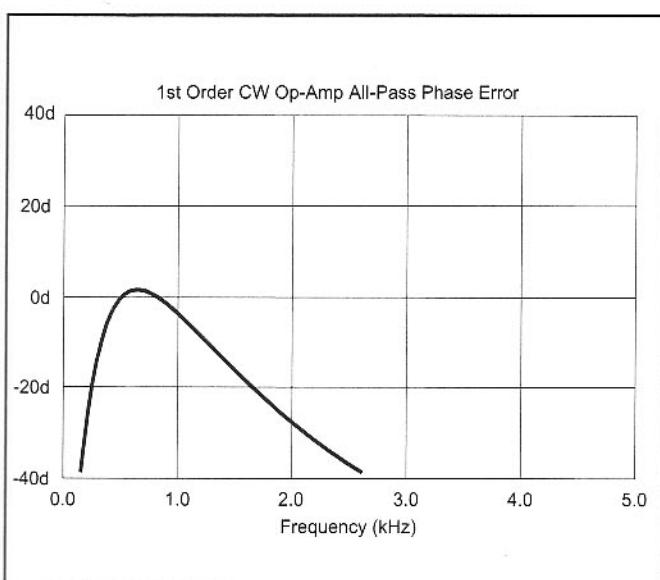


Fig 9.49—Phase errors of the Fig 9.48 network pair.



Fig 9.51—Phase errors from 0 to 4 kHz. The errors may be reduced by adding more sections and recalculating the all-pass network frequencies.

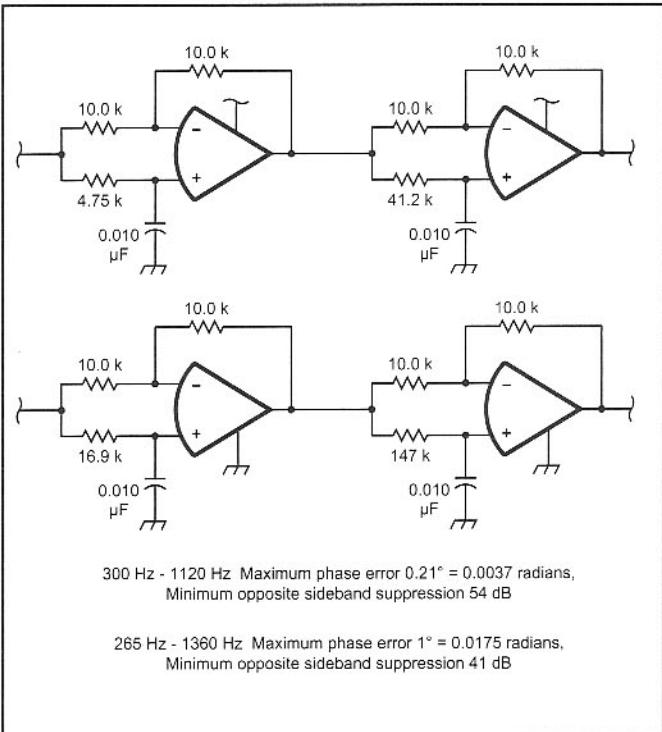


Fig 9.52—A second-order all-pass network pair for CW receivers that provides more than 50 dB of opposite sideband suppression from 300 Hz to 1120 Hz.

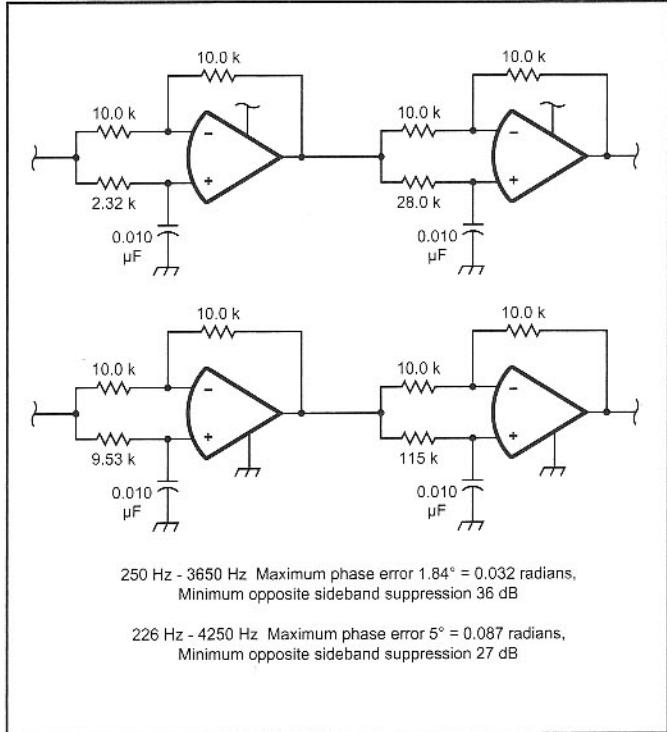


Fig 9.54—This second-order all-pass network provides more than 36 dB of opposite sideband suppression from 250 Hz to 3650 Hz for SSB operation.

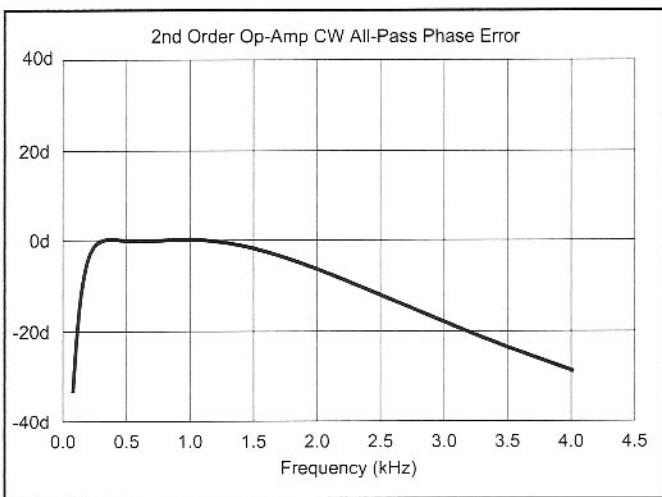


Fig 9.53—Phase errors in the second-order all-pass network shown in Fig 9.52.

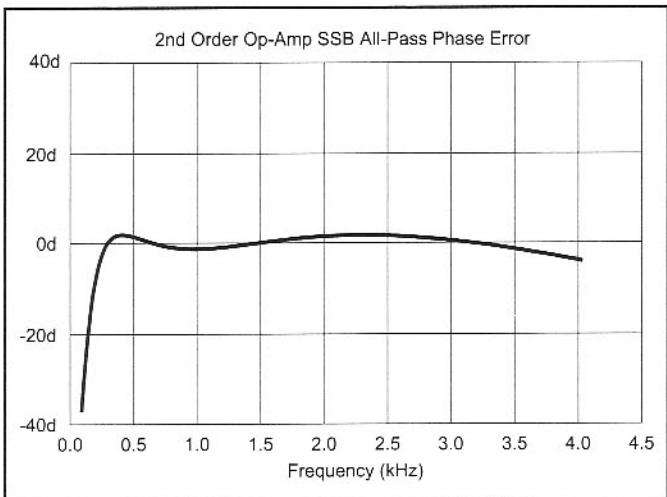


Fig 9.55—Phase errors in the second-order all-pass network shown in Fig 9.54.

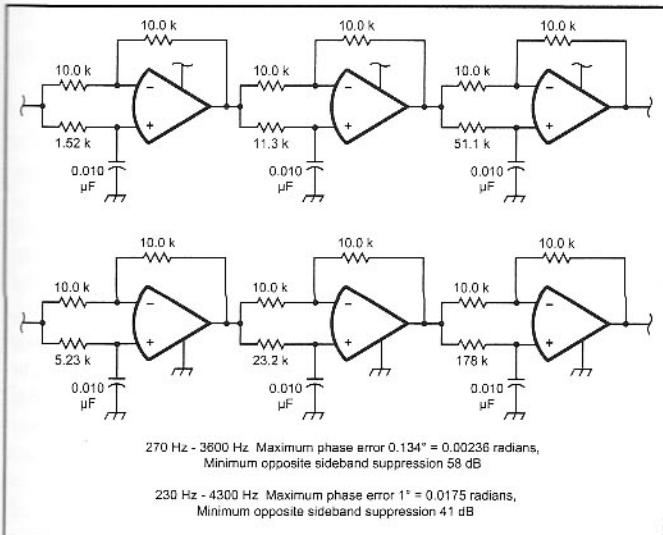


Fig 9.56—Adding a third pair of op-amps allows us to build a network with small enough amplitude and phase errors that we could achieve almost 60 dB of sideband suppression from 270 Hz through 3600 Hz, if the rest of the receiver were perfect.

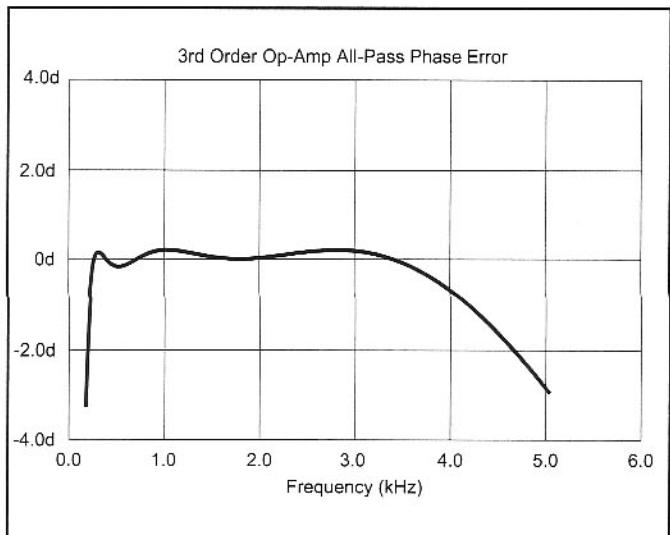


Fig 9.57—Phase errors in the network shown in Fig 9.56. Note the change in scale.

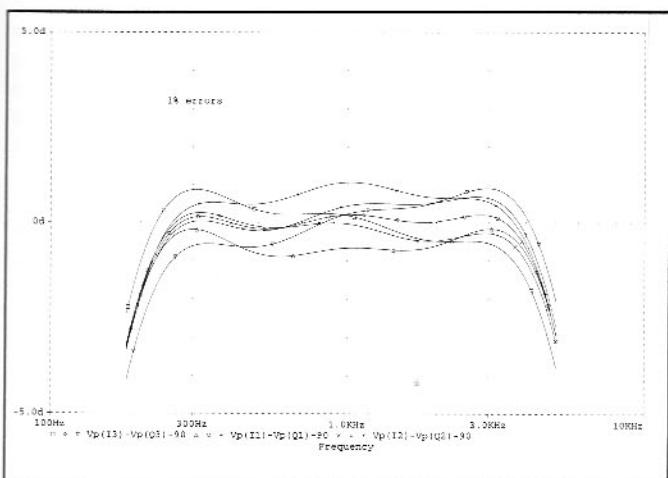


Fig 9.58—A simulation of the phase error when component values vary by 1% or less. Selecting the resistors and capacitors by hand using an accurate ohm and farad meter will improve performance.

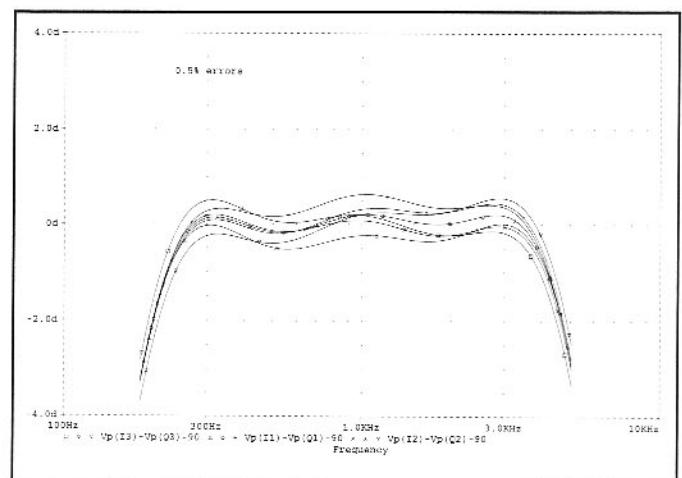


Fig 9.59—A simulation with 0.5% errors.

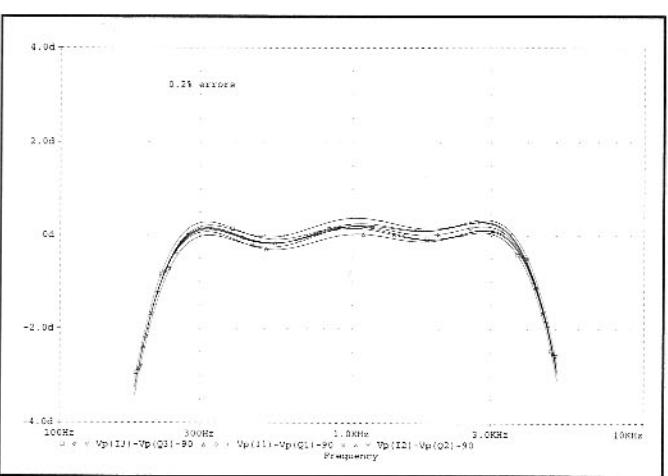


Fig 9.60—A simulation with 0.2% errors.

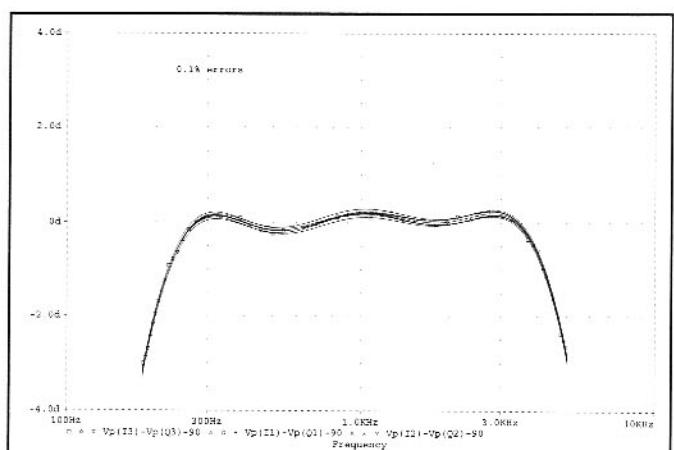


Fig 9.61—More precise matching beyond 0.1% does not provide any practical benefit with 3rd order networks, because the design errors in the network are then larger than the component tolerance errors.

9.7 OTHER OP-AMP TOPOLOGIES, POLYPHASE NETWORKS AND DSP PHASE SHIFTERS

Many other passive and active audio phase shift networks are possible, and have been described in the literature. The ones described above are ones that we have used and recommend. There are several other op-amp all-pass networks that have been used in phasing excitors and receivers. Many others are possible. Polyphase networks, described in the *ARRL Handbook*, may also be used in receiver and exciter applications. They are capable of excellent phase and amplitude balance across the passband. There are a few subtleties to consider in deciding between an op-amp all-pass network and a polyphase network. Polyphase networks are lossy, so more gain needs to be used ahead of them in receiver applications. The sideband cancellation actually occurs in the network, so no summing amplifier is needed afterward. This eliminates the possibility of trimming the summing amplifier for amplitude balance, requires that sideband selection be performed by reversing the LO drive to the mixers or inverting the output of one of the audio preamps, and requires duplicating the phase shift network for ISB applications.

Polyphase networks are 4 phase networks, and in I Q systems two of the phases are neglected. There are advantages to 4-phase receivers and excitors, however. Four-phase excitors have inherent carrier balance, as long as the four mixers are identical. This may be useful at VHF and microwaves, where it is difficult to obtain adequate carrier suppression with an I Q mixer pair. Polyphase network performance degrades rapidly outside the design passband, so it is useful to design the network for a significantly wider bandwidth than will actually be used. The biggest advantage of polyphase networks is that they are symmetrical, and therefore have self-correcting properties. Phase errors in the input section of the network are corrected by later sections. This allows reduced tolerance components to be used in part of the network. Good examples of rigs using polyphase networks are in the literature.

DSP may also be used to generate an I Q pair. This option is discussed in much more detail in the DSP chapters.

Some workers have included phase trim

resistors in the audio phase-shift networks of phasing rigs. This is discouraged for several reasons. First of all, it is unnecessary. A network that can support 50 dB of opposite sideband suppression can be built just by measuring the parts before construction. At this level, other errors in the system will begin to dominate. Secondly, all of the RC combinations in an op-amp all-pass network interact. The only reasonable method of tweaking the individual RC time constants involves a special phase-shift test procedure, and the adjustments might not be correct once the network is removed from the test fixture and inserted into a real receiver or exciter. Finally, it is possible to have too many adjustments. Imagine a car with a V-8 engine, and separate timing for the spark to each cylinder brought back to the dashboard and under control of the driver. Some things are better done correctly the first time, and then left alone. A notable exception to this is systems employing DSP. When the phase shift network is under software control, it is possible to optimize a large number of variables during a self-test routine.

9.8 INTELLIGENT SELECTIVITY

A final philosophical comment regarding the optimization of opposite sideband suppression is in order. The first 20 dB of opposite sideband suppression provides a real improvement in signal-to-noise level for SSB and CW signals, by removing the image noise contribution from the unused sideband. Once image noise is 20 dB down, it is hard to measure any further improvement in signal-to-noise ratio by suppressing it further. Additional opposite

sideband suppression is needed to suppress interfering signals in the unused sideband, which may be much stronger than the desired signal. In a receiver with "intelligent selectivity," the available resources can be optimized to suppress the interference, rather than to improve the opposite sideband suppression spec across the audio passband. This is significant, because the impulse response of a receiver with good selectivity in the tradi-

tional sense is significantly different than one with a wide response and a few deep nulls. Also, interference can take many forms, and it has long been recognized that optimizing the receiver to suppress nearby strong CW interference makes the receiver less robust to impulse type interference. Spending a few hours with a binaural IQ receiver is useful in understanding the implications of selectivity and interference rejection.

9.9 A NEXT-GENERATION R2 SINGLE-SIGNAL DIRECT CONVERSION RECEIVER

The R2pro is an image-reject direct conversion receiver subsystem consisting of several circuit boards. It is intended for applications where a performance improvement over the basic miniR2 circuit is desired, or for experimental applications where access to signals throughout the system is needed. For most applications, the miniR2 circuit provides excellent performance using off-the-shelf parts. The R2pro requires hand-matched components and careful measurements during construction. It is intended to be used with RF gain, and its design flexibility requires that some engineering decisions be made by the builder.

Review of Previous Work

The phasing receiver described in January 1993 *QST* was developed in parallel with the "High Performance Direct Conversion Receiver," described in the August 1992 issue. All of the basic circuitry from the straight DSB receiver was duplicated onto the phasing receiver circuit boards, with appropriate additions for eliminating the undesired sideband. The audio quality of the August 1992 DSB direct conversion receiver remains a benchmark for amateur receivers. The phasing version sounds good, but summing two channels with different time delays (as required by the image-reject circuitry) modifies the impulse response of the channel, and the receiver loses some of its presence. This is exactly the same effect one encounters with a SSB bandwidth crystal filter in a conventional superhet.

After several hundred R2 receivers had been built, the second-generation miniR2 circuit was developed. The miniR2 circuit board is half the size of the original R2, and has only headphone output. MiniR2 circuitry is simplified and has improved tolerance of component variations, so that good performance may be obtained without hand-matching the audio diplexer components. The audio filter component count was reduced to fit all of the parts on the small circuit board, but audio quality was not compromised. The miniR2 is suitable for use with headphones or an external audio power amplifier. The complete schematic for the miniR2 circuit board is in Fig 9.62. There is only one modification from the original *QST* article circuit—the 0.1 μ F capacitor in series with the inverting input to the summing amplifier. This capacitor elimi-

nates sensitivity to dc power supply voltage variations.

Many experimenters have used the basic R2 and miniR2 circuitry as the foundation for experiments using DDS frequency synthesizers and DSP audio signal processing, as suggested in the original *QST* articles. We have built a dozen different R2 and miniR2 receivers and transceivers for a wide variety of fixed and portable applications—often with outstanding results, and sometimes immediately indicating directions for further work.

After all this learning experience, it was natural to update the original high-performance phasing receiver circuit. A number of revised versions have been built—but the requirement that the new version work better than the original is tough. The original circuitry, and the circuit board layout, were optimized over a period of more than a year of continuous activity.

Updating the R2

The first task in updating the R2 circuit was to determine what needed to change. The following list was formulated:

- Replace the SBL-1 mixers with the TUF-3 package.
- Replace the LM 387 audio IC with a modern low-noise dual op-amp
- Revise the audio diplexers for better tolerance to component variation
- Improve opposite sideband suppression
- Improve receiver system noise figure
- Improve audio stability
- Make it easier to build advanced experimental receivers
- Design a receiver circuit that rewards component selection with performance
- Eliminate distortion from the muting circuit
- Improve LO reverse isolation

The new receiver was named the R2pro. The philosophy is that the R2pro trades more expensive construction, more expensive components, component matching, design flexibility, and a higher level of builder knowledge and experience for slightly improved performance over the miniR2. The miniR2 circuit is a better choice for most applications, particularly when small size or battery operation is desired. The R2pro is for designer-builders who want to go to the extra effort and expense required to push a receiver to the limits of the direct conversion architecture.

Multiple Circuit Boards

There is a significant problem with direct conversion receivers built on a single circuit board. *RF* grounding and shielding techniques are very different than the grounding and shielding techniques needed for high-gain *audio* amplifier circuitry. If the low-level *RF* signals, high-level *LO* signal, all the mixer conversion products, and high-gain *audio* amplifier are all on the same circuit board, there must be compromises in grounding and shielding. These compromises were handled on the R1, R2 and miniR2 boards by designing the ground traces such that the audio stages saw an approximate single-point-ground and the area around the mixers was an unbroken ground plane. Any of these single-board receivers can be made to oscillate by connecting the power-supply or speaker ground wire to the wrong point on the circuit board ground, even though all of the grounds are connected together. For a review of audio grounding techniques, see Horowitz and Hill, *The Art of Electronics*.

The conflicting requirement for an *RF* tight enclosure and a single-point *audio* ground makes it difficult to package single board direct conversion receivers. Early versions of the R1 and R2 direct conversion receivers pictured in *QST* were enclosed in soldered-up copper-clad PC board enclosures. Other packages, particularly those made of aluminum pieces held together with screws—are prone to intermittent *audio* oscillations and microphonics. Breaking up the receiver into separate functional blocks—each with its own circuit board—provides more grounding flexibility. Then the PC board with the mixers can be completely shielded, and the PC board with the *audio* output amplifier can have a single point ground. By optimizing the gain partitioning and packaging of the receiver, hum and microphonics can be eliminated and the placement of ground connections becomes much less critical. As a fringe benefit, breaking up the PC board makes it easier to build experimental versions using DSP, different mixers, *audio* processors and power amplifiers etc.

Block by Block R2pro Circuit Description

The R2pro block diagram is shown in Fig 9.63. Note that the R2pro system design includes an *RF* preamp, and that the *audio* output stage is a completely separate block.

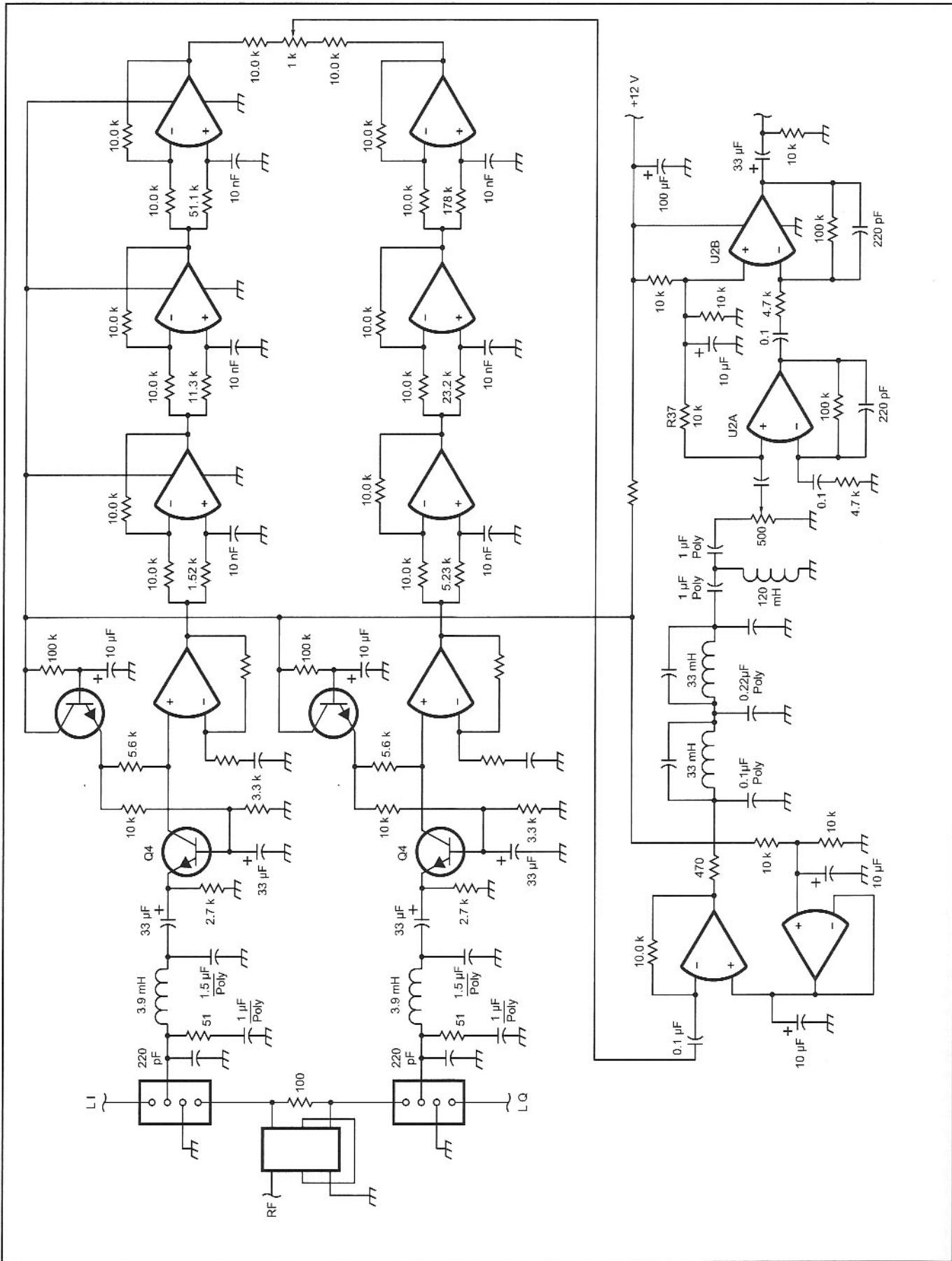


Fig 9.62—This simplified version of the mini R2 uses some different parts values and requires matching of the diplexer components.

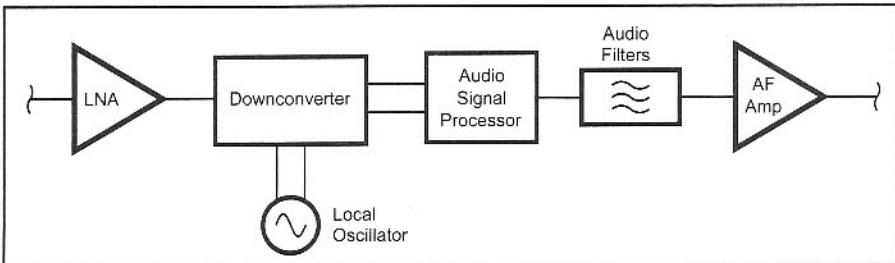


Fig 9.63—The R2pro block diagram.

RF PREAMP

The first block in the R2pro receiver subsystem is the RF preamp. The use of a preamp permits additional mixer loss in the design for improved dynamic range, improved phase and amplitude balance over the baseband frequency range, constant impedance at the downconverter RF port, and lower LO radiation from the receiver RF port. The basic design shown in Fig 9.64 is highly recommended, but any low-noise, moderate-gain 50- Ω bandpass amplifier with high reverse isolation (S12) may be used. Because direct conversion

receivers are sensitive to signals near the odd harmonics of the desired signal, it is necessary to provide significant attenuation to signals above the band of interest. This is particularly important in metropolitan areas with many FM broadcast signals. A separate RF-tight enclosure is appropriate.

The grounded gate circuit in Fig 9.64 was designed specifically to use in front of direct conversion receivers at MF through VHF. Low-pass filtering in the input and output match to the transistor provides the necessary attenuation of signals near odd

harmonics of the LO. The bias switch is part of the receiver mute circuit, and switches the amplifier gain between +13 dB and -40 dB. The grounded gate topology is a strong 40-dB attenuator when it is reverse biased, and can be switched in as a front-end attenuator when very strong signals are present, without introducing front-end distortion. It is common for direct conversion receivers to experience audible pops during full break-in CW operation. One source of these pops is the dc shift at the mixer IF port when the strong TX signal appears at the mixer RF port. One solution is to switch in a large attenuator between the antenna switch and mixer RF port. The “sleeping bag radio” described in Chapter 12 uses a similar preamp circuit in front of a miniR2 board, and has absolutely clean transmit/receive switching at all volume levels. Fig 9.65 shows the swept frequency response for several different bands. The typical input intercept of +13 dBm is a good match for receivers with standard level diode ring mixers.

The amplifier noise figure of approximately 4 dB and the relatively low gain of

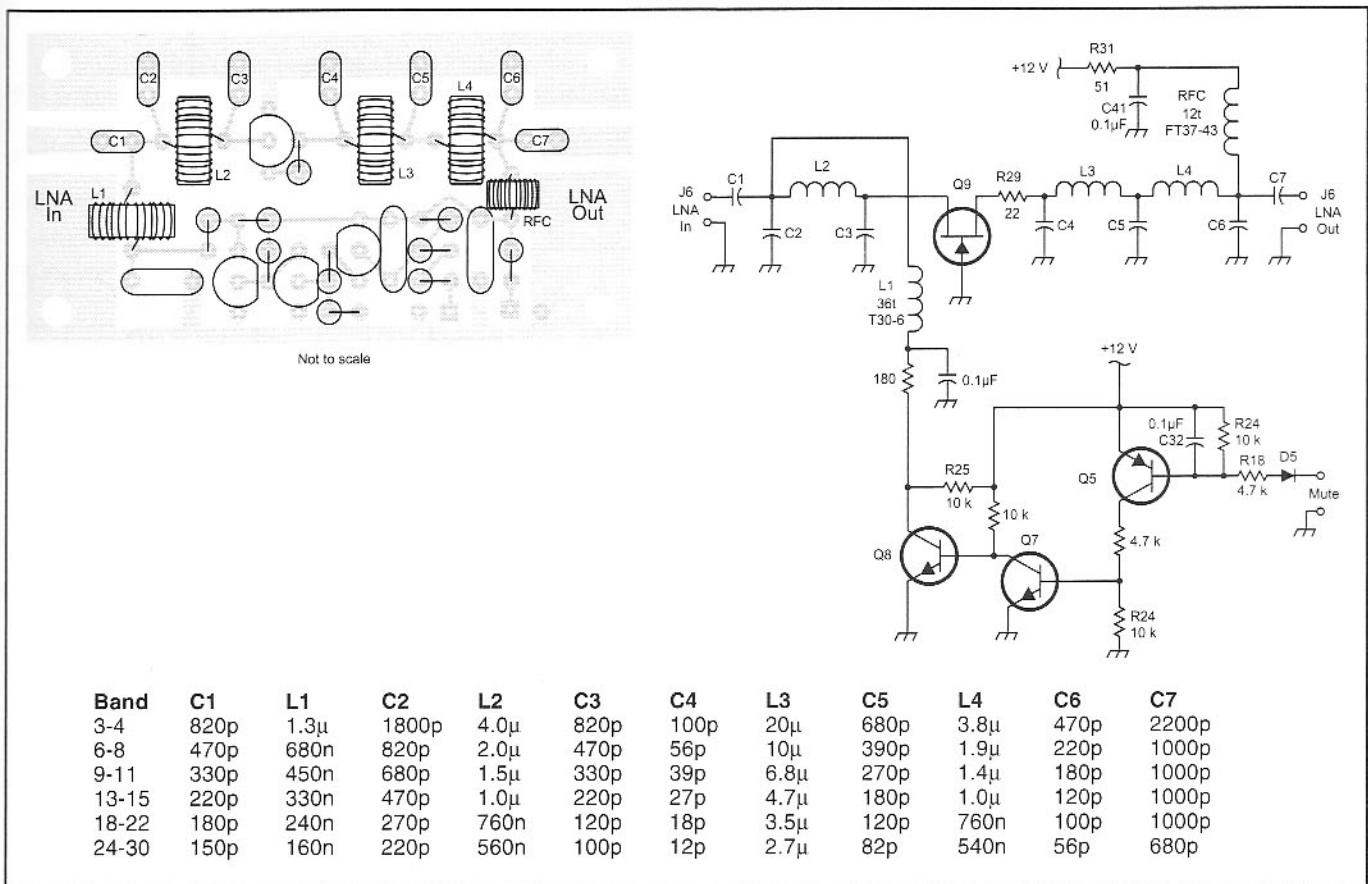


Fig 9.64—The use of a preamp permits additional mixer loss in the design for improved dynamic range, improved phase and amplitude balance over the baseband frequency range, constant impedance at the downconverter RF port, and lower LO radiation from the receiver RF port. The basic design shown here is highly recommended, but any low-noise, moderate-gain 50- Ω bandpass amplifier with high reverse isolation (S12) may be used.

the preamp stage have the effect of reducing the receiver noise figure without severely impacting two-tone third-order dynamic range. Third-order dynamic range near 100 dB is possible with standard level diode-ring mixers and a narrow CW bandwidth. High-level mixers permit better dynamic range numbers, if the LO system is quiet enough.

The direct conversion receivers described by the author in *QST* in 1992-1995 were all developed using a full-sized elevated 40-m dipole in a quiet lakeside location in the Upper Peninsula of Michigan. At this location, signals from all over the US and Canada were quite strong, and the antenna noise power was always high enough that a 15-dB noise figure was always adequate. There are other locations that can benefit from quieter receivers, even on 80 meters. In the mountains of the Pacific Northwest, band noise levels on 40 meters are commonly well below the

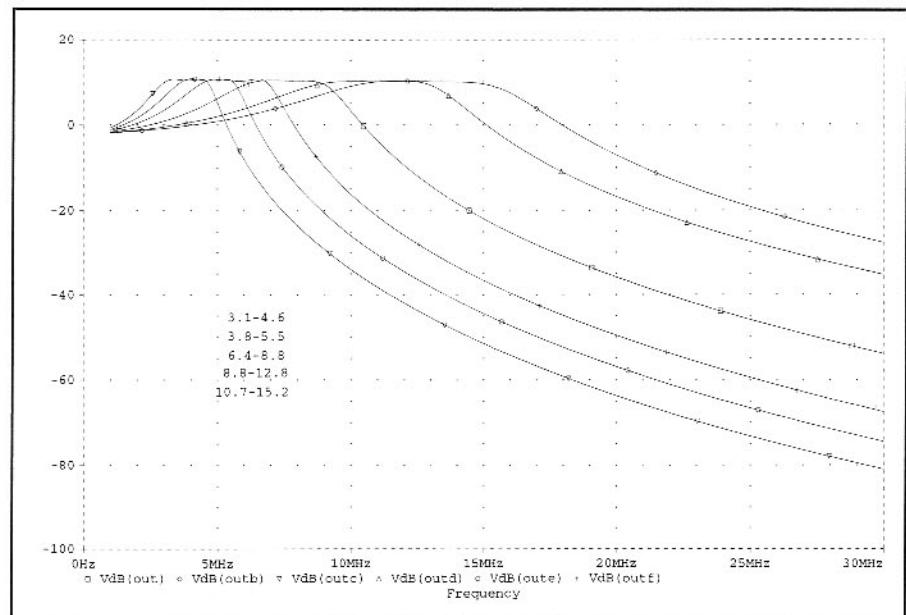


Fig 9.65—LNA swept frequency plot.

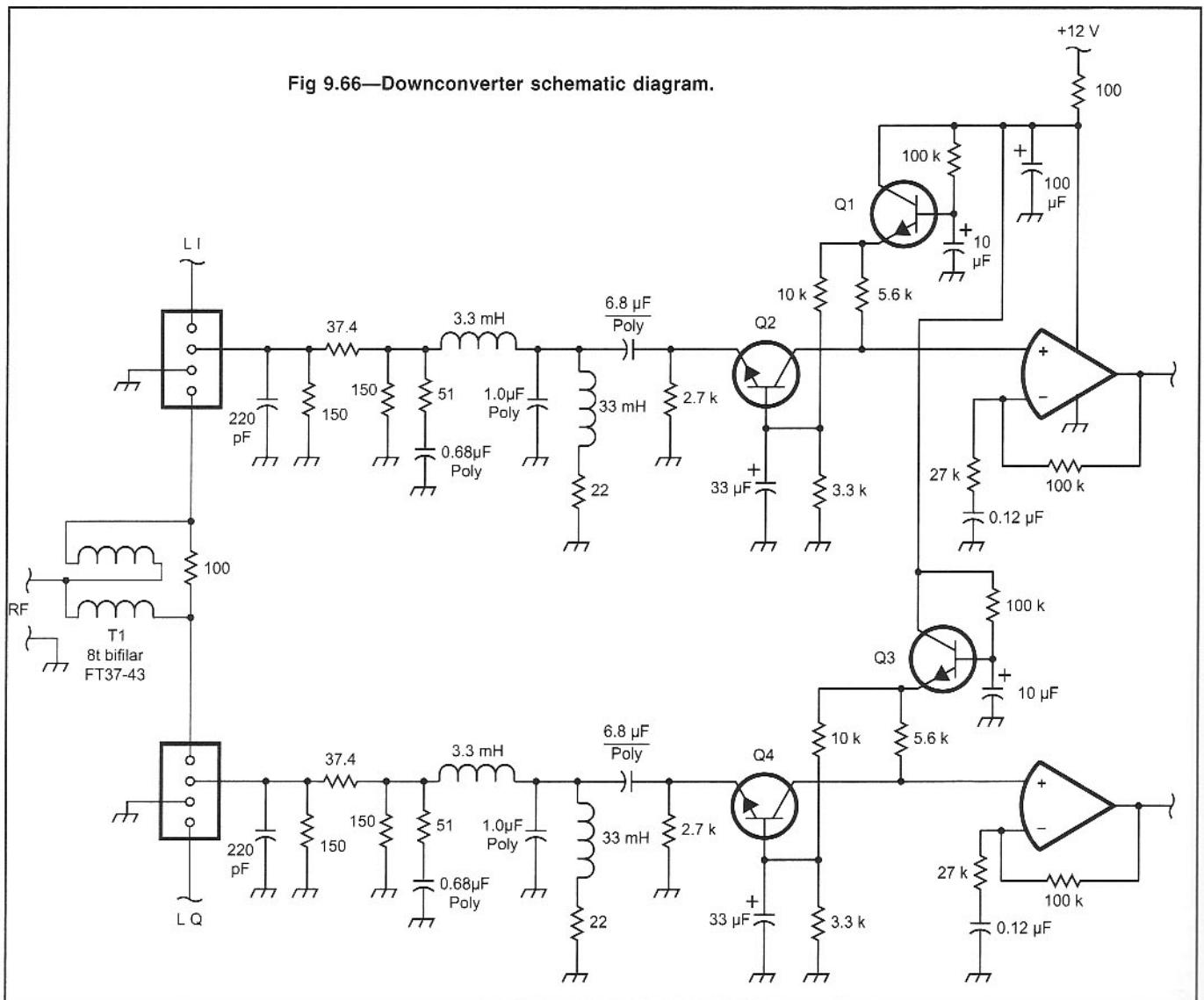


Fig 9.66—Downconverter schematic diagram.

accepted numbers in the amateur and professional literature. For mountain portable operation, receiver noise figures should be below 10 dB for all HF bands, and much better noise figures may be useful above 20 meters, particularly when using directive antennas.

For wide-band systems, a broadband impedance transformer can replace the tuned low-pass output on the RF preamp. This will permit coverage of multiple bands, but the low-pass function is still important and must be included somewhere in the receiver RF path. When a lower noise figure is desired, a two stage grounded-gate RF preamp is a good choice. Two of the Fig 9.64 circuits packaged separately with coax connectors is a high-performance construction option.

In summary, here are a few good reasons to include RF gain in any direct conversion receiver:

1. Improved Noise Figure.
2. Electronic front-end gain switching
3. Reverse isolation to eliminate LO radiation
4. Improved receiver gain distribution

For phasing direct conversion receivers there are additional advantages:

1. Providing mixer RF port impedance that doesn't change with antenna tuning
2. Option to use attenuators on all mixer ports

DOWNSAMPLER

After the preamplifier is the down-converter block, shown in Fig 9.66. (A layout and photo are shown in Figs 9.67 and 9.68.) The downconverter includes an RF in-phase splitter, two mixers, IF port attenuators, a matched pair of diplexer networks, and a matched pair of audio LNAs. All of the resistors in the downconverter

board should be 1% metal film. The input splitter is somewhat different than earlier versions. Rather than attempting to match to $50\ \Omega$, the splitter shown matches the mixer inputs to a lower impedance—but achieves nearly perfect amplitude balance and very low loss over a very wide frequency range. The upper frequency limit is reached when the winding on T1 approaches a quarter wavelength. At the lower frequency limit, amplitude balance is still perfect, but isolation is poor. If operation down to 50 kHz is desired, more turns on a type 71 core could be used. At 144 MHz and above, a few bifilar turns through a small ferrite bead work well. The mixers are type TUF-3, which offer better port-to-port isolation and lower conversion loss than TUF-1 mixers from 150 kHz through 225 MHz, the usual operating range of R2 type systems. TUF packaged mixers are available for direct conversion applications at frequencies up to 2500 MHz. The small sample of microwave diode mixers we have measured have higher 1/f noise than we have seen with TUF-1, TUF-3 and SBL-1 mixers. Microwave Doppler Radar systems use special low-1/f noise diodes.

After the mixers are a pair of matched attenuators. The 6 dB attenuators shown in the schematic should be used for most applications. If more gain is available before the mixers, more attenuation may be used. These attenuators serve three very useful purposes: they ensure textbook termination of the mixer IF ports; they attenuate mixer 1/f noise; and they provide a well defined source impedance to drive the matched diplexer networks. Mixer IF termination has been widely discussed in the literature. Mixer 1/f noise degrades receiver noise figure. Different mixers, even matched TUF-3s with the same date code, have widely varying amounts of 1/f noise. Attenuation between the mixer and the

audio preamp can't improve receiver noise figure, but it can reduce the effect of mixer 1/f noise. Advanced receiver artists are encouraged to study this. The R2pro circuit balances preamp gain and post-mixer attenuation to set the receiver noise figure and dynamic range, so that receiver performance is relatively independent of mixer 1/f noise.

The third very important function of the post-mixer attenuators is to set the driving point impedance to the matched diplexer networks. In the original R2, the diplexers are connected directly to the mixer IF port impedance, which varies with LO drive level. If one mixer has more LO drive than the other (a common condition) the phase and amplitude response of one diplexer network will be slightly different than the other. These differences are typically enough that the ultimate opposite sideband suppression of R2 systems across an SSB bandwidth is about 41 dB—even with perfect audio phase-shift networks. By contrast, the miniR2 with off-the-shelf components often exhibits nearly 50 dB of opposite sideband suppression.

The diplexer networks are slightly simplified from the original R2 networks. The R2 networks provided rapid roll off both above and below the 300 to 4000 Hz audio band. The roll off below the audio range does not contribute much to useable receiver dynamic range, but it does introduce rapid phase shifts in the critical 300 to 600 Hz frequency range. When R2 receivers are optimized for SSB operation, the suppression of the opposite sideband in the 300 to 600 Hz range is often right at the 40 dB spec. If the receiver is optimized for CW operation, sideband suppression usually falls off at higher audio frequencies. The miniR2 and R2pro eliminate the rapid roll off at the low end of the audio range, which permits good performance through the CW range when the receiver is optimized for SSB. Another change from the R2 and miniR2 circuits is the elimination of the electrolytic capacitors from the critical audio signal paths. The R2pro has only matched polypropylene capacitors in the audio path prior to the summing network.

The roll off above the audio range is retained from the R2, with slight changes to make the receiver less sensitive to component tolerance. For good performance, it is necessary to match the diplexer components in R2pro to within 1%, just as in the original R2. If this is not done, opposite sideband suppression is likely to be poor across the audio band. By contrast, the diplexers in the miniR2 were designed to be used with standard tolerance components. The benefit of using the R2pro

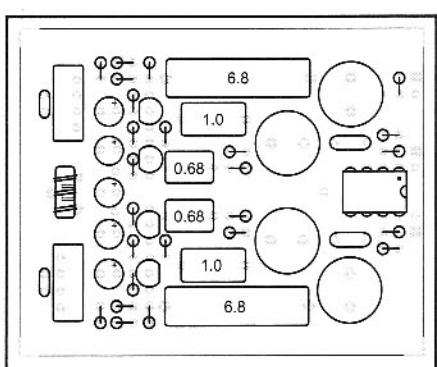


Fig 9.67—The downconverter board layout.

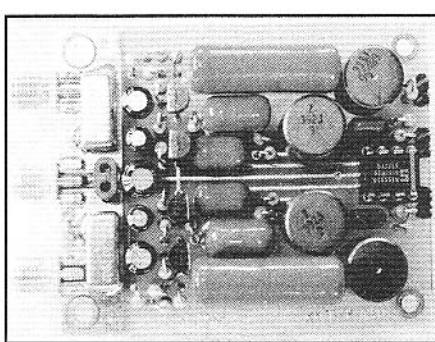


Fig 9.68—A view of the downconverter board.

diplexers with matched components is that the close-in dynamic range is good. R2pro two-tone measurements may be made at tone spacings of 10 kHz and 5 kHz.

The usual grounded-base audio preamp stages are used following the diplexer networks. There are other audio preamps that will work, but the grounded base stages have the advantage of having an input impedance that is set by the current through the transistors, which may be set up precisely using 1% resistors. The grounded base stages drive the non-inverting inputs of a low-noise dual op-amp, which provides low impedance drive to the following stages. Note that the outputs are not dc blocked. This is so that the low impedance drive from the dual op-amp can directly drive the audio phase-shift network. Because these outputs carry dc, there is the potential to short them and damage the dual op-amp. IC sockets are appropriate.

It is critical that everything in the I and Q channels of the downconverter block be well matched. In most cases, it is the I Q downconverter block, and not the audio phase-shift network, that sets the ultimate limitation on receiver opposite sideband suppression. The baseband LNA pair is nearly identical to the version used in the miniR2, with the exception that 1% resistors are used in all locations and transistor pairs Q1—Q3 and Q2—Q4 should be matched. This may be done by comparing the dc voltages on the I and Q outputs of the downconverter block using a digital voltmeter. First insert a temporary jumper between the emitter and collector holes for transistors Q2 and Q4. Then select a pair of devices for Q1 and Q3 that results in equal output voltages. The voltages should be matched to within 2%. Then solder in Q1 and Q3, remove the jumpers, and select a second pair of devices for Q2 and Q4 that results in equal dc voltages at the I and Q outputs. Since the gain and input impedance for these common base bipolar amplifiers are set by the quiescent currents, and the currents result in voltage drops across the 1% resistors, setting the dc voltages equal results in well-matched gain and input impedance for the baseband LNA pair.

The noise figure of the receiver is determined by the performance of the early stages. It is necessary to have enough gain in the early receiver stages to over-ride the noise of the later stages of the receiver. The analog signal processor block has a relatively high noise figure, resulting from the cascade of unity-gain op-amp phase

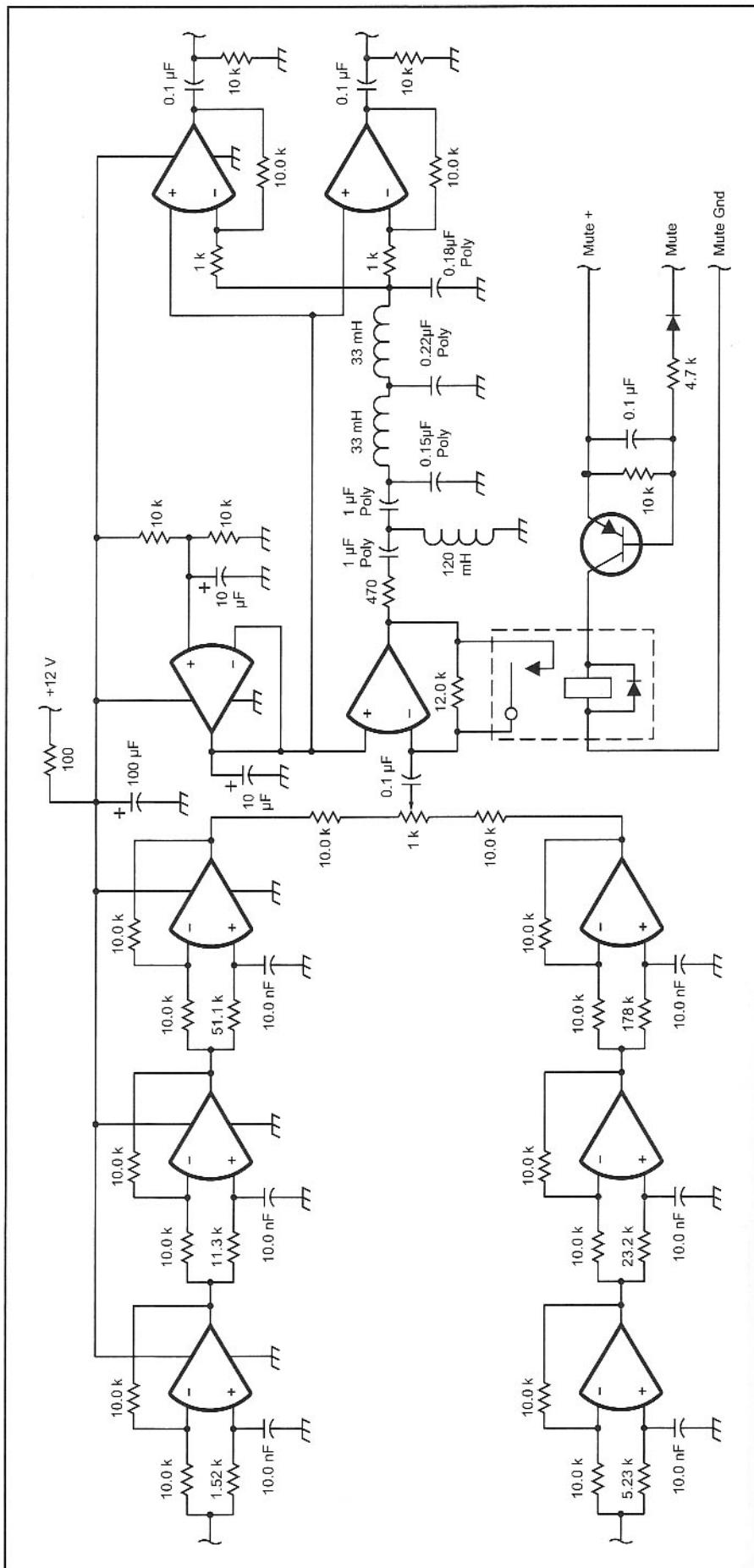


Fig 9.69—ASP schematic.

shift networks and the lossy bandpass filtering. The downconverter PC board gain is set by the ratio of the op-amp series and feedback resistors to a value that overrides the noise of the analog signal processor but that does not severely compromise in-band dynamic range. With the component values shown, the mixer loss is approximately 6 dB, there are 6-dB pads following each mixer, the bandpass diplexers have just under 2-dB loss, the grounded-base LNA stages have a noise figure of about 5 dB and approximately 40-dB gain, and the op-amp LNAs have 11-dB gain. Thus the total gain for the downconverter stage is about 37 dB and the noise figure at the downconverter RF input is approximately 19 dB. With all components matched to within 1%, the amplitude and phase errors in the I and Q outputs should be less than 0.1 degree and 0.02 dB across the baseband output range from 200 Hz to 4000 Hz.

Since the downconverter block contains both RF and low-noise audio signals, it must be constructed using good RF and audio practice. Audio signal levels are low and the gain is moderate so conventional RF grounding and shielding practices may be used for the downconverter block. With LO signals floating around on the same frequency as the desired input signal, shielding is very important. The circuit board is designed to fit inside a Hammond 1590B die-cast aluminum box. An enclosure soldered up from tin sheet or PC board scraps is even better. The RF and LO inputs should enter through coax connectors. Type BNC, SMA and RCA phono are all acceptable. The audio outputs should leave through either coax connectors or matched 1nF feedthrough capacitors. The audio

output signals include dc bias for the Op-Amps in the analog signal processor. For connection to the high impedance inputs of a DSP processor or oscilloscope, dc blocking capacitors may be used. The dc power supply lead should be connected using a feedthrough capacitor and external series resistor.

ANALOG SIGNAL PROCESSOR

The third block in the R2pro system is the analog signal processor (ASP) shown in Fig 9.69. (A board layout and photo is shown in Figs 9.70 and 9.71 respectively.) This board contains the audio phase-shift network, the summer, and a wideband passive audio filter. The audio gain is low, but the signal levels are also low, so this board should not be located where it can pick up power supply or computer noise. There are no RF signals present, so audio grounding rules apply. The single audio ground rail runs up the middle of the PC board between the ICs. The power supply line is decoupled by the $100\ \mu\text{F}$ capacitor and $100\ \Omega$ series resistor. Do not bypass the hot end of the $100\ \Omega$ resistor to ground. The dc bias to the non-inverting inputs to the analog signal processor comes from the previous stage.

There is only one change in the audio phase-shift network from the version used in the miniR2. $1.52\text{ k}\Omega$ is not a standard value in the 1% series. It is obtained by connecting a $1.50\text{-k}\Omega$ and $20\text{-}\Omega$ resistor in series. With the audio phase-shift network components (resistors and capacitors) selected to within 0.1% of their marked value, more than 60 dB of opposite sideband suppression could be obtained—if the rest of the receiver were perfect. By

selecting these components, the builder can be assured that the audio phase shift network is not limiting receiver performance. The image-reject mixer provides an attenuation band that covers the entire opposite sideband from 200 Hz to over 4000 Hz. This attenuation band is ideal for CW or SSB receivers, and provides very good selectivity when combined with audio channel filters.

Following the audio phase-shift network is a summing amplifier. The amplitude balance adjustment is conveniently located at the input to the summing amplifier. The summing amplifier drives a 250 Hz to 4000 Hz bandpass filter. This filter serves as a roofing filter, and provides optimum performance from optional external digital and analog filters that may be added to the output of the analog signal processor block. Roofing filter performance is good enough that it can serve as the only bandpass filtering in the receiver for high-fidelity listening. The output of the roofing filter drives a second gain block that provides an ideal filter termination for textbook bandpass response. The gain of the output gain block is set by the feedback resistor. With the values shown, the gain of the analog signal processor block is approximately 13 dB. It is possible to increase the gain of the output gain block to directly drive medium impedance headphones. The analog signal processor block also contains a mute circuit. Grounding the mute terminal drops the gain of the summing amplifier to zero. The mute circuit uses a reed relay with completely independent power, ground and control circuit. This permits the relay to be controlled by front panel switches and TR switching logic without corrupting the

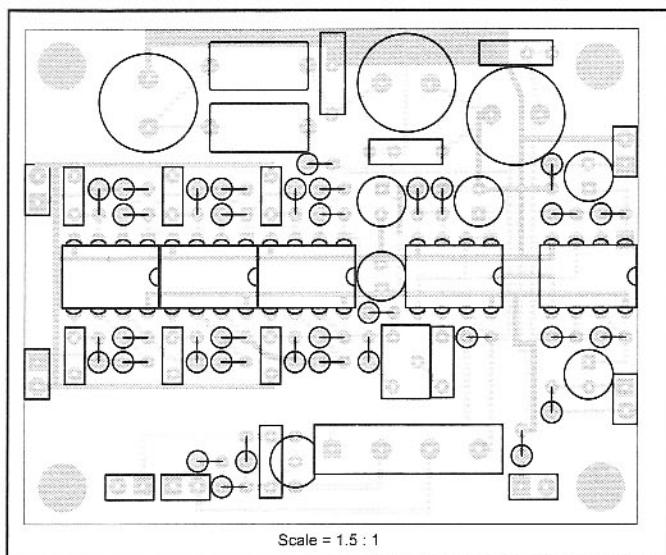


Fig 9.70—ASP layout.

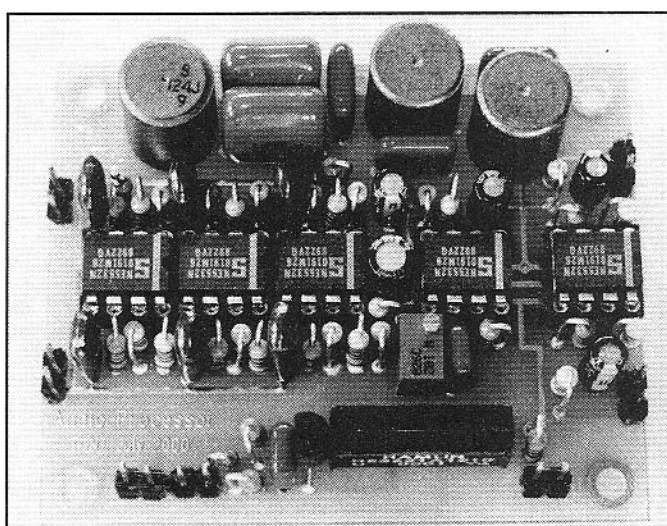


Fig 9.71—The analog signal processor.

Analog Signal Processor signal ground and power supply lines. Use of a relay also eliminates the low level distortion introduced by a FET switch. The sealed reed relay switching time of a few milliseconds is quick enough for full break-in operation on fast CW or digital modes.

The analog signal processor board has two isolated, independent outputs. The first output is normally connected through optional filters and the volume control to the audio output circuit board. The second output may be used to drive a signal level meter or audio derived gain control system. This is the ideal take-off point for DSP filters, FFT analyzers, home audio system stereo amplifiers, outboard audio filters or the computer sound card. Output levels may be independently selected by changing the output stage feedback resistors. The 1-k Ω input resistors should not be changed, as they provide the termination impedance for the roofing filter.

For construction hints on mounting and connecting to the ASP board, take the cover off a stereo receiver or amplifier and look at the circuitry around the magnetic phono cartridge inputs. Don't expect to find RF shielding, but a well defined single ground connection, shielded wire or twisted pair with the ground connected only at one end, and power connections directly to the big power supply capacitor

are common. This PC board should be mounted on nylon standoffs with a single wire to ground at the power supply.

OPTIONAL FILTERS

The low output impedance of the analog processor with a series 470- Ω resistor, and the 500- Ω volume control provide proper terminations for a wide variety of passive filters. Fig 9.72 is a pair of useful audio 500- Ω filters using standard value inductors and capacitors that have been used in a number of our radios. Also see the photo in Fig 9.73.

Signal levels are high enough at this point that open PC board construction is acceptable. If Wide SSB, Narrow SSB and CW options are all installed, it is useful to add attenuation to the SSB filters so that either gain or receiver output noise remain constant as filters are switched. 500- Ω attenuators are easy to construct. Use the resistor values from the *ARRL Handbook* tables, and multiply all resistor values by 10. For example, a 500- Ω 6-dB pi-network pad has a 390- Ω series resistor and 1.5-k Ω shunt resistors.

Signal channel selectivity is distributed through the baseband gain path. The bandpass diplexers pass a 300 Hz to 4000 Hz channel with smooth rolloff outside the passband to enhance phase-shift network performance and provide graceful impulse

response. The baseband LNA and gain block have wide bandwidth, to preserve amplitude and phase balance between the I and Q channels. After the summing amplifier, the 3rd order Butterworth High-Pass filter and 5th order Butterworth Low-Pass filter provide a flat passband with good impulse response at the medium frequencies. This roofing filter provides all the band-limiting needed for a high-fidelity SSB or CW receiver—and it is recommended that the receiver be put into operation with no additional filtering before adding narrow bandwidths. Some of the most skilled and avid CW operators are now using very wide bandwidth receivers when band conditions permit, because such receivers preserve the quality of

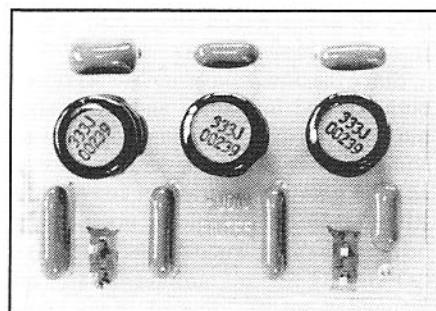


Fig 9.73—SSB and CW filters.

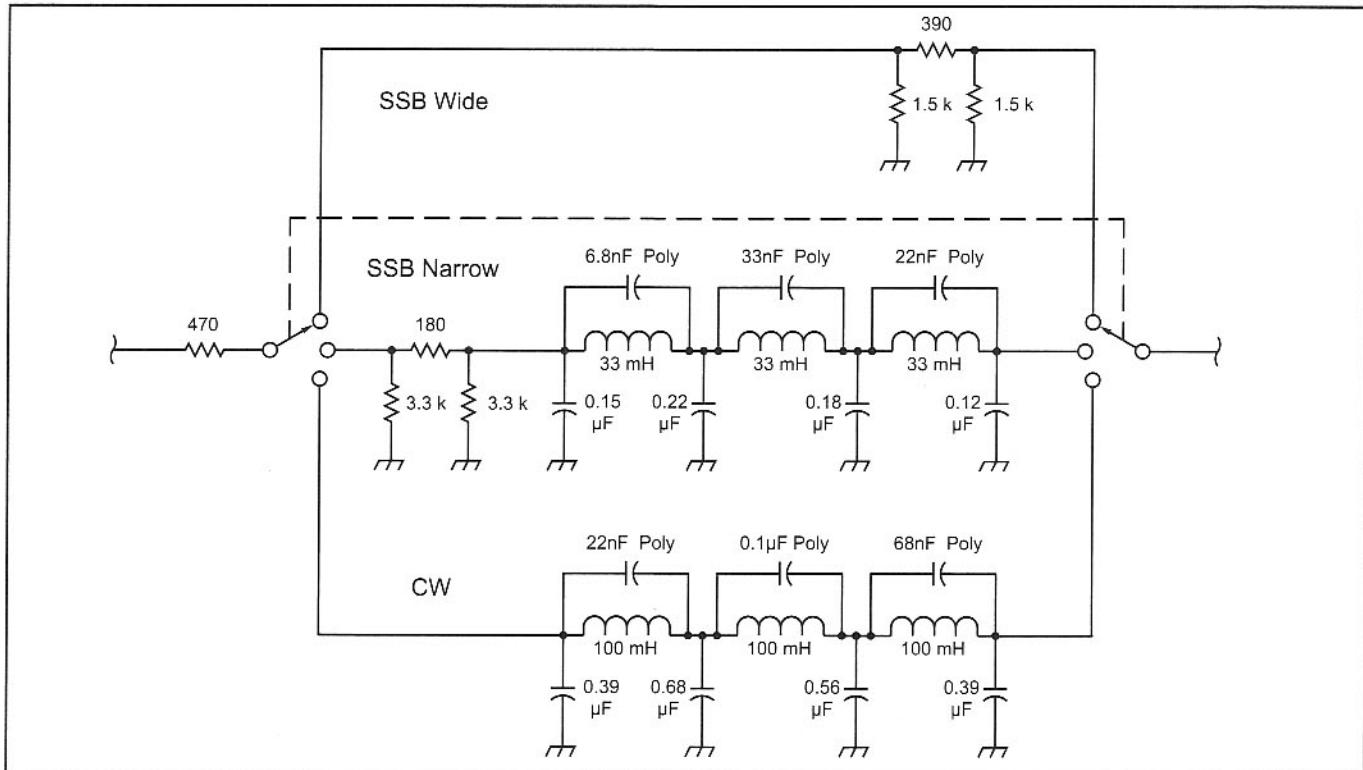


Fig 9.72—A pair of useful audio 500- Ω SSB and CW filters using standard value inductors and capacitors that have been used in a number of our radios.

transmitted signals and allow a much better perception of the texture of the band. Interestingly, low-audio-frequency impulse response is dominated by the effectively very steep skirts of the receiver response due to the high-pass filtering and the operation of the phase-shift image-reject circuitry.

Switched-capacitor and DSP filters may also be used at this point in the circuit. It is necessary to observe appropriate input signal levels, and bear in mind that the dynamic range and noise figure of the DSP may limit receiver performance. At the output of the analog processor, the receiver has an in-channel two-tone dynamic range of well over 60 dB and total harmonic distortion lower than 0.1%. By this point in the receiver, the noise floor, dynamic range and in-channel distortion have been set. DSP at this point can not improve these numbers—it can only provide wonderfully flexible filtering and additional whistles and bells. When the digital signal processing is carefully designed, it can add to the utility of the receiver without corrupting basic performance. If the DSP system has too few bits, if the A-to-D converters have a high noise figure, or if the signal levels are set up improperly so that the available DSP dynamic range is not used—a poor receiver with wonderfully flexible filtering will result. The audio recording industry has pushed the state-of-the-art in DSP well beyond the needs of this receiver. In particular, noise-free digital delay offers the

possibility of intelligent audio AGC systems that go well beyond the best commercially available amateur receiver systems.

The R2pro is set up so that sophisticated laboratory instrumentation may be used to observe the distortion at all points in the signal path. The ear can often detect distortion that is difficult to measure, and the ear-brain quickly learns to recognize different distortion and noise mechanisms. The acid test is to set up the receiver with a switch that completely bypasses the DSP, and equal gain in the DSP and non-DSP modes. When the DSP is set for wide bandwidth, and switching between modes is completely transparent, the operator can be confident that the DSP system is not corrupting receiver performance.

AUDIO POWER AMPLIFIER

An audio power amplifier circuit is shown in Fig 9.74 (also see the board layout in Fig 9.75 and the photo in Fig 9.76.) Any audio amplifier with enough gain may be used at this point, but it is a shame to connect a low distortion receiver to an inexpensive IC amplifier with questionable fidelity. The version in Fig 9.74 has a gain of 46 dB, with the volume control arrangement shown. Since the audio power amplifier has high gain and is capable of medium power operation, signal currents flow in the power supply wires. It is critical that the power amplifier use appropriate audio amplifier construction practice. In particular, both speaker wires must connect to the appropriate

points in the circuit. Do not use the chassis as the negative speaker lead connection or as the negative power supply lead to the audio output amplifier. The circuit board layout works well when connected directly to the speaker, and to the power supply

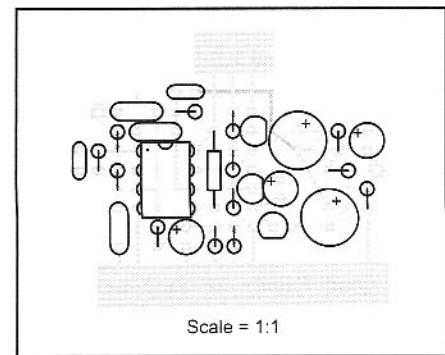


Fig 9.75—Board layout for the audio power amplifier.

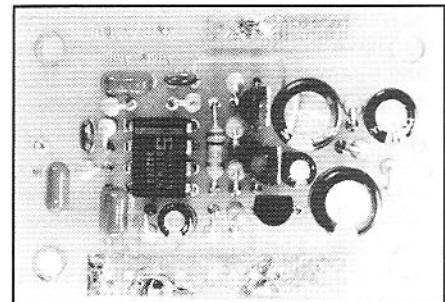


Fig 9.76—The audio power amplifier.

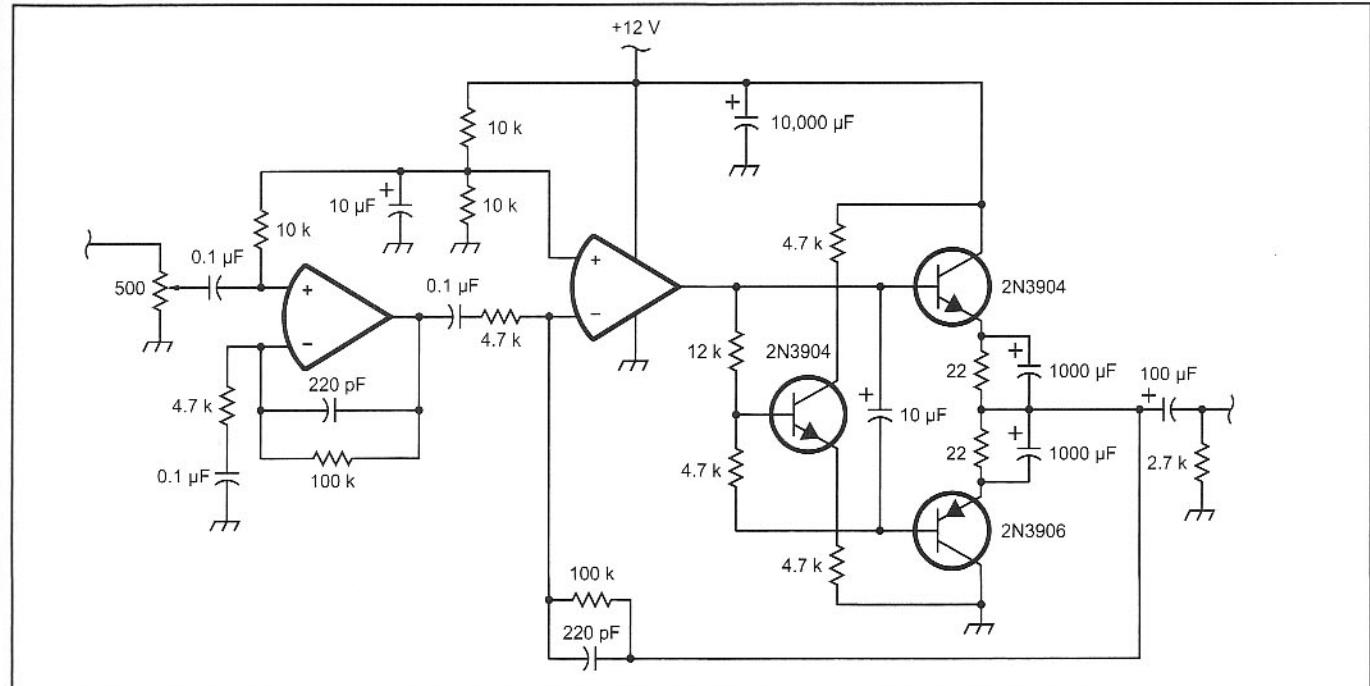


Fig 9.74—An audio power amplifier circuit.

capacitor with #18 wires. Feedback problems (howling) in direct conversion receivers can often be cured by using a separate battery power supply for the audio power amplifier. While this is not always attractive for normal operation, temporarily operating the audio power amplifier circuit board from a separate battery supply can serve as a very useful troubleshooting tool when trying to figure out which ground wire needs to be cut to eliminate the offending ground loop.

This audio power amplifier provides reasonable output with headphones or a small speaker in a quiet room. For more volume, an external power amplifier should be used. Some external sound card amplification systems for computers are quite good. Others are quite inexpensive. Each has its merits.

LOCAL OSCILLATOR

A local oscillator is not included in the R2pro receiver system, but the choice of LO in large part determines the success of the finished project. Two local oscillators that have been used to build excellent direct-conversion receivers are a well-shielded JFET Hartley and a moderately well-shielded JFET Hartley driving a balanced frequency doubler. When the diode doubler is used in a circuit with toroid inductors, open PC board construction is acceptable. The Kanga UVFO circuit in Chapter 12 works well and provides additional useful features such as CW offset and a keyed auxiliary output. Because of differences in the way even and odd harmonics add, direct conversion receivers that use odd harmonic frequency multipliers must be very well shielded.

While analog local oscillators represent mature technology and simple elegance, the state of the synthesizer art continues to progress rapidly. The best hybrid DDS—PLL synthesizers are very, very good, and continue to improve. The R2pro circuit blocks provide a convenient platform for experiments with different types of synthesizers.

Sideband Switching, Binaural, and ISB modes

It is not trivial to set up a switched-sideband phasing image-reject receiver system with equal sideband suppression on either sideband. This is particularly the case for the R2pro, with available sideband suppression of over 50 dB. The reason for the difficulty is subtle. In a phasing system, all the cumulative amplitude errors throughout the system may be compensated with a single amplitude trimming

adjustment. Similarly, all of the cumulative phase errors may be trimmed out with a single phase trim. When the sideband switch is thrown, the receiver configuration changes, and the distribution of amplitude and phase errors is likely to change. Our R2 and miniR2 receiver trimmed for more than 40 dB opposite sideband suppression on one sideband typically exhibit less than 30 dB opposite sideband suppression when connections to the analog signal processor are reversed. Readers fluent in image-reject concepts can investigate options for sideband switching that preserve the distribution of amplitude and phase errors when switching sidebands. A good strategy is to trim the errors before the audio phase shift network, so that at the input to the nearly ideal analog signal processor the I and Q channels have precisely equal amplitude and 90° phase shifts. Reversing connections at this point will then switch sidebands without redistributing the errors.

One viable method to provide good sideband suppression in a switched-sideband receiver is to make the amplitude and phase trim adjustments front-panel controls. This is particularly attractive for receivers that cover a wide frequency range, as phase shifts will likely need to be tweaked when changing bands. Judging from the front panels of many high-end radios, there is no penalty for providing additional operator control over receiver functions. A well-shielded external crystal calibrator with variable output is a useful accessory for a receiver with front-panel phase and amplitude trims. It is important that the test signal enter the receiver on the antenna connector, and that all leakage paths into the I and Q RF circuitry are 60 or 70 dB down.

For single-band switched-sideband receivers, there are other options. From the basic theory, four trimming adjustments (one amplitude and one phase trim for each sideband) are needed for to optimize suppression of either sideband. A very conservative option is to use two independent down-converter and analog signal processor PC boards, with switched (or split) LO and RF inputs. An independent LO (or RF) phase trim can then be implemented for each downconverter, and one analog signal processor can be set up for upper sideband and the other for lower sideband. The desired sideband may then be selected by switching between analog processor outputs. Of course, an additional audio power amplifier could also be added for full Independent Sideband operation. The trimming adjustments for suppression of opposite sidebands are completely independent in this implementation.

Binaural operation is simple to add to an ISB receiver with two identical audio channels. Binaural ISB, with one sideband in each ear, just requires additional switching. For Binaural IQ, as described in March 1999 *QST*, the I and Q outputs of the downconverter board are amplified by a stereo amplifier. A number of experimenters have noted that Binaural IQ receivers sound best with very little audio filtering. A versatile receiver might have a switch that provides wide open Binaural IQ for tuning around the band and then a number of narrow band options for communicating with individual stations.

Some of the receiver circuitry in the previous paragraphs adds many parts to achieve a very tenuous performance advantage. Philosophically, minimum parts considerations should not apply to high-performance phasing direct-conversion receivers. Also philosophically, front-panel amplitude and phase trim adjustments are an elegant solution, and are really cool to play with. The philosophy behind each receiver is different, however—which may be the whole point of this entire book.

Trimming

Finally, here are a few words on the actual process of trimming a phasing receiver for best opposite sideband suppression. A “target” analogy is a useful way to think about trimming a phasing receiver. The undesired

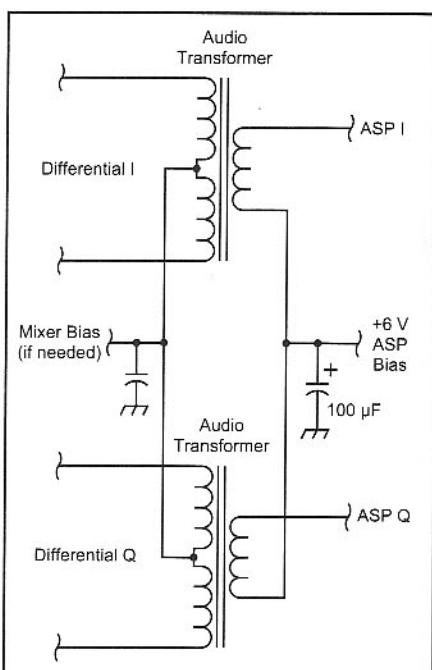


Fig 9.77—A circuit for connecting an I Q balanced mixer output pair into the I and Q inputs of the R2pro analog signal processor board.

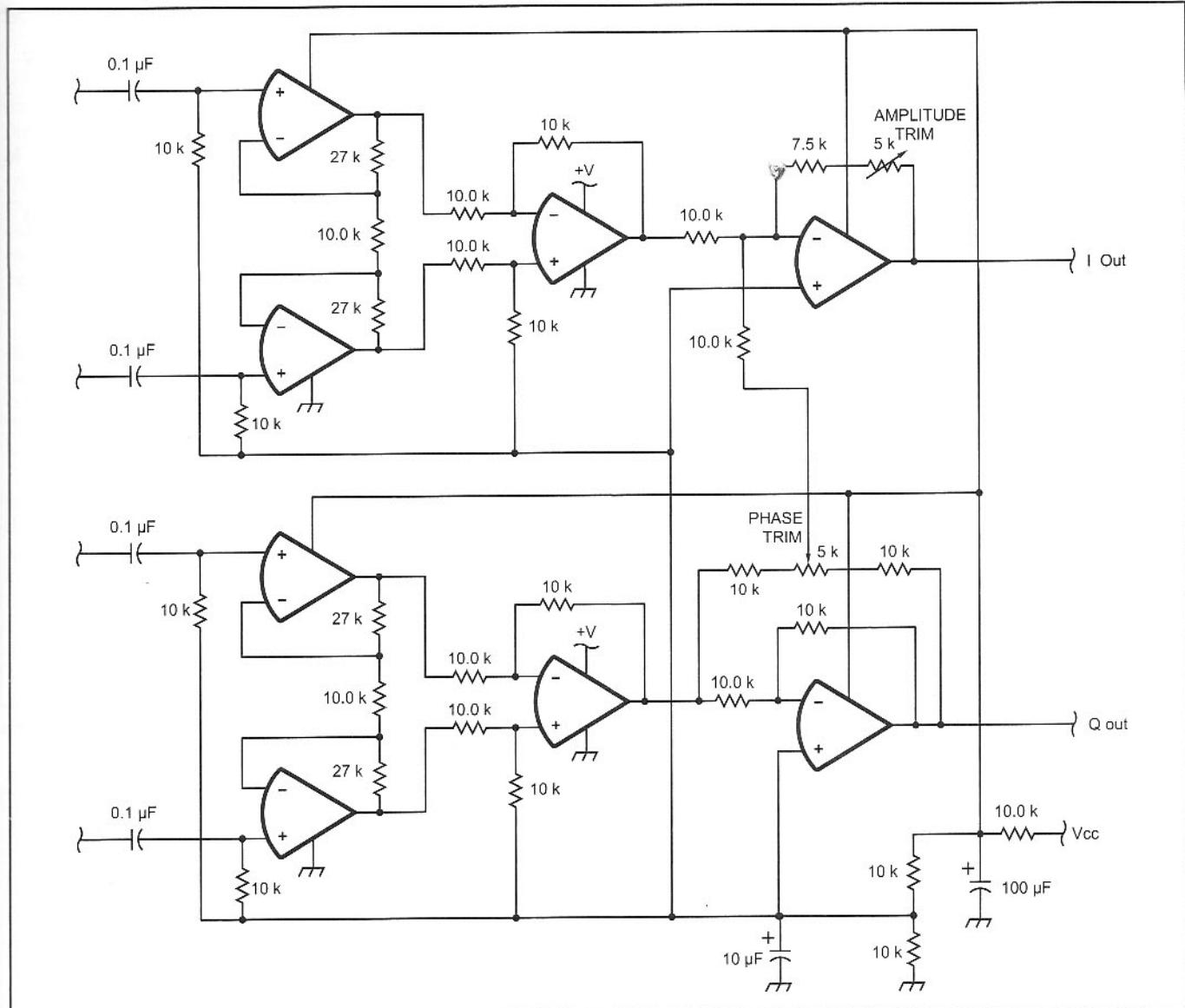


Fig 9.78—Connecting the I Q balanced mixer output pair into the I and Q inputs of the R2pro analog signal processor using a pair of differential op-amp circuits.

opposite sideband level is the distance from the center of the target. The two adjustments, amplitude and phase, are like the windage and elevation adjustments on a gun sight. If one adjustment is way off, adjusting the other one will have little effect on distance from the center of the target. Once one adjustment is perfect, the other adjustment will have a very large effect.

In a phasing receiver, the output we hear when tuned to the wrong sideband is the level of the undesired signal, which represents distance from the target center. There is no indication whether amplitude, phase, or both need to be adjusted. If neither adjustment has much effect, then both are way off. Adjust first one, then the other, while listening to the undesired signal level. As the adjustments approach the optimum values, they become more criti-

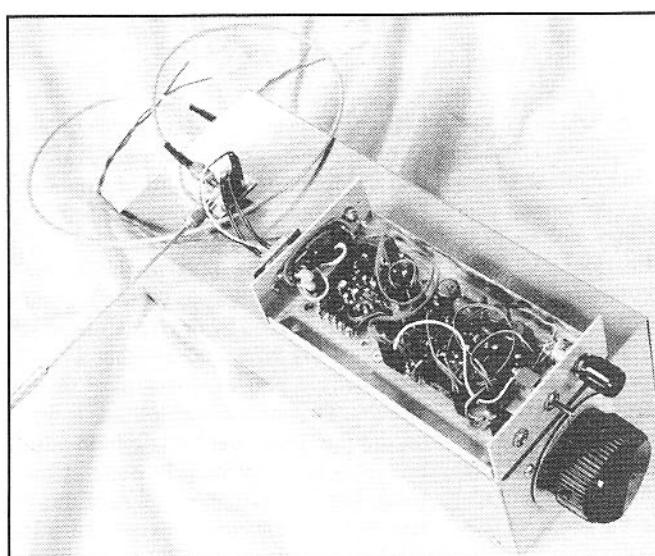


Fig 9.79—The interface circuit board connected between the R2pro ASP and a commercial IQ mixer operating at 2.3 GHz.

cal. It should be possible to reduce any sine wave frequency in the audio passband down below the noise level. If the signal is strong, it will be possible to reduce the fundamental below the noise while hearing the distortion products. It is important to listen while adjusting, because a meter can't tell the difference between the signal being suppressed, the desired channel noise floor, and distortion products. Once a single-frequency tone is suppressed below the noise floor, tune the receiver slowly to change the tone frequency and observe its suppression. In a properly adjusted R2pro, the suppression will be more than 50 dB over the entire audio frequency range. If it is not, re-optimize the receiver using a different tone frequency. Frequencies near the middle of the receiver audio passband are most useful.

A phasing receiver will always have some opposite sideband suppression. If it does not, then one of the two channels is not working. If the signal has equal strength on either side of zero beat, don't touch the amplitude and phase trimmers, fix the broken I or Q channel first.

Once a phasing receiver using modern components is optimized, the phase and amplitude adjustments hold very well. The prototype miniR2 on 20 meters still exhibits 43 dB opposite sideband suppression from 300 to 3000 Hz after six years, a circumnavigation, numerous camping trips, and a number of disassemblies to display the circuitry.

Interface Circuitry For Other Mixer Types

Much of our work in the amateur bands uses diode ring mixers. Diode rings work well, are available in small quantities in many different varieties, and offer good performance in familiar, mature circuits. Much of our work in our professional lives has been in the development of passive FET mixers of various topologies. FET mixers offer a number of performance trade-offs with diode rings, and often the passive FET mixers are superior. There is also a wide variety of other mixer types including active mixers using Bipolar and CMOS transistors that may be the best choice for some applications. Classic vacuum tube beam deflection mixers, and future optical mixers offer interesting experiment possibilities. This paragraph presents a few interface circuits that have been developed to interconnect passive FET balanced and I Q mixers to the baseband circuitry developed for the R2pro. Much of this work is in the microwave bands, and outside the scope of this text.

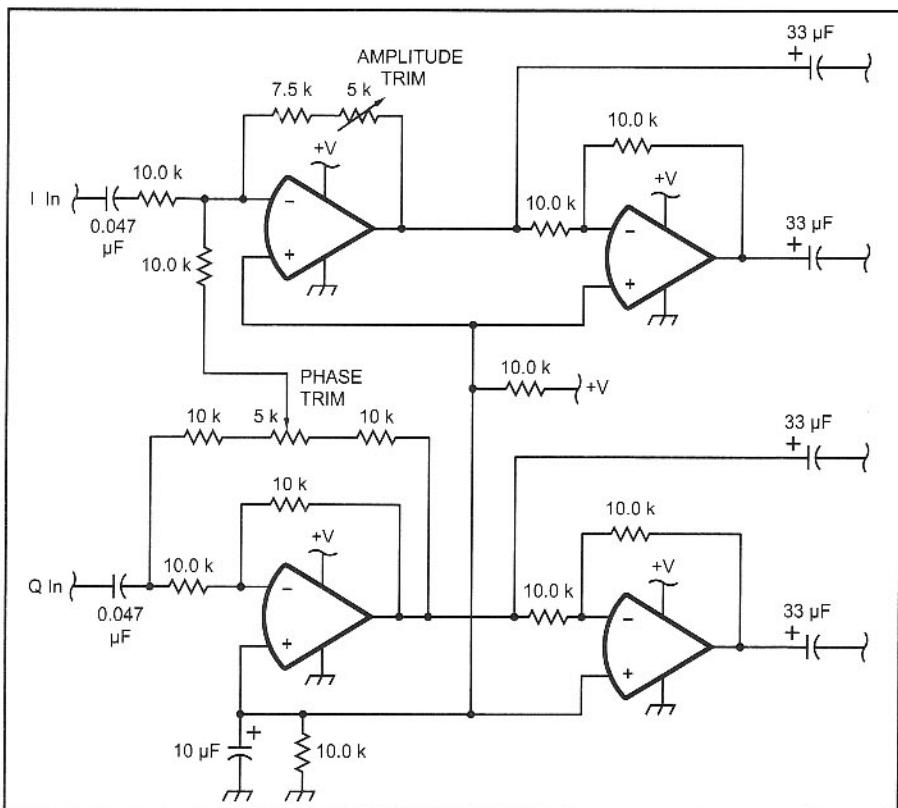


Fig 9.80—A circuit that provides dc-isolated balanced I and balanced Q drive to the inputs of an I Q upconverter.

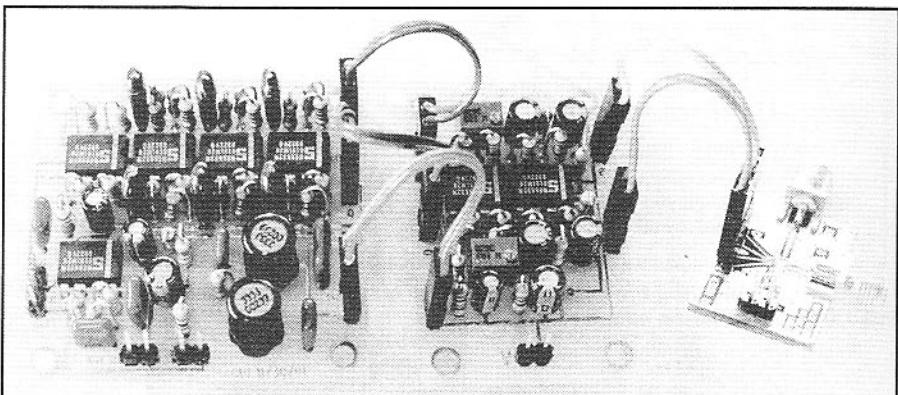


Fig 9.81—A prototype microwave SSB exciter connected to a commercial passive IQ FET mixer at 2.3 GHz.

Fig 9.77 is a circuit for connecting an I Q balanced mixer output pair into the I and Q inputs of the R2pro analog signal processor board. The center-tapped floating transformer primaries may be used to provide operating bias to the mixer if needed, and 6 V bias to the ASP I and Q inputs is provided by the transformer secondaries. Fig 9.78 accomplishes a similar task using a pair of differential op-amp circuits. The phase and amplitude trim pots on the interface board allow both adjustments to be conveniently done at baseband. Fig 9.79 is a photograph of this circuit board connected between the R2pro ASP and a commercial IQ mixer operat-

ing at 2.3 GHz.

Passive FET mixers are also used as upconverters, and Fig 9.80 is a circuit that provides dc-isolated balanced I and balanced Q drive to the inputs of an I Q upconverter. Fig 9.81 is a photograph of a prototype microwave SSB exciter connected to a commercial passive FET mixer at 2.3 GHz.

Alternative mixer types are a rich field for amateur experimentation, and there is much progress to be made in this area. Between the 50-Ω interface circuitry described for diode rings and the balanced circuitry presented here, an experimenter should have the tools needed for experiments with many different mixer types.

9.10 A HIGH PERFORMANCE PHASING SSB EXCITER

After completing the R2pro design, it was natural to take a similar approach to the basic phasing exciter. The design of the resulting circuit is described here. In block diagram form, and even in simple circuit implementations, a phasing SSB exciter and SSB receiver have much in common, but as circuitry is optimized for each application, significant differences become apparent. A few differences are:

1. The audio drive signals at the exciter diode ring IF port are only about 10 dB below the LO drive. The diode ring thus contributes significant distortion, and its IF port impedance will vary dynamically with drive.
2. The overall gain from microphone input to exciter output is much lower than the gain in a receiver. Curing unwanted audio feedback and oscillations in an exciter are not significant design tasks.
3. Carrier suppression is an issue, and can not be helped by RF amplifier reverse isolation.
4. RF feedback from the antenna back in to the modulator or LO tuned circuit causes FM.
5. There are significant differences in the handling of SSB and CW.
6. There are significantly different grounding considerations.

Since there are so many different requirements between optimized receiver and exciter circuitry, each exciter circuit block was redesigned, borrowing subcircuits from the receiver and previous designs where performance met the exciter requirements.

Microphone Amplifier

The microphone amplifier input is the connection point for a dynamic or electret mike element. It needs to interface to a wide variety of signal sources without changing its gain or passband characteristics. The microphone amplifier defines the noise floor inside the channel during pauses between words, or when using an external digital signal source connected to the exciter audio input. Typical inexpensive electret elements with integral FET amplifiers have an output voltage of about 20 mV and a signal to noise ratio of more than 60 dB. The mike amplifier needs to

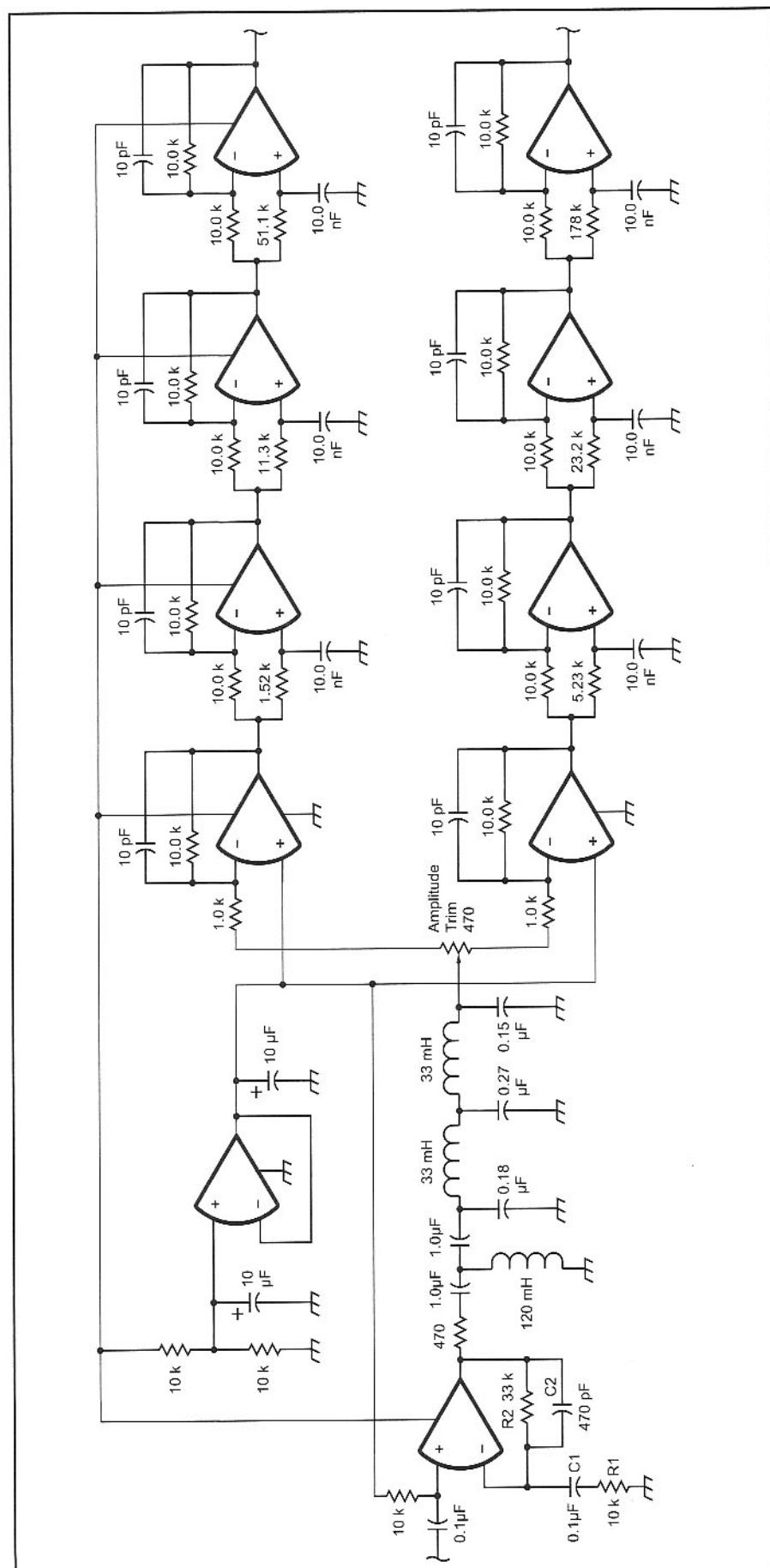


Fig 9.82—This schematic is a speech amplifier and analog signal processor.

The I and Q audio outputs may be directly connected to either the modulator circuit shown in Fig 9.83 or the balanced output circuit in Fig 9.80.

have input noise much less than 20 μV across the speech passband to ensure that the exciter noise is below the microphone noise. Typical low-noise Op-Amps have input noise voltage of less than $10\text{nV}/\text{Hz}^{1/2}$. Thus the equivalent input noise from the op-amp in a 4-kHz bandwidth is about 630 nV—90 dB below the microphone output. This is good enough for any microphone likely to be used in amateur service.

It is useful to calculate the output noise floor of the exciter when the microphone is disconnected. If the rms input noise of the mike amplifier is 630 nV across the speech bandwidth and the transmitter linearly amplifies a 20-mV signal up to, for example, 10 W (22.4 V rms) into a 50- Ω load, then the transmitter has a total of 61 dB linear gain from the microphone input to the antenna. The output noise voltage is 61 dB stronger than 630 nV, or 700 μV rms. The noise power at the output is 10 nW—low power even by QRP standards. When the inexpensive electret mi-

crophone is connected, the noise output increases by 30 dB, up to about 10 μW . This is strong enough to easily hear in nearby receivers on the quiet VHF bands.

The microphone amplifier circuit in Fig. 9.82 has an input impedance of 10 k Ω , 10 dB gain, a high-pass characteristic defined by R1 and C1 and a low-pass provided by R2, C2. For maximum fidelity and flexibility in tailoring the microphone response, the mike amplifier passband is flat from 150 Hz to 4 kHz, with very graceful roll-off above and below. The output impedance of the Op-Amp is raised to about 500 Ω with the series resistor, to drive the LC speech filter.

High Fidelity Speech Filter

The speech filter is designed for high quality speech and rapid roll-off above the desired passband. A 1-dB ripple Chebyshev low-pass prototype was scaled to 500 Ω and 4 kHz to provide the high

frequency filter edge, and a single series capacitor provides one high-pass pole at 100 Hz. The filter output is terminated in the 470- Ω input resistor to the inverting input of the output op-amp.

The gain distribution through the exciter audio is designed to minimize off-channel noise and the impact of component tolerances on opposite sideband suppression. Most of the audio gain is before the LC speech filter, so that the filter will have maximum effect on off-channel amplifier noise. The 1-dB ripple Chebyshev speech filter has rapid phase and amplitude variations near the upper passband edge, so this filter is placed before the audio channel is split into I and Q paths. A matched pair of such filters could be used at the output of the I and Q phase shift circuitry to suppress the op-amp phase-shift network noise, but then the component tolerances would have to be unreasonably tight. Instead, a pair of simplified 50- Ω LC low-pass filters is used after the I and Q audio power amplifier stages to remove the

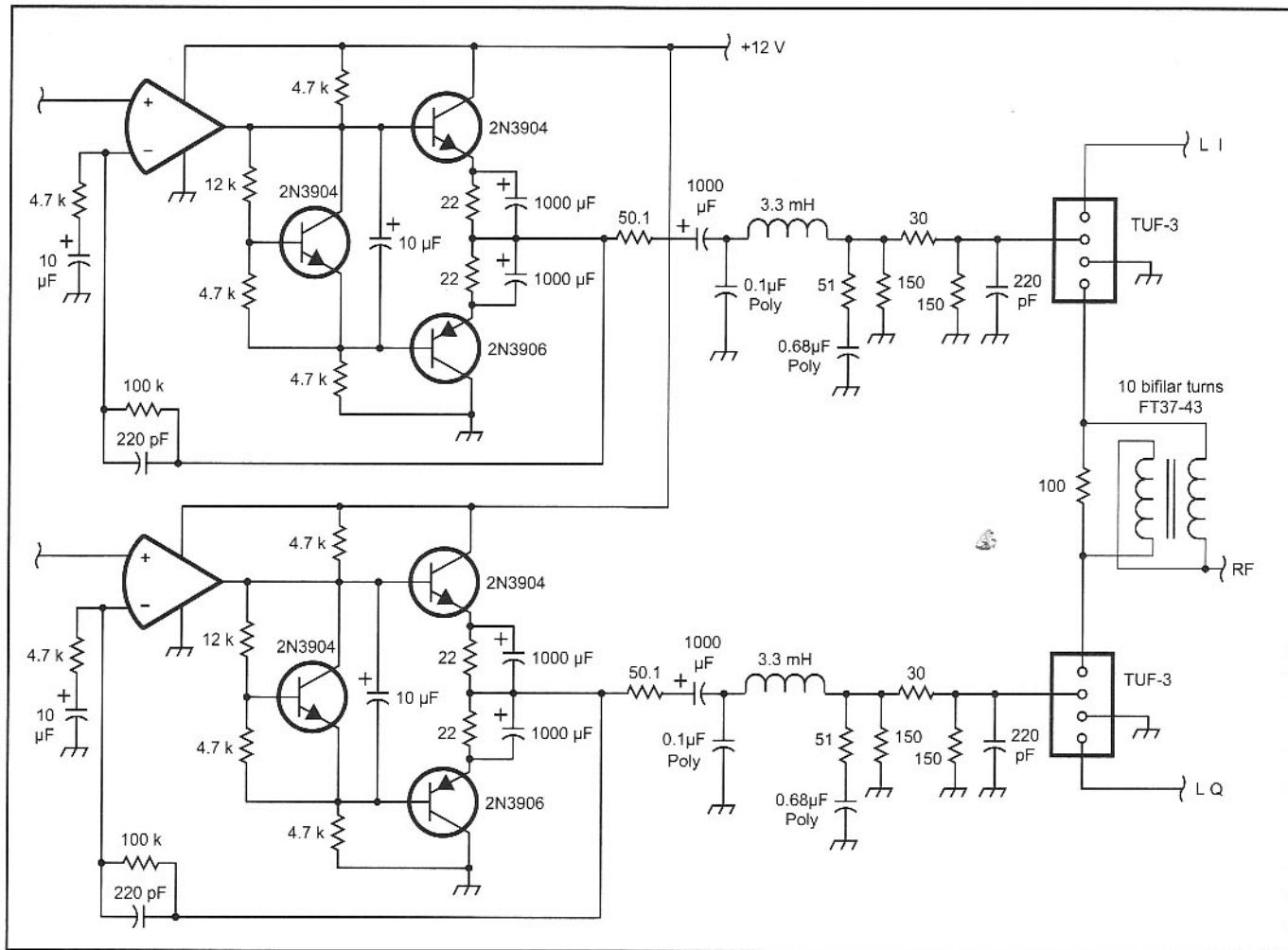


Fig 9.83—The modulator circuitry shown here is connected directly to the output of the audio phase-shift network.

broadband noise from the active phase-shift network and I and Q power amplifiers. These $50\ \Omega$ LC low-pass filters were designed for amplitude and phase errors small enough for more than 50 dB of opposite sideband suppression when built with 1% matched components.

Buffer Amplifiers

The LC speech filter termination drives a pair of buffer amplifiers through the amplitude balance pot. These buffer amplifiers provide low impedance drive to the audio phase-shift network. This is a change from the April 1997 *QST* circuit that drove the phase shift network directly from the amplitude balance pot. The original circuit could be adjusted for more than 40 dB of opposite sideband suppression, but both the amplitude and phase needed significant re-adjustment when switching sidebands. The new circuit may be adjusted for almost 50 dB of opposite sideband suppression with very little trimming needed when switching sidebands.

Audio Phase Shift Network

The audio phase shift networks are copied directly from the R2pro circuit. There is no need to change component values. There is some degradation of sideband suppression at audio frequencies below 200 Hz, but less than one would experience with a filter exciter. Using the values derived for the receiver provides maximum suppression of adjacent-channel interference. Dual op-amps are used instead of the quad op-amps specified in the earlier *QST* circuit to ease board layout and reduce the number of parts that need to be kept in stock. With parts selected to 0.1% tolerance, this phase shift network pair will provide more than 50 dB of opposite sideband suppression from 300 to 3500 Hz.

Mixer IF Port Driver Amplifiers

The modulator circuitry shown in Fig. 9.83 is connected directly to the output of the audio phase-shift network. As in the R2pro circuitry, this connection is dc coupled and carries the 6 V bias for the modulator op-amps. The I and Q output audio amplifiers are changed significantly from the earlier design. One issue is that diode ring IF port impedance is a function of both LO drive level, and for modulator service, IF drive level. Since the diode ring IF port is the termination for the LC noise filter, any change in impedance will create

phase and amplitude errors between the two channels. Not only do such errors limit the amount of sideband suppression that may be obtained, they will change when tuning across the band, and require readjusting the exciter when switching sidebands. A significant reduction in phase and amplitude errors caused by diode ring IF port impedance variations may be made by adding a 6-dB $50\ \Omega$ attenuator between the LC filter and the diode ring IF port. This attenuator may also improve diode ring intermod distortion performance.

The input termination to the I Q LC filter pair is provided by a the low impedance output of the audio power amplifier circuitry with a $50\ \Omega$ series resistor and $1000\ \mu F$ dc blocking capacitor. The dc blocking cap could have been used to shape the channel, but then it would have had to be a precision component. Since $10\ \mu F$ capacitors with the necessary tolerance are both expensive and very large, the capacitor value was increased to the point where a standard tolerance electrolytic could be used. A $1000\ \mu F$ capacitor with a $50\ \Omega$ load has a high-pass pole at 3.2 Hz. A +50% capacitance error from $1000\ \mu F$ to $1500\ \mu F$ in just the I channel introduces less than 0.1 degree of differential phase error in the low end of the audio passband.

The appropriate drive level for the diode rings is determined by the desired amount of third order distortion. There is a trade-off between third-order distortion, carrier level, and exciter noise. Exciter third order distortion may be reduced to an arbitrary low level by driving the IF port at low level, but then the RF output is low relative to the diode-ring LO output, and more noisy gain must be used to reach the desired RF output level. With +7 dBm LO drive and two 0 dBm tones on the IF ports of a TUF-1 mixer, the RF third-order products are only 15 dB down from the -9.0 dBm desired outputs. This might be acceptable for some simple VHF or microwave applications where the mixer is connected directly to the antenna—but it is hardly in keeping with a high-performance phasing exciter.

Of particular importance is the fact that mixer intermod products do not have the same phase relationships between the I and Q channels as the desired signals that produced them. The largest signals in the opposite sideband of a phasing exciter are usually intermod products, not the suppressed sideband. Thus it is meaningless to build a phasing exciter with phase and amplitude accuracy to provide 50 dB of opposite sideband suppression, and then over-drive the I and Q mixers so that the intermod products are only 30 dB down.

Measurements

A TUF-1 mixer was measured with two -10 dBm IF tones and a 22 MHz, +7dBm LO. The desired outputs dropped to -15.3 dBm, and the 3rd order intermod products dropped to 47.5 dB below each desired tone. -15.3 dBm outputs from -10 dBm inputs indicates a conversion loss of only 5.3 dB. The 22 MHz carrier feedthrough is at -63.3 dBm, or 48.0 dB below either tone of the two-tone output. At 7 MHz the carrier suppression improves to 49.9 dB below either of the two tones.

From these experiments with -10 dBm two-tone drive into a single mixer, the carrier and intermod products are both more than 47 dB below either tone. This puts them -53 dB below the PEP output. Combining a pair of these mixers as a SSB modulator makes a further improvement. The carriers from the two mixers are 90 degrees out of phase, so the resultant voltage is 1.414 time the voltage of each carrier. The desired sideband adds in phase, so the resultant voltage is 2.0 times the voltage for either mixer output. A passive combiner involves an impedance transformation, so the resultant voltages are reduced by 0.707 into a $50\ \Omega$ load. The final output tones are then 3 dB stronger than the tones from a single mixer, but the combined carrier outputs are the same as for a single mixer.

The situation is more complicated for intermod products. Some of them add in phase, some cancel, and some add with 90 degree phase shift. The worst case is when the intermod products add in phase, exactly the same as the desired sideband.

A SSB modulator built with two TUF-1 mixers operating at a carrier frequency of 22 MHz, with two -10 dBm tones into each mixer IF port, will have desired sideband output tones of -12.3 dBm (-15.3 dBm + 3 dB), a carrier 51 dB below either tone, and intermod products at least 47 dB below each tone. This performance is a good fit with a precise phase shift SSB system that provides 50 dB of opposite sideband suppression.

The IF amplifier driver amplifiers are also potential sources of distortion. With a 6-dB pad between each LC low-pass filter mixer IF port, filter loss, and the 6-dB loss through the $50\ \Omega$ series termination resistor, the total loss between the driver amplifier and mixer IF port is about 14 dB. Two -10 dBm tones is -4 dBm PEP, so the driver amplifier must supply a two-tone +10 dBm with distortion products well below the level produced by the mixer. Fortunately, a suitable amplifier was designed as the audio output stage for the R2pro. At the +10 dBm PEP output level, distortion products are all more than 60 dB below each of the desired tones.

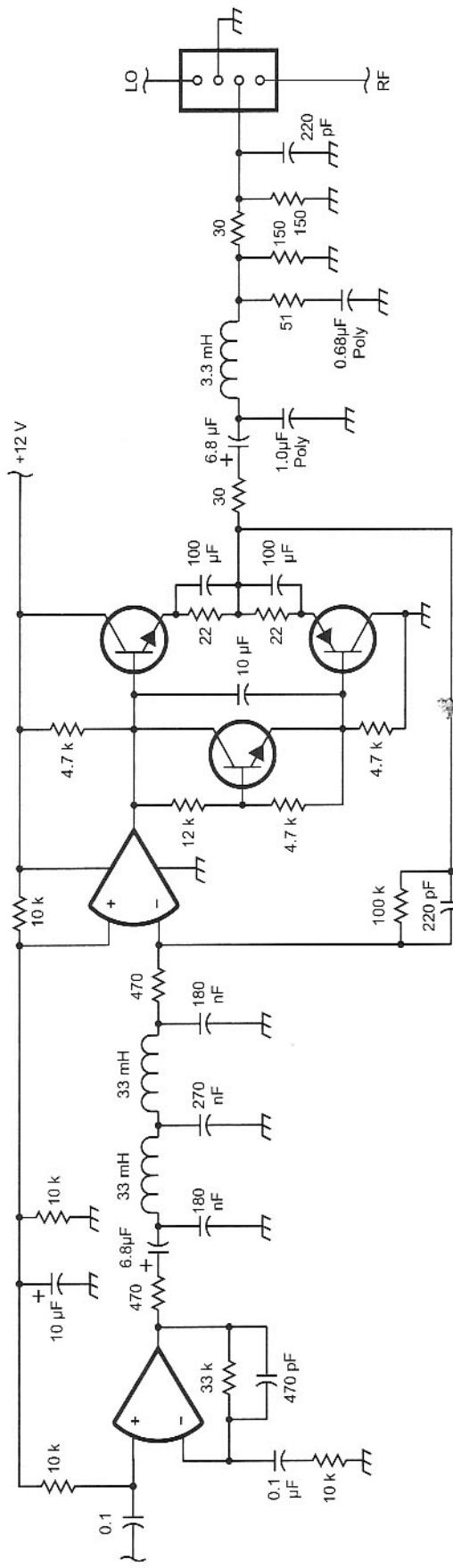


Fig. 9.84—A complete low-distortion DSB modulator with 50- Ω output.

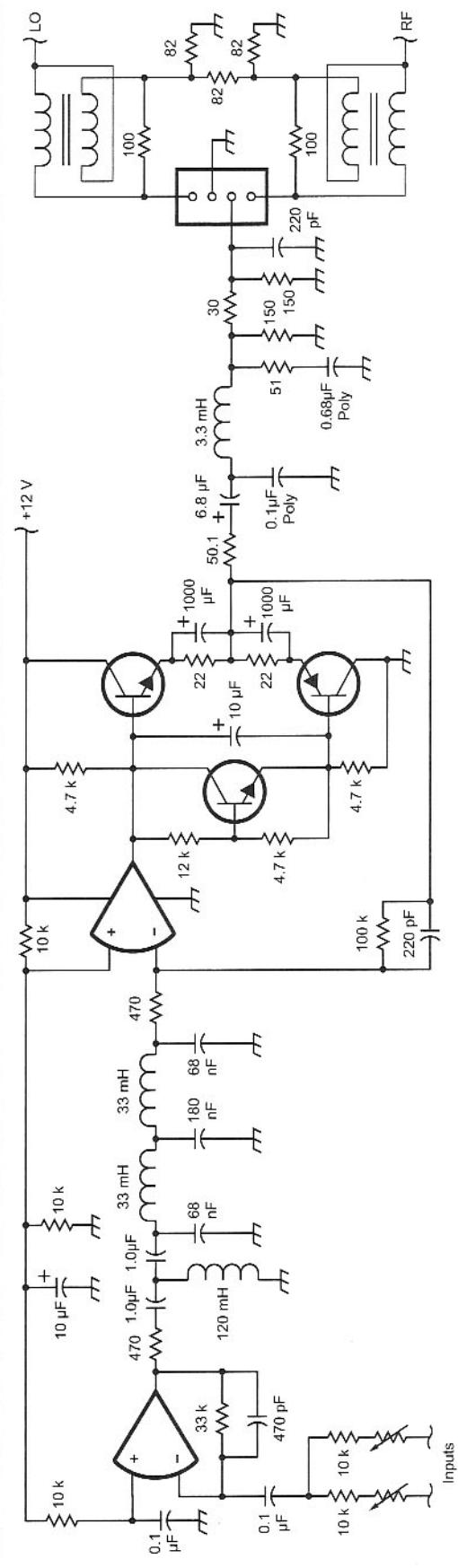


Fig. 9.85—An AM exciter that generates a DSB signal and then adds the correct amount of carrier to obtain 100% modulated AM at very low distortion.

Mixer Environment

To obtain 50 dB opposite sideband suppression, amplitude errors between the I and Q channels across the entire speech passband must be held to less than about 0.03 dB, and phase errors must be held to less than 0.007 radians (0.4 degrees). Since mixer port terminations affect both conversion loss and the phase behavior of any LC networks connected to the ports, it is important for the mixers to operate in as ideal an environment as possible. Good 50- Ω terminations on all three mixer ports, constant LO drive level, and good isolation between the RF ports of the I and Q mixers are all necessary to maintain sideband suppression. Isolation between the I and Q mixer RF ports is needed because the LO leakage from one mixer is 90 degrees out of phase with the LO drive to the other mixer. This is precisely the phase that results in maximum sensitivity to recovery of phase noise or other fluctuations on either mixer.

On each mixer port, 6-dB resistive pads will generally improve opposite sideband suppression across the audio and RF passband. In transmit applications, the noise figure penalty is less of a concern, so the use of a 6-dB pad on each IF port, and a 6 dB increase in audio drive level, is good practice. Pads on the LO ports of the mixer help maintain opposite sideband suppression when LO connections are changed (or cables are flexed). LO port pads should be used if sufficient LO drive level is available. Above 20 MHz, the Mini-Circuits MAV-11 provides a simple way of obtaining +17 dBm of LO drive. After a twisted-wire hybrid splitter, the I and Q LO levels will both be +14 dBm. 6 dB pads (and a little circuit loss) will drop this to the appropriate drive level for standard level diode ring mixers. A 6 dB pad on the RF port helps maintain constant mixer behavior across a wide RF band. An alternative to a resistive pad on the RF port is an amplifier with a good, broadband, resistive input match and high reverse isolation. The reverse isolation prevents changes in the amplifier output load from appearing at the mixer summer.

sion when LO connections are changed (or cables are flexed). LO port pads should be used if sufficient LO drive level is available. Above 20 MHz, the Mini-Circuits MAV-11 provides a simple way of obtaining +17 dBm of LO drive. After a twisted-wire hybrid splitter, the I and Q LO levels will both be +14 dBm. 6 dB pads (and a little circuit loss) will drop this to the appropriate drive level for standard level diode ring mixers. A 6 dB pad on the RF port helps maintain constant mixer behavior across a wide RF band. An alternative to a resistive pad on the RF port is an amplifier with a good, broadband, resistive input match and high reverse isolation. The reverse isolation prevents changes in the amplifier output load from appearing at the mixer summer.

likely to need very little trimming when switching sidebands. The sideband selection method chosen depends to a large extent on whether the exciter is to be used at a single frequency, or will be required to cover a multi-octave range, and whether the I and Q audio drive is obtained from a DSP chip or an analog IC chain.

A DSB Modulator

The same basic circuits that are used to build up a phasing exciter may be used to build up a DSB or filter-type SSB exciter. Fig 9.84 is a complete low-distortion DSB modulator with 50- Ω output. The microphone gain should be set up so that the output level at each sideband is -15 dBm.

DSB with Carrier

There are applications for a very low distortion AM exciter. Fig 9.85 is an AM exciter that generates a DSB signal and then adds the correct amount of carrier to obtain 100% modulated AM at very low distortion. Two inputs are provided, so that the exciter may be connected directly to the stereo output of a CD player. With a +10 dBm LO in the 1 MHz range, this exciter may be used to play collections of vintage radio programs over lovingly restored AM broadcast radios. Use low-pass Pi networks to connect to the 25- Ω RF and LO ports.

9.11 A FEW NOTES ON BUILDING PHASING RIGS

Some of our phasing rigs have been learning experiences, and some are fine radios that have displaced all the commercial equipment in the author's home and portable stations. The most successful radios have a few features in common.

1. Separate receiver and exciter circuitry. The individual components in phasing rigs are inexpensive, and it is false economy to include complex switching networks so that a circuit block used in the receiver may also be used in the exciter. Complicated switching schemes to re-use receiver components in the SSB exciter is an obsolete concept that became popular in the 1960's to save money on expensive crystal filters, and to reduce the number of vacuum tubes and filament current drain.

2. A common VFO for full transceive operation, but independent LO phase shift networks. A conservative approach is to distribute low level LO signals on 50 Ω lines to buffer amplifiers and LO phase-shift net-

works in the exciter and receiver modules. This eliminates interaction between the receiver and exciter adjustments.

3. Buffered RF ports on both the receiver and exciter. A receiver LNA with good reverse isolation and a relatively broadband, near 50- Ω RF output should be hard-wired to the RF input of the image-reject mixer. The exciter image-reject mixer should be hard-wired to a broadband, 50 Ω low-level amplifier input. The LNA and exciter low-level output amplifier should be built into the receiver and exciter modules.

4. Good RF filtering and a very clean LO. Phasing circuitry does a fine job of eliminating the opposite sideband, but it does nothing to reduce strong off-channel and out-of-band signals that can cause interference through various distortion mechanisms.

5. Modular construction using feedthrough capacitors and mechanically solid RF-tight enclosures. Not only are individual modules easier to test and align,

they hold their alignment when interconnected, and greatly reduce spurious responses and outputs. Modular construction with 50 Ω interconnecting signal cables and bypassed dc connections should be used whenever performance is more important than construction time.

The philosophy behind our phasing rigs is also worth noting. Early amateur work, and much of the professional use of phasing techniques, has been motivated by the desire to cut costs. In contrast, our work has been primarily directed toward improved performance compared with the usual inexpensive narrow-IF-filter superheterodyne approaches. It is an interesting exercise to build and communicate with a radio having only a few parts, but that is a different experience from using a system designed for smooth operation and high performance. For minimum parts count projects, simple DSB direct conversion receivers and simple superhets are often the best choice.

9.12 CONCLUSION

In the 25 years since publication of *Solid State Design for the Radio Amateur*, much has changed. Some of the most simple, light-weight mountain rigs include microprocessor frequency control and superhet receivers with crystal filters carefully designed for optimum CW intelligibility. Rack-mount direct conversion receivers are used in high-end weak-signal tropospheric scatter UHF SSB and CW stations. EME contacts have been made using a few watts of transmit power and truly awesome receiver signal processing power.

At the end of this chapter it is useful to explore some of the advantages of phasing receivers and excitors.

1. Phasing techniques work at any frequency. This can be used to eliminate frequency conversions in heterodyne receiver and transmitter system, which makes it easier to avoid internal and external spurious responses and achieve spectral purity. The same baseband processor may be used with simple RF circuitry on any amateur band from 170 kHz through millimeter waves.

2. Phasing receivers and excitors require low distortion mixers and audio amplifiers. While it is possible for a conventional superhet receiver or exciter to sound good, most published designs and commercial

products do not. High fidelity is necessary for a phasing rig. Now that there are many published receiver and exciter phasing circuits to duplicate, the designer-builder can confidently construct a very fine sounding radio system.

3. The emphasis on low distortion all the way through the RF to audio chain means that there is no penalty for using audio filtering for selectivity. High-performance audio filters may be realized using conventional L C networks or digital signal processing systems.

4. Phasing rigs inevitably have lower in-channel distortion than conventional superhets using narrow filters. Low in-channel distortion provides a significant performance improvement on any mode that injects a baseband signal into the SSB microphone input and recovers the signal from the receiver audio output. This includes conventional SSB and all of the present and future modes using Computer Sound Cards interconnected with the radio.

5. The basic phasing rig block diagram has many components that may be replaced by DSP and DDS systems. DDS and DSP are two areas in which the state of the art is rapidly advancing. Phasing receivers and excitors provide the radio experimenter with the interface between antennas and the latest advances in signal pro-

cessing technology.

6. The final advantage to phasing systems is philosophical. A basic superhet receiver with a crystal filter is fairly easy to explain and understand. It is also straightforward to build, and alignment is simple. When badly constructed and poorly adjusted, it still provides adequate performance. A phasing receiver is no more complicated than a superhet, but its underlying principles are more subtle. Care in construction pays off, and listening while playing with the phasing adjustments is really very cool. An amateur who has built up a phasing receiver, looked at the I and Q channel signals on a dual-trace oscilloscope, and tweaked the phase and amplitude adjustments while listening to an opposite-sideband signal drop into the noise acquires a depth of understanding far beyond that of most wireless graduate students and many of their professors. The best part is that understanding of phasing systems comes from experimenting with simple circuits and thinking—the tinkering comes first—then the understanding. In this area the amateur with his simple workbench; primitive test equipment; and time to contemplate, has a profound advantage over both the engineering student with a computerized bench and exam next week, and the professional engineer with a million-dollar lab and a technician to run it.

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DSP Components

The basic concepts of performing signal processing functions in a computer go back many years. Much of this processing was performed on relatively slow computers, where signals were treated as a series of numbers. But, Digital Signal Processing, or DSP, as applied to communications systems is more: It refers to the conversion of conventional analog signals into digital words, then processing these words for some useful purpose and the conversion back to analog signals. In addition, all of this must occur fast enough to keep up with the incoming signal. That is to say, the computation is "in real time."

The increased speed of digital computing hardware along with improvements in low-cost converters for input and output devices has brought DSP to many everyday products. This has made possible some functions that were difficult to perform in analog hardware. In addition, there are reduced production costs associated with using DSP, all of which is attractive to equipment manufacturers and home-builders alike. Not surprisingly, there are also limitations in using DSP to replace analog functions. These lie primarily in the areas of speed and dynamic range.

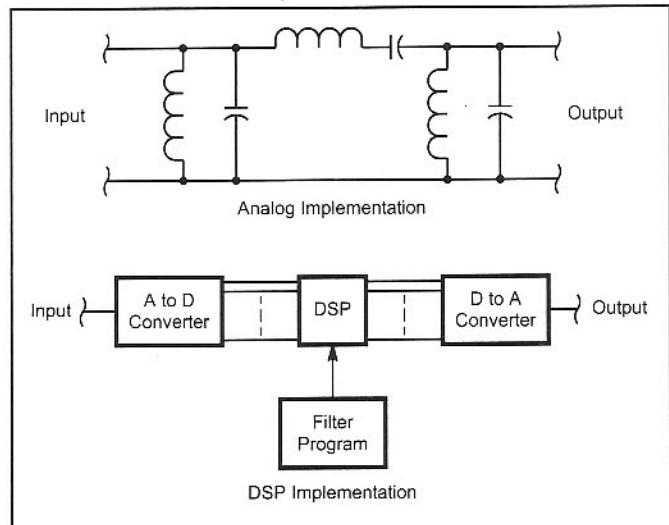
Figure 10.1 illustrates the implementation of a bandpass filter first as a conventional LC design and then as a DSP element. The LC design is obviously simple in only requiring 6 components. It can be built over a wide range of frequencies and

consumes no power. However, in order to achieve high Q in the inductors it may occupy a fair volume and, particularly at lower frequencies, may become heavy.

In contrast, the DSP version has much greater hardware complexity. Most of this is hidden away inside integrated circuits, but even the interconnect wires (PC board traces) will count in the tens or hundreds for most implementations. The DSP implementation might consume a few watts of power, as well. However, once the filter program is written, it is precisely

duplicated by any number of builders. Once the signal has been converted to digital form it is often easy to add other functions, such as AGC, or to increase the performance of the filter considerably beyond that which is practical for the analog filter. For this reason, it would be unusual to see a DSP based circuit that was as simple as just a band-pass filter. The DSP implementation is limited in the upper frequency that can be used and is most often seen for frequencies in the 10's of kHz. The increasing processing rates of DSP devices can be

Fig 10.1—Alternate analog and DSP implementations of a band-pass filter.



expected to push these frequencies up in the future.

In this chapter, we will explore the types of DSP building blocks that can replace or supplement analog circuitry. Where possible, comparisons with similar analog functions will be made. This will help to give a rational basis for mixing DSP functions into communications gear in the places where it "makes sense." Examples of mixed analog and digital circuitry will show how these building blocks can be used for both audio and IF applications.

This chapter will attempt to provide enough detail to allow construction or modification of working "DSP components." In the case of hardware construction, this usually requires that the builder is able to write down a schematic diagram complete with component values. For our software case, there is no direct equivalent of the schematic diagram. Many have tried to use various forms of "flow diagram" to communicate the contents of programs. For logic decisions, this can be a useful tool. However, for a computational algo-

rithm, such as a digital filter, the flow diagram does not add clarity over communicating directly with a well-commented computer program, written in a reasonably clear language. This approach will be applied here.

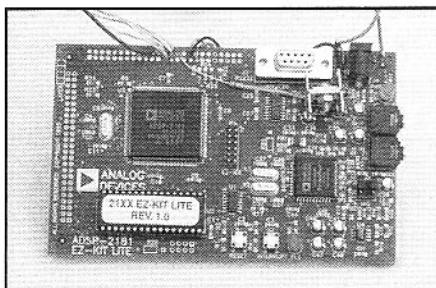
This chapter places emphasis on working DSP components. The background mathematics is not emphasized. However, there are other texts, such as that by Doug Smith¹, KF6DX, which should be consulted to add this perspective.

10.1 THE EZ-KIT LITE

One of the interesting parts of circuit design is the selection of components. For instance, we might need a basic NPN transistor to operate at low signal levels and since the "junk-box" has a supply of 2N2222 we will use them. These devices are readily available from a number of sources, inexpensive and chosen for those reasons, as much as technical ones. However, as the complexity of the circuit function increases, the devices become more specialized and the number of sources diminishes. For instance, most integrated RF amplifiers, even at low power levels, are available from only one or two sources. When we get to DSP devices it is a case of each manufacturer having a separate processor that not only doesn't substitute for any other, but that have different internal structures requiring different programming languages.

For these reasons, it is necessary to pick a specific language and a specific processor family when describing the operation of a DSP function. If this is not done, the description becomes quite mathematical and remote from an actual working program. The Analog Devices ADSP-2100 family and specifically the ADSP-2181 are used in this chapter to describe the DSP functions. This choice was made for several reasons:

- 1 – The assembly language is easy to follow



The EZ-Kit Lite.

- 2 – Good support manuals are available
- 3 – The EZ-Kit Lite makes getting started simple.

This, however, is not to say that the Analog Devices ADSP-21xx series is the best solution for a particular problem. However, this is a good all-around processor and provides a consistent language to illustrate the examples that follow.

Fig 10.2 is a block diagram of the EZ-Kit Lite board. The processor is an ADSP-2181 that has both 16K on-chip words of 16 bit data memory and 16K on-chip words of 24-bit program memory. This is more than adequate for any likely amateur project. When the board is powered down, programs can be stored in a 27C080, or in a smaller EPROM. The firmware procedure for loading from this 8-bit EPROM storage to the 24-bit program memory is part of the DSP hardware. The EPROM is not used after program loading is completed. The EZ-Kit Lite executes 33

million instructions per second.

Communications with a PC through a serial port requires a software UART (Universal Asynchronous Receiver/Transmitter) to be run in the EZ-Kit, but the hardware to change to RS232 levels is part of the board.

Analog input and output takes place through a dual (stereo) set of converters in a AD1847 CODEC.* The sampling rate of the CODEC is programmable up to 48 kHz and supports an analog bandwidth of about 20 kHz.

Other digital lines are available for con-

*The term CODEC stands for Coder/Decoder and refers to the combination of Analog-to-Digital and Digital-to-Analog conversions, along with dynamic-range compression algorithms. For the applications in this book, no compression algorithms are used, but we will still refer to the conversion package by its common nickname CODEC.

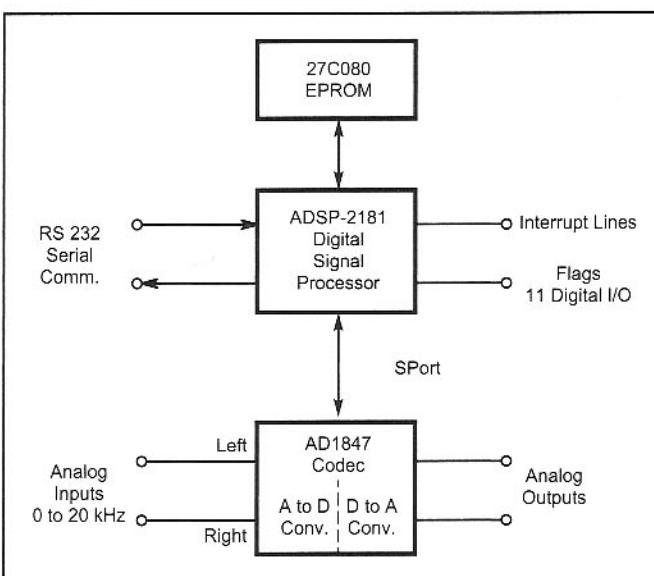


Fig 10.2—Block diagram of the EZ-Kit Lite from Analog Devices. The CODEC has dual A/D and D/A converters. Memory in the ADSP-2181 can be loaded from the EPROM.

trol purposes and connections are supplied for adding almost any kind of memory or I/O device.

Mixed-Modes

All real-life signals are analog in their nature. This means that a signal level is not constrained to a fixed set of levels, but rather may take on any level as time passes. Even the outputs of digital logic circuits are not just "0" or "1" but instead consist of waveforms that have rise-times, ringing and other variations. All of the RF, IF, and audio signals used in radio systems are, more obviously, analog.

DSP provides an alternate way to deal with these analog signals. This involves approximating the analog signal with a series of digital numbers, processing these numbers with some sort of computer and then creating a processed analog signal that again only approximates the desired result. It is important to keep in mind that the signal of real interest is the analog one. The digital calculations are only a means to obtain the processed signal. In order to maintain an adequate approximation of the analog signal, one must examine the computer routines and in some cases take special precautions. The human ear is often the final judge of DSP distortion. Most people cannot hear digitized distortion when 7 or 8 bits are used in the representation. Even with a 16-bit processor, care must be taken to ensure that this number of bits is retained accurately.

Why DSP?

Traditionally signal generation and processing has used analog components. Most of this book involves these techniques. A transistor oscillator can create a signal of good spectral purity. Inductors and capacitors make fine signal filters. Combined with a few transformers and diodes, one has a mixer capable of handling a very wide range of signal levels. The simplicity of this approach has great appeal and for many projects, it is clearly the proper approach. The arguments for putting some portion of the equipment into a DSP process generally are:

- Increased performance in networks such as filters, 90-degree phase-shift networks and banks of filters.
- Better precision in operations such as SSB generation.
- Simpler reproduction of software, relative to hardware.
- The availability of functions that are difficult to implement in hardware, such as adaptive filters.
- The DSP processor likely will have

extra time available for conventional control functions, such as displays or switches.

From a manufacturer's point of view, where a commercial product is involved, much of this can result in lower production costs at high volumes. For the experimenter, producing a project for himself, this can simplify the project as well, assuming that much of the project can be based on existing programs. However, if one must develop the entire program, it may well turn out that the time required is considerably above that of similar hardware.

Arguments in favor of using analog components generally center about the following considerations:

The A/D and D/A conversion processes tend to restrict the dynamic range of the process.

- The bandwidth of the process is too great for a DSP.
- The basic complexity of the DSP is not justified.
- The power consumption is higher than the analog counterparts.
- Programs and debugging of programs requires new skills.

As with any other technology, one must weigh the various considerations and decide if DSP is the best approach to a particular application.

Dynamic Range

In any communications system the lowest level of a signal that can be handled is limited by noise, and some form of overload sets the highest level. The ratio of these two levels, usually expressed in dB is the dynamic range of the system. Systems using DSP have dynamic range limitations, as do analog systems, but the form of noise and overload effects can be quite different. In well-designed systems, the limitations on dynamic range normally come from the conversions to or from analog signals. Internally, the DSP can handle a wide range of signals, because of the resolution of data words and by the use of level shifting algorithms, such as AGC.

For both A/D and D/A converters, noise is introduced by the minimum resolution of the converters. In addition, as will be seen below, some converters may have higher levels of noise associated with the conversion process itself. As converters get faster, they tend to have fewer bits per word with a larger least-significant bit and this represents more noise. This is not always a problem, since a faster converter spreads the noise over a wider frequency range. The noise in a single communications channel may actually be less with the wider bandwidth converter. This is due to

the noise, from the A/D encoding process, being spread over a wider frequency bandwidth and a smaller percentage of this noise hitting within the communications channel.

The EZ-Kit Lite uses the AD1847 CODEC for both the A/D and D/A conversions. This is of the *sigma-delta** type² that is commonly used in DSP applications. The internally generated noise for this conversion process can be considerably greater than that associated with a least-significant bit. **Figure 10.3** is an oscilloscope picture of the noise associated with the A/D converter running with a 48-kHz sample rate and no input signal. The levels were measured by using the DSP to multiply the A/D noise by 100, making it of sufficient level to cover the D/A noise. The RMS A/D noise can be seen to be 153 µV, or about 8 times the level attributable to the least-significant bit. This effectively limits the useful bits to 16–3 or 13.

The corresponding D/A noise, shown in **Fig 10.4**, has an rms level of about 200 µV, which is slightly greater than the A/D noise. It is more difficult to quantify this since the bandwidth of the noise on the output of the D/A converter is much wider than half the sample rate. The level given

*Sigma-delta A/D converters use low-resolution conversions (usually 1 bit), operating at very high conversion rates. The very high digitizing noise is reduced by digital filtering, which accepts only a small part of the noise frequency spectrum. Further noise reduction comes from feedback loops that are able to shape the noise spectrum to move much of the noise energy to high frequencies allowing it to be removed by the digital filters. Similar processes are used to reduce the noise in the sigma-delta D/A converters.

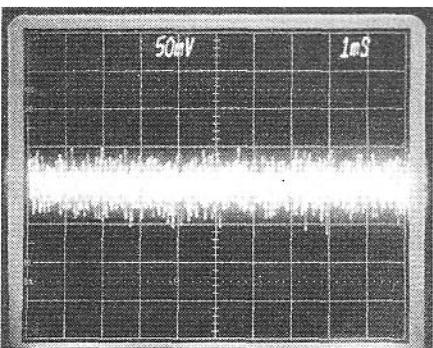


Fig 10.3—Oscilloscope trace of the A/D converter noise in the EZ-Kit Lite. There was no input signal to the converter and the DSP was used to amplify the noise by 100. This was then applied to the D/A converter to produce the trace shown. Each vertical division is 50 millivolts and each horizontal division is 1 millisecond.

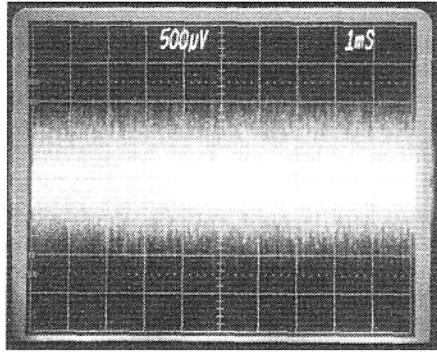


Fig 10.4—Oscilloscope trace of the D/A converter noise in the EZ-Kit Lite. No signal was driving the converter and the oscilloscope bandwidth had been limited to 30 kHz. Each vertical division is 500 μ V and each horizontal division is 1 mS.

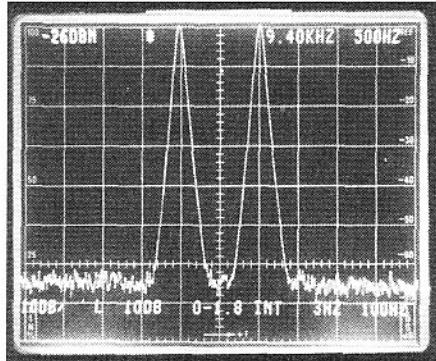


Fig 10.5—D/A output spectrum for two sine waves at 8.9 and 9.9 kHz. Each signal was 2.0 V p-p so that the peak level for both sine waves was 4.0 V p-p, which is full scale for the D/A converter. The noise floor, which is about 65 dB below each of the sine waves, is mainly from the spectrum analyzer.

above was estimated by placing an RC low-pass filter, down 3 dB at 30 kHz, on the output of the converter. This limited the noise to roughly the band of interest (24 kHz for a 48-kHz sample rate).

It is often desirable that the noise associated with the analog processes prior to the digital hardware be amplified until it is somewhat stronger than this “digital” noise. However, doing this reduces the total dynamic range. These are the same tradeoffs between overload prevention and signal sensitivity that have always existed in analog signal design.

The number of bits of the A/D converter limits the top end of dynamic range. Depending on the type of converter, this may result in abrupt compression or it may generate erroneous values. Although this latter form of distortion can obliterate the ability to receive a signal, either effect is a severe form of distortion.

Intermodulation distortion in analog equipment is usually dominated by the third and fifth order products (see Chapter 2). This is due to the gradual nature of the non-linearities of analog components. In contrast, the digital process distorts an

input signal by quantizing it into a series of small steps. On a detailed scale, these input/output characteristics do not appear at all linear. However, as long as the input signals are within the range of the digital words, the process, on a large scale, is often very linear. This results in the small step non-linearities dominating and the resulting intermodulation distortion being spread over a very large number of products, in a noise-like fashion. The term intermodulation ceases to be a good descriptor. As an example, **Fig 10.5** shows the spectrum of two sine waves produced by DSP computation and converted to analog signals by the AD1847 CODEC. No conventional intermodulation products are observable, although the sine waves are using the full available range of the D/A converter. Although mostly obscured by the spectrum-analyzer noise floor, if it could be seen, the distortion product from the two signals would appear to be similar noise.

In contrast to analog circuit distortions, the overload point of the digital signal is abrupt and creates severe distortions. Depending on the nature of the computation, either the signal output will reach a maximum value and not go any further, or even worse, it may wrap around between the greatest positive and the most negative values. In DSP processors, such as the ADSP2181, this choice of overload responses is programmable. Never-the-less consideration must be taken to avoid problems from operating in these signal regions.

10.2 A PROGRAM SHELL

We now need to digress from the signal processing subject to gain a general understanding of the process of programming a DSP microprocessor. The details shown here are specific to the EZ-Kit, but all DSP microprocessor environments have a corresponding process.

The EZ-Kit Lite requires sizeable amounts of programming before it can be used for even the most trivial DSP function. Much of this is associated with programming the CODEC that provides the A/D and D/A conversions. An example of this is setting the sample rate to 48 kHz as is used in the example programs. It is important that these hardware initialization chores be performed correctly, but most often the DSP programmer need not be concerned about the details involved.

For this reason, the EZ-Kit manufacturer provides a program shell. This is a computer program that does almost no useful work other than to pass data through unchanged. It provides a place where a DSP function can be placed to create a useful program.

Fig 10.6 shows the overall flow of the shell, which is the same for any of the programs in this book. When first started, the program initializes the parameters of the hardware and software. This is only done once, although the program may continue to operate for days, months or longer. Following initialization, the program goes into a continual loop. In the figure, this loop is referred to as a background process.

The operations in the background process loop can range from no process to a

complicated mathematical computation, such as a Fast Fourier Transform. As much processing as possible should be put here. The only requirement for being part of the background is that the processing does not require periodic computations at precise time intervals. Examples of background processes would be the reading of a switch or the outputting of data to a controlling PC. These operations need to be done quite often, but the exact times are not critical.

Computations that must be done periodically are handled by interrupts. The interrupt is a signal sent to the DSP to request special processing. In our case, the reason for the interrupt is that another 1/48,000 second (about 20.8 μ s) has elapsed. The specific hardware that generates the interrupt is the CODEC. Typical of

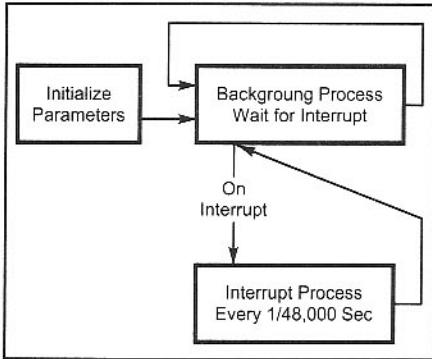


Fig 10.6—Main flow of the DSP programs. To give some feel for the numbers involved, the interrupt rate is shown as 48,000 per second. Depending on the application, this rate might range from 6,000 to 100,000 interrupts per second.

the types of process that must be done periodically are the reading of the A/D data, the computational update of a digital filter, or the outputting of data to the D/A converter. If any of these events do not occur on their precise, periodic schedule, there will be considerable distortion in the signal waveforms coming from the processor.

When the processor receives an interrupt, the background program instruction in progress is completed and the program then “jumps” to the location assigned for processing the interrupt. After the interrupt processing is completed, the program jumps back to the next place in the background process and continues with the background computations. This leaves a maximum amount of time for background processing, while still guaranteeing that the periodic needs will always be met. Recall that the basic processor can execute 33 million instructions per second, much faster than the 48-kHz rate of jumping to an interrupt routine.*

Several things can go wrong when the program is jumping to different places in the program at seemingly random times, however. The interrupt process could take longer than 20.8 microseconds, in which case the next interrupt would arrive before the first processing was complete. Called an *interrupt overrun*, this results in only partial completion of the interrupt process

with very detrimental results. The program must be designed to keep all processing sufficiently short to prevent this. In addition, the background will generally be using a variety of computational registers. If the interrupt routine changes these registers, there will be errors in the resultant data in the background process. The interrupt routines must make sure that any register that it uses is restored before the background process resumes. In the case of the Analog Devices ADSP-2100 series of processors, this is very easily done for one interrupt. All of the computational registers are duplicated and they can be changed by the single instruction `ena sec_reg` or `dis sec_reg`. As one might surmise from the instructions, the two register banks are referred to as primary and secondary.

Programming within the Shell

No attempt will be made here to go through all the details of the shell program. A copy is included on the CD-ROM as `SHLPRG.DSP`. Comments have been added to the original Analog Devices program which explain most of the operation. Although it is not necessary to know all the details of this code, it is instructive to see a few lines of the program to understand the overall structure of a DSP program.

For those that have not yet written a DSP program, this programming information may seem mysterious and difficult to follow. It may be useful for the reader to skim through this section and the following one on “autobuffering”, with the idea of returning when it is time to actually put a program together. The concepts here are important for making the DSP program, but not necessary for seeing how DSP fits into the “bag of tricks” for improving our communications circuitry.

When the DSP program first runs, a number of hardware and software parameters are initialized. In the program this looks like:

```

start: imask=0; { Turn off all interrupts }
        call init0; { Instructions that
                      simulate easily }
        call init1; { And those that do not }

```

The first instruction is to prevent an interrupt from occurring in the program operation, before the initialization is complete. The two subroutine calls, “call init0” and “call init1” do the initialization. Two calls are used as a convenience when testing the programs using the emulator program provided with the EZ-Kit Lite.

Certain items, such as hardware interrupts, require extra effort for simulation but can be omitted for much program testing. When this is the case, the call to `init1` can be “commented” out of the program.

For our shell program the background process is particularly simple:

```

again: { We have no background
        process. If we did, it would go here.}
        jump again; { Go round and round
                      forever }

```

This starts with a label “again:” that is not an instruction, but merely a name for the location in memory where the actual instruction `jump again` is located. The net result of this is that the instruction is executed repeatedly. This does nothing useful, but does allow the program to wait for an interrupt to occur. When this happens, the operation of the program is transferred to the interrupt routine. The return from the interrupt routine will once again go back to the “jump again” loop.

The interrupt routine, often called an “ISR” for interrupt service routine, is again simple:

```

input_samples:
ena sec_reg; { use secondary
               register bank }

mr0=dm(rx_buf+1); { Get left audio
                     from A/D }
mr1=dm(rx_buf+2); { Right }

{ This shell does no processing
  to the signals, other than to pass
  them through. Processing would go
  here. }

dm(tx_buf+1) = mr0; { Send left audio
                     to D/A }
dm(tx_buf+2) = mr1; { Right audio}
dis sec_reg; { Back to primary
               registerbank }
rti; { This undoes the interrupt }

```

The first instruction switches all computational registers to the secondary set. All computation will be performed using the values in the secondary register set, while the primary register set is fully preserved for future use. The next instruction, `mr0=dm(rx_buf+1)`, uses the computational register, `mr0` as temporary storage for the number that was in memory at the address `rx_buf+1`. This is the data from the A/D for the left channel signal. Then, `mr1` is loaded with the data from the A/D for the right channel signal.

*The ratio of the instruction rate and the interrupt rate determines the maximum number of instructions allowed in the interrupt routine. For our case, this is $33,000,000/48,000$ or 687 instructions. Of course, if the interrupt routine always used this maximum number, there would be no time left for the background process. The balance between the two processes is part of the design process.

To make a more useful program, we could now perform some signal processing action on one or both of these signals. However, since this is only an "empty" shell we will just send the data to the D/A converters for both the left and right signals. Putting the numbers back in memory at the addresses `tx_buf+1` and `tx_buf+2` does this. The primary registers are then brought back as the active computational registers and the processing is restored to the background process by the `rti` instruction.

Autobuffering

A potentially puzzling question is "who put the data into memory at `dm(rx_buf+1)` and who is taking it back out from `dm(tx_buf+1)`?" There is specialized hardware, called *autobuffering*, built into the processor that is able to exchange data between a serial port and data memory. The address in memory where this occurs is set up as part of the initialization process. These memory address were given

the symbolic names `rx_buf` for incoming data and `tx_buf` for outgoing data. Left channel data is located 1 address location past the start of the data areas, referred to as `rx_buf + 1` and the right channel data is 2 address locations past the start of the data area. The transfer of the data takes place without any processor instructions being required.

Every 1/48,000 second the CODEC, which includes the A/D, initiates a serial data transfer that is handled through the autobuffering. The completion of this transfer causes an interrupt in the DSP. This, in turn, causes the background activity to be stopped and our interrupt processing to begin.

The interrupt routine is in program memory at the symbolic address `input_samples`. This address is jumped to at the time of the interrupt as the result of a table of instructions that is placed in the first 48 instructions of program memory. These mini-programs are each 4 instructions long and the one used for the serial port used with the CODEC looks like:

```
jump input_samples {14: SPORT0 rx }
rti;           { Three filler instructions }
rti;           { so that there are a total of 4 }
rti;
```

The jump instruction is all that is needed for our shell program and so the remaining three instructions are filled out with do-nothing instructions, in this case they are `rti`, or return-from-interrupt instructions. The particular instruction is not important. The use of `rti` is often intended to prevent problems in case of accidental interrupts, but the utility of this is questionable and the real reason is to comply with a convention!

There are always 11 more interrupt mini-programs, most of which are not used. As can be seen from the full program listing, each serves a particular interrupt, if the interrupt mask enables it. Each of these has a specific address in memory. Our serial-port program is at address 14 hex (20 decimal.)

10.3 DSP COMPONENTS

When a piece of electronic equipment is assembled in a traditional way, a number of components are soldered together. These components can be fundamental ones, such as a resistor or a diode. In some cases, though they will be complex building blocks, such as a phase-locked loop built in an integrated circuit. In the same manner, one can look at DSP functions as components that can replace, or add to the analog components. In the following pages we will explore some of these DSP components, and see how they fit into radio designs.

Amplifiers and Attenuators

As DSP components, amplifiers and attenuators consist of multiplying the signal by a constant. If the constant is greater than 1.0 we have an amplifier and if it is less than 1.0 we have an attenuator. For instance, a 4-dB attenuator could consist of a signed multiplication:

```
my0=20675; { -4 dB as a fraction of
            32768 }
mr=mr1*my0 (ss); { The signal is in
                   mr1 already }
```

It is assumed that the input signal has already been placed in the `mr1`. The instruction `my0=20675` places a constant

into one of the multiplier input registers, called `my0`. The output is called `mr` and for the ADSP-2100 series of processors this is a 40-bit register divided into three parts, called `mr2`, `mr1` and `mr0`. For our case of the multiplication of two 1.15 format signed numbers,* the 16-bit signed result is in the `mr1` register.**

The attenuation value in `my0` is the 1.15 format fraction corresponding to the voltage ratio for -4 dB. In equation form this is:

$$my0 = (\text{int}) \left(32768 \cdot 10.0^{\frac{-A}{20.0}} \right) \quad \text{Eq 10.1}$$

where A is the attenuation value in dB, which in our case is 4.0. The `(int)` operator

*See the sidebar "Decimal numbers in a fixed-point DSP" for a description of the number formats.

**The `mr0` register contains the least-significant 16 bits that are used if we want to work with more than 16 bits. The high 8 bits in the `mr2` register are available for functions that use "multiply and accumulate." This allows one to multiply two numbers together and add the product to a previous result. This is common operation in DSP.

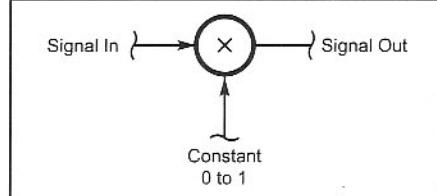


Fig 10.7—DSP attenuator using a multiplier. This multiplication operation occurs for every input signal sample.

indicates that we will use the closest integer to the calculated value. Fig 10.7 shows this attenuator in block diagram form.

This simple arrangement does not work for amplifiers. In 1.15 format, the largest number is 32767/32768, which is slightly less than 1.0. This can be overcome by the use of shifting. For instance, a "voltage" gain of 4.0 (as a ratio), or 12.04 dB, is achieved by shifting the binary number for the signal level to the left by two bits, as illustrated in Fig 10.8. In general, we need better control of gain than can be obtained with powers of 2 and this is achieved by cascading the shifting operation with the attenuation operation. As a more general example, a gain of 3.5, or 10.88 dB, is illustrated in Fig 10.9. In program form this would look like:

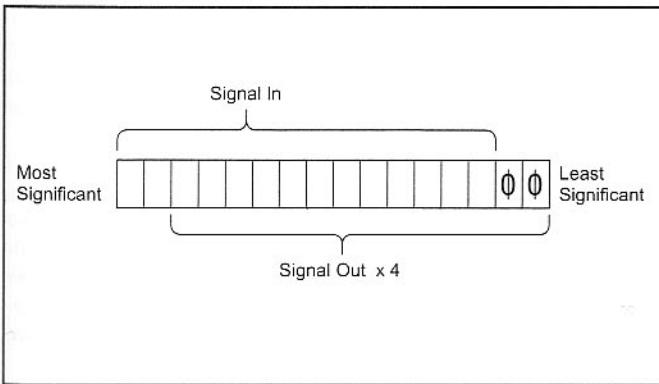


Fig 10.8—DSP gain of 4 using a shift register. The shift operation allows any amount of shifting, either up or down, in a single operation.

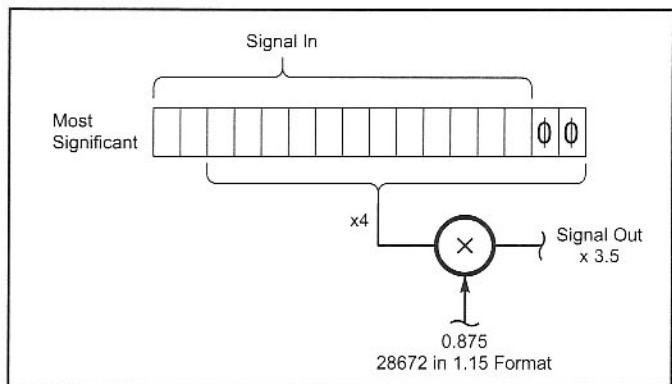


Fig 10.9—DSP gain of 3.5 using a shift register and a multiplier. A gain of 4 is first applied by the shift register, as was done in **Fig 10.8**. Following the shifter, an attenuation of 0.875 is applied, using the multiplier of **Fig 10.7**. This brings the net gain to 3.5.

```
sr=ashift mr1 by 2 (hi);{ The signal is in
mr1; shift 2 bits }
my0=28672; { 0.875 in 1.15 format }
mr=sr1*my0 (ss); { Multiply the shifted
signal by my0 }
```

with the result again in the mr1 register.

The examples shown here are for constant values of attenuation. In many instances, it is necessary to have the gain the result of some calculation. The shift register is useful for this case, allowing the number of bits of shift to depend on a register value. One should take care

that the number of bits of shift is not more than necessary. If a large amount of shift is followed by a large amount of attenuation, there will be a loss of accuracy (dynamic range). The attenuation constant in my0 should be between 0.5 and 1.0.

10.4 SIGNAL GENERATION

Generation of signals using DSP is easily done. The primary advantages are the accuracy of the waveform and its stability over time. DSP signal generators tend to be limited to frequencies in the low MHz range, or less, due primarily to the computational load. Two examples of signal generation, the sine wave and random noise, are shown here.

Sine Wave Generator

One basic component that is needed for many DSP programs is a sine-wave generator. Digital generators can be implemented either as lookup tables or as calculated functions.

Lookup tables consist of a large block of data in memory that has every sine-wave value stored according to the phase angle. In its pure form this could require 65K words of storage for 16 bit phase angles. This is the fastest implementation, but obviously is impractical for many applications, because of the memory needs.

Various schemes allow the reduction of memory usage.³ The most obvious is to use the symmetry of the sine wave and only compute values for a 90-degree segment from 0 to 90 degrees. This reduces the table to a fourth of the original size in exchange for a few computer instructions.

Other methods reduce the table size further by approximating the output waveform. This can be done as a series of steps where the output does not change, although the input phase does; this has very little computational overhead. More exact results are obtained by approximating the sine wave with a series of straight lines connecting the lookup-table values, but with higher computational overhead.

At the other extreme is direct calculation of the function.⁴ This uses very little

memory, but each data point requires, for our example, about 27 DSP machine cycles. This is quite acceptable for many applications. In terms of computing time, each data point takes $27 \times .03 = 0.81$ microseconds on the ADSP-2181. The method again starts by dividing the sine wave into four regions of 90 degrees each as shown in **Fig 10.10**. For any point between 0 and 90 degrees, the sine wave is approximated by the following polynomial equation.⁵

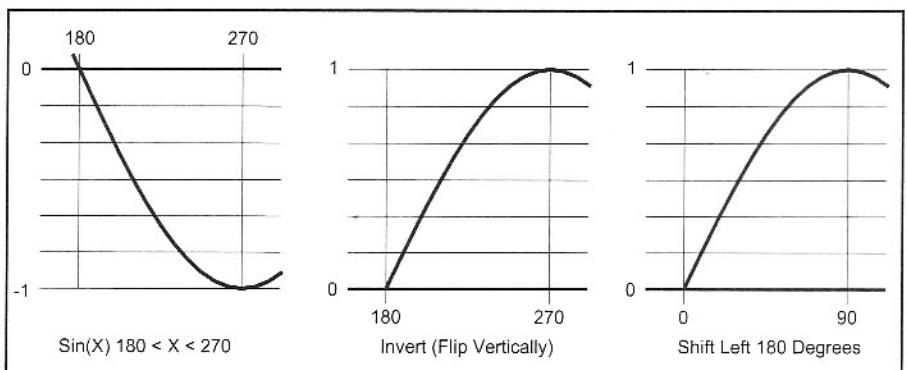


Fig 10.10—The values of sin(x) between 180 and 270 degrees are seen to be the same as those from 0 to 90 degrees, after the curve has flipped vertically and shifted 180 degrees. This symmetry allows the values from 0 to 90 degrees to be the only ones that need be calculated.

$$\begin{aligned}\sin(x) = & 3.140625x + 0.02026367x^2 \\ & - 5.325196x^3 + 0.5446778x^4 \\ & + 1.800293x^5\end{aligned}$$

Eq 10.2

where x is the angle in degrees divided by 180. In the fixed point processing of the DSP (see the sidebar), the equation requires integer coefficients and takes the form

$$\begin{aligned}\sin(X) = & 12864X + 83X^2 - 21812X^3 \\ & + 2231X^4 + 7374X^5\end{aligned}\quad \text{Eq 10.3}$$

Two items are being dealt with in creating this equation. First, the coefficients have been scaled up to be 16-digit integers. But, in addition, they have been scaled back by a factor of 8 to insure that overload does not occur when the DSP calculation is only partially completed.

The calculation of the sine-wave value by these equations is valid only for 0 to 90 degrees. In fixed-point values this corresponds to 0 to $65536/4$, or 0 to 16384. To deal with all possible angles from 0 to 360 degrees, the values are corrected according to the symmetry rules, such as those given above.

The five coefficients for the calculation of the polynomial are kept in a program-memory table called `sin_coeff`. Access to this table is discussed below, and is initialized in the first two lines of the `sin` routine.

The next four lines are to divide the input data into four 90-degree segments. Note that the program constants are given as hexadecimal numbers. This requires a bit of translation to the more familiar decimal numbers. Many hand-held calculators have this translation, making the task simpler. In the program instruction `my1=ar`, both of these computational registers will have a value that is somewhere between 0 and 16383 decimal, or 0000 to 3FFF hexadecimal. This is the input value to the polynomial calculation.

The instruction `mf=ar*my1 (RND)`, `mx1=pm(i4,m4)`; indicates that the `mf` register will be hold the results of the rounded multiplication of the `ar` and `my1` registers, and that the `mx1` register will be loaded with the first polynomial coefficient that was in program memory (`pm`). The comma shows that both halves of this computation occur simultaneously, i.e., this is a single instruction. Not all instructions can be combined this way, but when it is possible, there is quite a bit of savings in processor time. The register `mf` now contains the input value squared.

Next `mr=mx1*my1 (SS)`, `mx1=pm(i4,`,

`m4)`; multiplies the first coefficient in `mx1` by the input value in `my1`, leaving the product in `mr`, and also loads the second coefficient into `mx1` register, overwriting the first coefficient.

The remainder of the polynomial calculation continues in a similar fashion. For efficiency in program size, the middle three multiplications are put into a loop. The register `cntr` controls the loop and it is automatically decreased with every loop. Loop initialization is performed by the instruction `do approx until ce;`.

After the polynomial is calculated, the value is adjusted according to the 90-degree segment of the input. Finally `rts`; is a subroutine return.

Using The Sine Wave Routine

Incorporation of this routine into the program shell takes only a few instructions. First, we need to initialize the frequency of the sine wave to some value, which for this example will be 1000 Hz. A number called "dphase" is set up in memory:

```
.var/dm dphase; { For generation of
    sine wave }
```

and this is initialized to the nearest integer value to the phase shift that occurs during $1/48,000$ second, given by $1000*65536/48000 = 1365.33$. This is put into data memory by:

```
ax0=1365; { 1000.24 Hz }
dm(dphase)=ax0;
```

The sine wave calculation consists of adding this phase change to the last phase value and using this in our sine wave routine. The program segment that goes into the middle of the ISR looks like:

```
ax1 = dm(dphase); { Phase increment
    for oscillator }
ay1 = dm(phase); { Last phase }
ar = ax1 + ay1; { New phase }
ax0 = ar; { The phase input
    to sin is reg ax0 }
dm(phase) = ar; { Save for next data
    point }
call sin; { Phase in ax0, Sin
    returned in ar }
```

Finally the sine wave is sent to both the left and right D/A:

```
dm(tx_buf+1) = ar; { Send sine wave
    to Left D/A
    (Codec) }
dm(tx_buf+2) = ar; { Right D/A }
```

A sin Routine

The routine for the EZ-KIT Lite looks like the following:

```
sin: m4=1; l4=0;
i4^.sin_coeff;
ay0=H#4000;
ar=ax0, af=ax0 and ay0;
if ne ar=-ax0;
ay0=H#7FFF;
ar=ar and ay0;
my1=ar;
mf=ar*my1 (RND), mx1=pm(i4,m4); { mf = input**2 }
mr=mx1*my1 (SS), mx1=pm(i4,m4); { Start polynomial calculation }
cntr=3;
do approx until ce;
mr=mr+mx1*mf (ss);
approx: mf=ar*mf (rnd), mx1=pm(i4,m4);
mr=mr+mx1*mf (ss);
sr=ashift mr1 by 3 (hi);
sr=sr or lshift mr0 by 3 (lo);
ar=pass sr1;
if lt ar=pass ay0;
af=pass ax0;
if lt ar=-ar;
rts;

{ Use i4,m4 index registers to }
{ point to polynomial coeffs }
{ This is 90 degrees }
{ Check 2nd or 4th quad. }
{ If yes, negate input }
{ This is a mask to replicate data, }
{ while removing the sign bit }

{ More polynomial calculation }
{ Power increase; get next coef}
{ Do last polynomial calculation }
{ Mult *8 (shift left 3) }
{ Convert to 1.15 format }
{ See if result >=1.0 }
{ If so, saturate, i.e. set to 0x7FFF }
{ See if input was negative }
{ If so, negate output}
```

Index Registers

The sin program uses *index registers*, in particular **i4**, along with the modifying registers **m4** and **I4**. These allow access to sequential addresses in memory without having to spend DSP computational time.

In the sine wave calculation, **m4=1** indicates that after the index register **i4** is used, we want to move sequentially to the next higher address. **I4=0** indicates that there is never a wrap-around in the addresses that are generated by adding on the **m4** value. And **I4=^sin_coeff** sets index register 4 to the address of **sin_coeff**, a table in program memory that was loaded with five polynomial coefficients by the assembler directives:

```
.var/pm sin_coeff[5];
.init    sin_coeff: H#324000, H#005300, H#AACC00,
        H#08B700, H#1CCE00;
```

This usage of the index registers is illustrated by the instruction **mx1=pm(i4,m4)**; indicating that the computational register **mx1** will be loaded with the contents of program memory at address **i4**, and then **i4** will have the value **m4** (one) added to it, for use next time. Other values of **m4** can be used, including negative ones, to allow stepping through tables in any equal arrangement.

The ADSP-2100 series of DSP have 8 index regis-

ters, named **i0** to **i7**. The **m0** to **m7** modify registers are used to change the address of the index registers after they are used. With some restrictions, the number of the index register need not be the same as that of the modify register. For instance, **i0** can be modified by **m0**, **m1**, **m2** or **m3**. The length registers always correspond to a particular index register and can be a value such as **I0 = 10** which means that the buffer that starts with the address in **i0** has a length **10**. When the 10th value is either read or written, the address in **i0** will not be incremented again by **m0**. Instead the address will be taken back to the initial value given to **i0**. This is the meaning of a *circular buffer*. If **I0** had been given a value of 0 the DSP would interpret this as a special case with **i0** indexing into a conventional non-circular buffer.

Program memory is 24 bits per instruction. Tables are often stored in program memory, but most often only 16 bits worth of data is used, since this corresponds to the size of most computations and of the data memory words. To make the data line up properly, 8 zero bits must be appended to each table entry stored in program memory. As an example, the first **sin_coeff** entry is the hex number 324000. The last two zeros are the extra 8 bits. Removing these we have the hex number 3240, which converts to a decimal value of 12864, which is the first coefficient of the sine calculation.

We should remember that we have only calculated a series of numbers that represent the sine wave at specific points, as shown in Fig 10.11. Before this is a “clean” sine wave it is necessary that this be converted to a continuous curve. In the case of the EZ-Kit, the low-pass filter to accomplish this is included in the D/A converter of the CODEC. The

need for this conversion becomes more obvious as the frequency of the sine wave increases and fewer points are calculated per cycle.* Fig 10.12 illustrates this for an 8500-Hz sine wave with a 48-kHz sample rate. To a good approximation, this collection of sample points will be converted to a

continuous sine wave by the application of a low-pass filter at half the sample rate, on the output of the D/A converter. If one studies the apparently random collection of data points, it will become apparent that they are indeed sample points along a sine wave with about $48/8.5=5.6$ data points per cycle.

* See chapter 4, section 4.7, for further discussion of hardware DDS computations. The process is identical, except that in the DSP case, one may need to use the sine-wave for internal functions such as driving a software mixer instead of always driving a D/A converter to produce an analog output signal.

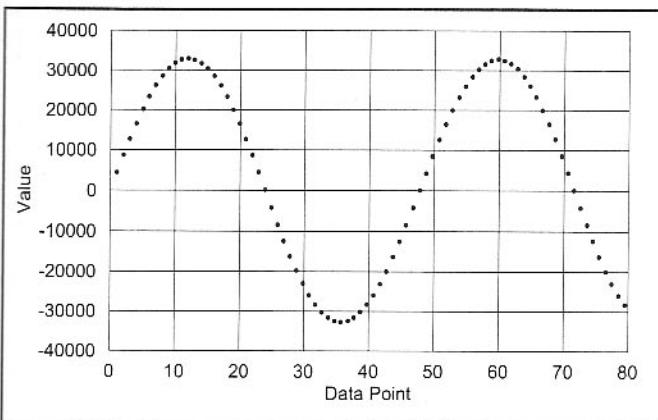


Fig 10.11—Calculated points for a 1000-Hz sine wave sampled at 48 kHz. The ability of these points to be smoothed to a continuous sine-wave curve is readily apparent.

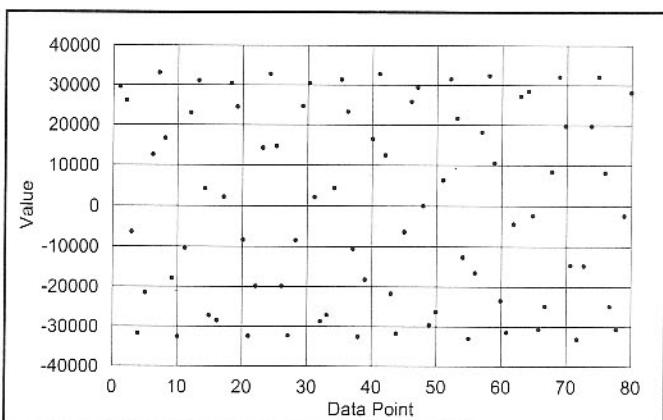


Fig 10.12—Calculated points for a 8500 Hz sine wave. The sample rate is identical with that of Fig 10.11. Careful study will show that these are indeed sample points on a sine wave. The ability of the low-pass filter to connect these points into a smooth curve is not so obvious, yet the resulting sine wave is exact.

10.5 RANDOM NOISE GENERATION

For the testing of transmitters and receivers it is often useful to have a noise-like signal. In the area of modulation and coding, interesting experiments can be performed by using a controlled noise source. A simple example is to add Morse code to the noise and test various filters and signal processors for the accuracy of copy by an operator.

One feature of a digital computer is the

total predictability of computational results. This seems inconsistent with generating noise, and in a philosophical sense, it is! However, in a practical sense, the noise generator can be made to have a repetition period long enough that it is functionally random. For instance, the noise generator that will be described here repeats its pattern in about 25 hours running in the EZ-Kit Lite. Within that

period, the output seems "noise-like" by most measures, although each successive output is totally determined by the previous output.

One algorithm, called the linear congruence method,^{6,7} produces most of the computer-generated random numbers of the world. Three constants must be selected for this method, and large amounts of study have gone into the rules for selecting

Decimal Numbers in a Fixed Point DSP

The fixed point DSP use an arithmetic system called 2's Complement.* In this system, positive numbers start at zero, represented by all binary bits being zeros, and progress to larger values by adding 1 to the next lower number. This progresses until all of the bits are 1, except for the farthest left bit that is always a zero for positive numbers. In the simple case of a three-bit system, the positive values would be

011 binary	3 decimal
010 binary	2 decimal
001 binary	1 decimal
000 binary	0 decimal

The 2's complement negative numbers are created by interchanging all binary values, bit-by-bit, and then adding 1 while saving the right-hand three bits. For instance, the decimal value +2 is 010 and if we interchange the binary values, we have 101. Adding 1 to this yields 110, which represents the decimal value -2. The same two operations will also bring us back to +2 indicating consistency. Applying this rule to the four values above produces the following table for the negative values:

000 binary	-0 decimal
111 binary	-1 decimal
110 binary	-2 decimal
101 binary	-3 decimal

The values for -0 and +0 are the same, which fits our idea of "nothing!" And the three true negative values all have a leading one, which is consistent with the positive values having a leading zero. However, the binary value of 100 does not appear in either table. Since it has a leading one, indicating a negative number, and it fits in the binary sequence either below -3 or above +3, it will be assigned the decimal value of -4. It does not follow the 2's complement rules for negation, since it produces the same 100 value. The last table entry is thus:

100 binary	-4 decimal
------------	------------

Now, the operations of addition can be performed by following the same rules that we have in the decimal system, except that a *carry* will be generated when the

result exceeds 1 instead of when it exceeds 9. For the binary system this occurs when we add 1+1. That is:

$$\begin{array}{l} 0 + 0 = 0 \text{ No Carry} \\ 0 + 1 = 1 \text{ No Carry} \\ 1 + 1 = 0 \text{ Carry Generated} \end{array}$$

When there are multiple places in addition, the carry is added as a 1 in to the next position to the left.

So, for our 3-bit example, decimal values 1 plus 2 is

$$\begin{array}{r} 001 \\ +010 \\ \hline 011 \end{array}$$

or decimal 3. This applies equally well to negative numbers and extends to subtraction, which starts to explain the wide use of 2's complement arithmetic systems in binary computers!

Our 3-bit example shows the operation of the number system, but it does not convey a feel for working with numbers in a 16-bit DSP system. The following table shows a few of the decimal values, and their binary representations for the larger number system:

Largest positive number	
0111 1111 1111 1111 binary	+32767 decimal
-----	-----
0000 0000 0000 0111 binary	+7 decimal
-----	-----
0000 0000 0000 0010 binary	+2 decimal
0000 0000 0000 0001 binary	+1 decimal
0000 0000 0000 0000 binary	+0 decimal
1111 1111 1111 1111 binary	-1 decimal
1111 1111 1111 1110 binary	-2 decimal
-----	-----
1111 1111 1111 1001 binary	-7 decimal
-----	-----
1000 0000 0000 0000 binary	-32768 decimal

In *fixed-point arithmetic*, the standard way to use this arithmetic system to represent decimal numbers is to divide the number value by some power of 2. For instance, if all the values are divided by 32768 (2 to the 15th power) the table looks like: (see top of next page)

In this case, the last column is the *fractional representation* of these same 2's complement numbers. The

* Processors, such as the ADSP-2181 allow for either "Unsigned" arithmetic, or for "Signed 2's complement arithmetic." Because of its greater generality, only the latter type is considered here. See Reference 4 for details of unsigned arithmetic.

these constants, as can be read about in the references. From the point-of-view of the noise-generator user, it is usually sufficient to borrow upon others study of these constants and apply them. This generator comes from the formula

$$v(n+1) = (av(n) + c) \bmod m$$

where

$v(n+1)$ = current generator output
 $v(n)$ = last generator output

a, c, m are constants
 $\bmod m$ means dividing by m and taking only the remainder.

The constants are carefully chosen not only to produce good random numbers, but also to simplify the computation using our fixed-point processor. One good set is

a = 1664525
c = 32767

$$m = 2^{32} = 4,294,967,296$$

The length of time before the random noise repeats is determined by m. The value used here is the largest that can be used with a 32-bit word size. This requires double precision calculations, but if we restricted our calculation to 16 bits, the result would repeat $2^{16} = 65536$ times faster, or about every 1.36 seconds. For some purposes, this could cause strange results.

Largest positive number	0111 1111 1111 1111 binary 0000 0000 0000 0111 binary 0000 0000 0000 0000 binary 1111 1111 1111 1111 binary 1111 1111 1111 1001 binary	Fractional 32767 / 32768 = 0.99997 7 / 32768 = 0.00021 0 / 32768 = 0.0 (65535-65536) / 32768 = -0.00003 (65529-65536) / 32768 = -0.00021 (32768-65536) / 32768 = -1.00000
Most negative value	1000 0000 0000 0000 binary	

total range is from -1.0 to almost 1.0. With 16 bits available, the step size (the fractional value of the least-significant bit) is 1/32768 or about 0.00003.

Sometimes the range of numbers being represented do not lie between -1 and +1. This is handled by dividing the binary representations by some other power of 2 than 32768. If the numbers were between -8.0 and 8.0 the divisor would be 4096 (2 to the 12th power.) The price paid for this is the resolution step size is now 1 / 4096 or about 0.00024.

Note that the divisors such as 32768 or 4096 are only implied, and not carried in any way with the 2's complement numbers. When writing a DSP program it is necessary to keep track of the number form. If a subroutine is expecting numbers in one format and they arrive in a different one, erroneous results will occur. Comments in the DSP program should carry the format information.

The notation describing the divisor value is not consistent in all literature. Often times a divisor of 32768 is called Q15 notation, since there are 15 bits to the right of the implied decimal point. The divisor of 4096 would be Q12. In their literature, Analog Devices uses the terminology 1.15 for Q15, 4.12 for Q12 and so forth. In this book we will continue this notation.

Addition is the operation for which 2's complement arithmetic fits perfectly. So long as the implied decimal points are the same for two numbers, they can be added without regard for their sign. As long as there are enough bits for the result, it will be correct. However, if there is not sufficient room for the result, bad things happen. For instance if we add the decimal representations of 15,000 and 20,000 together, one would expect to get 35,000. However, this is larger than can be represented with 15 bits, which is 32767. This will result in generating a carry bit that hits, of all places, in the sign bit. If we proceed blindly ahead we will have the erroneous negative value 35000-65536=-30536. This is called wrap around.

DSP program writers must take steps to prevent wrap around from occurring. In many cases, the DSP microprocessor can cause the results of computations to go to maximum positive or negative values in the case of overflow, preventing wrap around. In other

cases, a formal check of the numerical values is required with appropriate adjustment of the data.

Multiplication of numbers occurs frequently in DSP programs. The sign bit adds an extra complexity to this operation. For instance, 3 times 2 would seem to produce the following, in binary signed 1.3 format numbers:

$$\begin{array}{r} 0010 \text{ Signed 2} \\ \times 0011 \text{ Signed 3} \\ \hline 0010 \\ 0010 \\ 0000 \\ \hline 0000110 \text{ Signed 6} \end{array}$$

But this is not what is found if one operates a DSP microprocessor. Instead, the result will be shifted one bit to the left and the result, in binary, is 00001100 that would seem to be 12 in decimal. The DSP signed multiplier has been built to acknowledge that each number being multiplied has a sign bit, but the result doesn't need two sign bits. Thus all results of signed multiplies are shifted left.

This all sounds somewhat arbitrary until it is seen that if there is an implied decimal point in the numbers, it will move one position to the right with each multiply, unless the shifting of one bit occurs. Dividing the numbers in the previous example by 8 turns them into Q1.3 format numbers. Doing the example again with Q1.3 format and the decimal point shown results in:

$$\begin{array}{r} 0.010 \text{ or Signed 2/8} \\ \times 0.011 \text{ or Signed 3/8} \\ \hline 0010 \\ 0010 \\ 0000 \\ \hline 0.000110 \text{ or Signed 6/64} \end{array}$$

Notice that only 6 places are needed to the right of the decimal point. Along with a single sign bit, 7 bits are required.

The generator, in DSP code is:

```

my1=25;           { Upper half of a (1664525/65536) }
my0=26125;        { Lower half of a, the remainder }
mr=sr0*my1(uu);  { 32 bit multiply: a(hi)*v(lo) }
mr=mr+sr1*my0(uu); { and a(hi)*v(lo)+a(lo)*v(hi) }
si=mr1;          { Temp storage to free mr1 }
mr1=mr0;          { LS Word of a*v(mid) }
mr2=si;           { 8 bits of
mr0=h#ffffe;      { c=32767, left-shifted by 1 }
mr=mr+sr0*my0(uu); { (above) + a(lo)*v(lo)+c }
sr=ashift mr2 by 15 (hi);
sr=sr or lshift mr1 by -1 (hi); { Right-shift by 1 }
sr=sr or lshift mr0 by -1 (lo); { Now have uniform rn in sr1

```

This program from the Analog Devices library⁸ is an example of a routine that is carefully tuned for a particular application. In order to make the repeat period very long, the random number is generated as a 32-bit unsigned number. The constant multiplier, a, is 21 bits long and so the product can be up to $32+21=53$ bits. The final operation of the algorithm, as shown above, is to divide by 232 and then take the 32-bit remainder. At this point the top 32 bits will be discarded. The program does this, in part, by never generating that part of the product at all. If one examines the construction of a 64-bit product from two 32-bit numbers (using a 16 bit processor) it is seen that there are four terms to be added together. The product of the high-order 16 bits of v, with the high-order 16 bits, need never be produced.

The choice of m as a power of 2 is a common trick to avoid explicit division. A right shift of the data equal to the value of the exponent is all that is needed.

Selecting the desired words does a shift of 32 bits. This makes the three shifts at the end of the listing a surprise, at first. These three shifts are really only a shift of 1 bit corresponding to a division by 2. It is needed to correct for the shift in the multiplier result for unsigned multiplies, as discussed in the Decimal Number sidebar.

The resulting random numbers, left in the sr1 register, are equally likely to be anywhere between 0 and 65535, the full range of a 16-bit number. This is referred to as a Uniform Random Number.

Gaussian Random Numbers

What we have from the Uniform random number generator is not quite the noise that occurs in receivers, called Gaussian noise. Gaussian noise can take any value, but with decreasing probability as the magnitude of the value gets greater, as illustrated in Fig 10.13. There are several ways to convert our random numbers into Gaussian noise, all of which must be

approximations. There is always some overload point in real hardware, and Gaussian noise does not allow this! Fortunately, the probability of achieving these levels is very small, and as a practical matter can generally be ignored.

One simple way to generate Gaussian noise is to simply add several of the outputs of our uniform random number generator together. This is well founded on a mathematical principle known as the Central Limit Theorem.⁹ The more numbers we add together, the better the approximation becomes. This is done in DSP by a loop (see box at bottom of page).

Most of the instructions in the loop are to free up the shift register for the division by 8. The division is needed to prevent overflow when 8 numbers are added together. One subtle operation is the use of an arithmetic shift (rather than a logical shift) to divide by 8. Doing this implies that the random number that ranged between 0 and 65536 is now being treated as a signed number ranging between -32768 and 32767. In fractional, 1.15 format this corresponds to numbers between -1.0 and 0.99997.

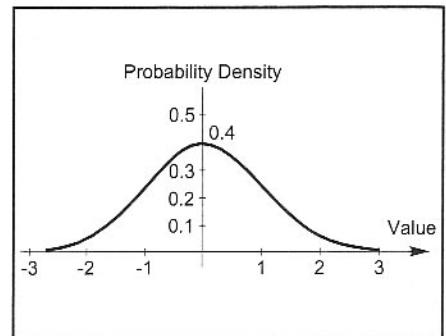


Fig 10.13—Gaussian noise probability curve, showing relative probability of being in the vicinity of any value. The curve extends forever on either side of the graph, but the probability of achieving these values rapidly becomes insignificant.

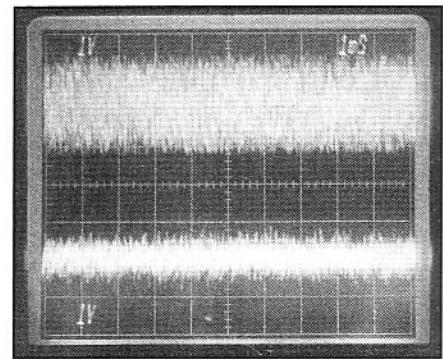


Fig 10.14—Oscilloscope picture of random noise as generated by the listings in the text. The upper trace is uniform random noise and the lower trace is Gaussian.

Program For Generating Random Gaussian Noise From 8 Uniform Noise Samples

```

getrnd:
    my1=25;           { Upper half of a (1664525/65536) }
    my0=26125;        { Lower half of a, the remainder }
    af=pass 0;         { Clear the arithmetic accumulator }
    cntr=8;            { The number of uniform rn added }
    { Now loop 8 times to generate a noise sample: }
    do randloop until ce;
    sr1=dm(seed_msw); { Decrease cntr until 0 }
    sr0=dm(seed_lsw); { Get the 32 bit seed from last }
    { call to this fcn or last loop }
    { The Random Number Generator, shown above, goes here,
    leaving the result in the sr0 and sr1 registers }
    dm(seed_msw)=sr1; { Save new seed, high 16 bits }
    dm(seed_lsw)=sr0; { and low 16 }
    { Uniform random number still in sr1. Add to accumulator: }
    sr=ashift sr1 by -3 (hi); { Divide by 8, ie, shift right 3 }
    randloop: af=sr1+af; { Accumulate 8 uniform rn }
    rts;                 { Random 16-bit value in af }

```

One of the advantages of the DSP approach of noise generation is the ability to know the noise power precisely.* This is found by considering the process used to generate the noise samples:

- 1/3 is the average power for -1.0 to $+1.0$ uniform random numbers.

*The normalized values of numbers range from -1.0 to 0.99997 , which can be thought of as voltages. In order to think about power in the DSP computation we must square the voltage and divide by the "resistance." For simplicity, the resistance value is chosen to be $1\ \Omega$ and the power is just the normalized value squared.

$+1.0$ uniform random numbers.

- This is diminished in power by $(1/8)^2 = 1/64$ for the shift by 3 bits.
- This is increased by 8 for adding the 8 numbers together.

• The final result is a total noise power of $1/(8 \times 3) = 0.04167\text{ W}$.

The process of combining the 8 uniform random numbers has reduced the power from 0.333 to 0.04167 , but the maximum possible values have been kept at -1 and $+1$. We are increasing the peak-to-average ratio, a necessary operation if a Gaussian approximation is to result.

The generation of each Gaussian noise value by this method requires 134 instruction cycles, or about 4 microseconds of EZ-Kit Lite processor time.

Fig 10.14 is an oscilloscope plot showing both the uniform random numbers before scaling (top) and the Gaussian noise, both to the same scale. It can be seen that the Gaussian noise clusters about the center value, much more than the uniform generator. It is not so obvious that the attainable peak values are the same for both plots. The Gaussian generator produces these peak values very infrequently!

10.6 FILTERING COMPONENTS

After A/D encoding of an analog waveform, such as an audio or an IF signal, we can then apply frequency selective filtering to the waveform. Such filters, called *digital filters* can be implemented in DSP with all the conventional passband shapes such as Low-Pass, High-Pass and Band-Pass. The input to the filter consists of a sequence of numbers representing successive samples of a voltage. Each sample period the filter performs some calculations on the new sample. This involves values that were previous samples and in some cases the results of the previous calculations. By carefully designing this calculation it is possible to make its output level very sensitive to the frequency of the input, which is what we mean by frequency domain filtering.

There are two basic ways to implement a digital filter, called IIR and FIR filters. The distinction in the arrangement of the calculation is not great. The IIR filters involve the results of previous calculations and FIR filters do not. Never the less, this small difference has major influences on both the design and the operation of the filter.

output of a properly designed filter will get smaller with time and eventually become smaller than the smallest number our processor can recognize. The simplest IIR filter is the analog of the RC low-pass filter shown in **Fig 10.15**. The digital

implementation consists of adding a small fraction of the new input to a fraction of the last filter output. If we call the filter input sample x_i and the filter output sample y_i then our filter consists of the single calculation:

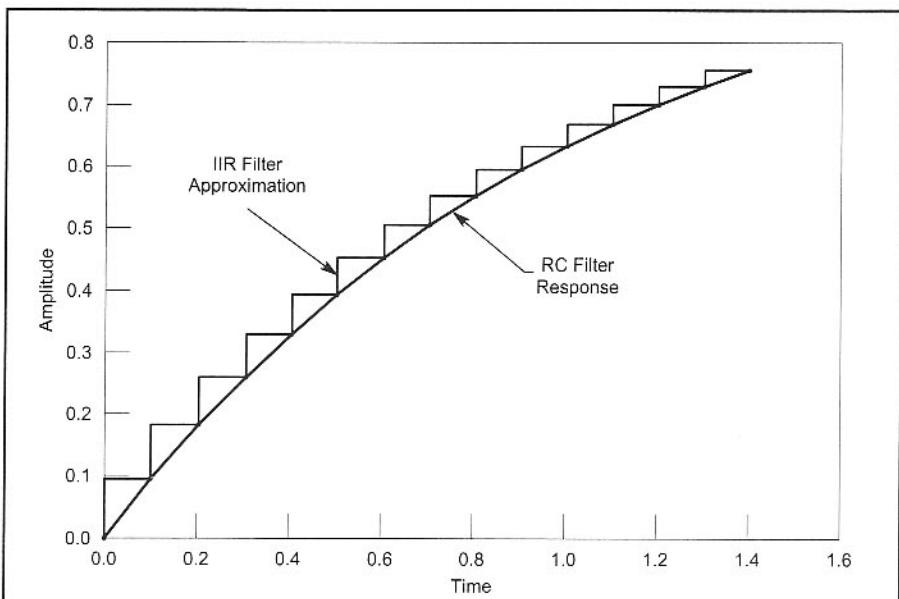


Fig 10.16—The charging response for the RC filter and the IIR filter approximation.

IIR Filters

IIR stands for Infinite Impulse Response and refers to the fact that, in principle, the output of the filter continues forever after an input has been removed. In actuality it does not, of course, since the

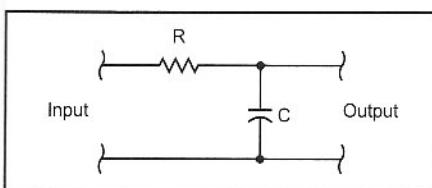


Fig 10.15—Simple RC low pass filter in analog form.

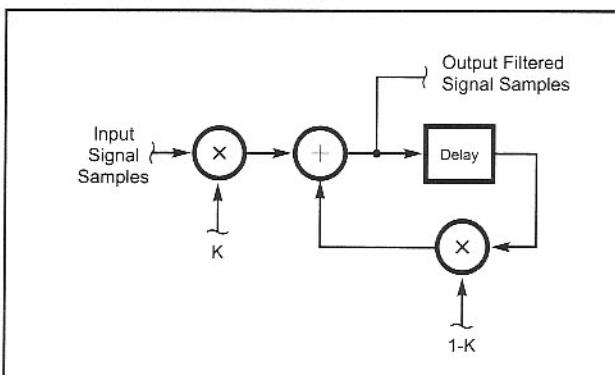


Fig 10.17—Block diagram of the simple IIR filter that has the response of an analog RC low-pass filter. The output signal is delayed by a sample period and a fraction of this is fed back to be summed. This use of feedback is characteristic of IIR filters.

$$y_i = K x_i + (1-K) y_{i-1} \quad \text{Eq 10.4}$$

where K is between 0 and 1, typically 0.001 or less. **Figure 10.17** is a block diagram of this filter. Operation of this simple filter can be calculated for the first few terms while the input rises from 0 to 1. We assume that the output is 0 when we start and that $K=0.1$ (this big value for K makes things happen faster for our example):

New Input, x_i	$K x_i$	$(1-K) y_{i-1}$	New Output, y_i
0.0	0.0	0.0	0.0
1.0	0.1	0.0	0.1
1.0	0.1	0.09	0.19
1.0	0.1	0.171	0.271
1.0	0.1	0.2439	0.3439

It can be seen that the output is growing towards 1.0, but with smaller steps with each new input. This is the same exponential growth that we associate with the RC filter. **Fig 10.16** shows both the charging characteristics of the RC filter and our digital equivalent. If we allow the process to continue for a very long time, the output will achieve a value of essentially 1.0. At that point the response is as follows:

New Input, x_i	$K x_i$	$(1-K) y_{i-1}$	New Output, y_i
1.0	0.1	0.9	1.0
1.0	0.1	0.9	1.0

Notice that if the input and output are the same there is no change in the output, as would be expected for the RC filter. RC filters are characterized by their time constant, T , in seconds that is equal to the product of the resistance and the capacitance. This is the time for the capacitor to charge to 63% of its final value. Design of the equivalent digital filter involves choosing the value K according to:

$$K = 1 / [0.5 + (T / T_s)] \quad \text{Eq 10.5}$$

where T_s is the time between successive input samples.

The RC IIR filter, implemented in DSP assembly language, is shown in the box to the right.

Notice that in conventional 16-bit representation of signed decimal numbers the value 32768 (or 2^{15}) would be 1.0 if it was not the wrap-around point and therefore 32768 represents -1.0. This is why it is used for the calculation of $1.0 - K$. For example, if the value for K in the DSP program is 5 representing a decimal value of $5/32768$ or 0.0001526, then $32768 - 5$ would be 32763 representing 32763/32768 or 0.99985.

One limitation of our routine is the

smallest value for K being $1/32768$ or 0.00003. This means the longest possible time constant is 32767.5 times the period between samples. To circumvent this problem we would need to use more than 16 bits in our arithmetic. This is available as standard arithmetic in some processors. For 16 bit processors it is implemented through multiple precision arithmetic. The price is slower processing. The routine given here computes a new filter output in 0.18 microseconds on the ADSP-2181 whereas a double precision version would be roughly twice as long.

The simple IIR filter has limited performance and a frequency response that drops off at only 6-dB per octave. Although slow in rolling off the frequency response, this is adequate for many applications. Improved performance comes from using not only the current input sample but also one or more of the previous input samples. Additionally, one or more of the previous output values can be used along with the current output. Each of these inputs and outputs has a different K value by which it is multiplied. This provides high filtering performance for the small computational complexity involved. As with most things, there are some drawbacks. Determination of the K values for a particular filter response involves some complexity. Narrow-band IIR filters often involve small K values that end up requiring multiple precision arithmetic. This can end up negating the simplicity arguments. There can be numerical stability* problems associated with computational accuracy as well as detrimental effects from the phase

* Numerical stability here refers to the inherent errors in the calculations causing the algorithm to produce errors of major proportion. This most often happens when subtracting two numbers that are almost the same value. For these occasions, special care may be required, such as the use of multiple precision arithmetic, using 32 or more bits in a data word, in place of the normal 16 bits.

response of the IIR filters such as unnecessary ringing. Never the less, the IIR filter has many applications where its computational efficiency makes it the filter type of choice. However, because of the drawbacks listed, we will concentrate on the alternate category, the FIR filter.

FIR Filters

For filters of higher complexity it is often desirable to use the FIR filter, standing for Finite Impulse Response. These filters never use the previous outputs of the filter computation, but do use the current input along with many of the previous inputs. Analog circuit designers have used the corresponding circuit called a transversal filter as was described in Chapter 3.

DSP construction of the FIR filter is very simple, as shown in the block diagram of **Figure 10.18**. The signal is already available in sampled form from the A/D converter. A delay line consists of places in memory for some quantity of previous samples. Each time a new sample arrives we put it into the beginning of the delay-line memory. Multiplying all the samples by constant numbers and then adding them together form new outputs. The constant multiplier numbers are referred to as the FIR coefficients, or tap weights. The filter design consists of choosing the coefficients to suit the particular application. As with analog filters, there are tradeoffs between the complexity (number of coefficients), pass-band ripple and the out-of-band rejection.

The FIR structure can be used to form filters that are highly selective to the frequency of a sine wave input signal. All of the response characteristics of L-C filters, such as Butterworth and Chebyshev are possible with the FIR filter.

The actual implementation of the FIR filter will be shown in DSP assembly language. This is not hard to follow and allows us to see the type of optimization that has been done to the DSP hardware to make these calculations particularly efficient. For a 10-coeffi-

Program for IIR Filter

```

my0 = K;                                { The new sample is in register mx0, the previous
                                         output of the filter is in RAM at the location save_y
                                         and K is a constant defined at the top of the program
                                         by #define K=5;}
mr = mx0 * my0 (ss);                     { Load register my0 with charging constant }
mx0 = dm(save_y);                        { Multiply the sample by K, both signed integers }
my0 = (32768 - K);                      { Get the last output }
mr = mr + mx0*my0 (ss); { Let the assembler figure out 1.0 - K }
dm(save_y) = mr1;                         { Diminish last output and add new contribution }
                                         { Get ready for next time, output left in mr1 }
                                         
```

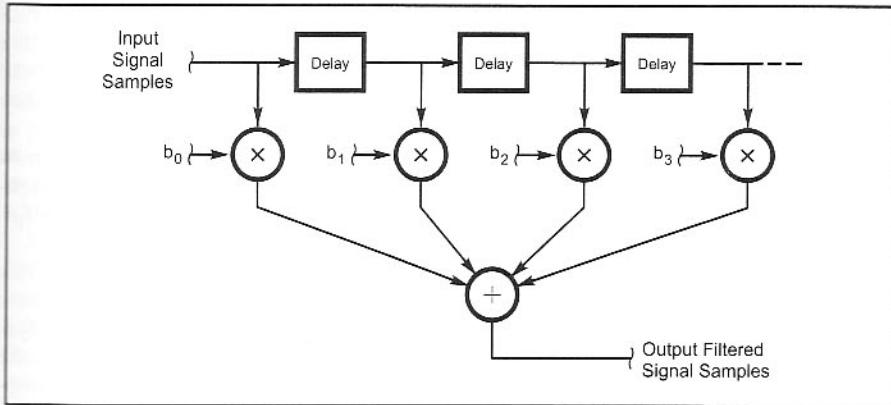


Fig 10.18—Block diagram of the software operations for the FIR filter. The input signal samples are delayed by multiples of the sample period. After multiplication by the filter coefficients, shown here as b_i , the results are summed to produce the filtered output sample. The output values are not brought back into the calculation as was done with IIR filters. The filter can be extended to the right to increase the performance. Filters with more than 100 coefficients are common.

cient filter we start with the initialization shown in Box 1.

These three instructions are part of initialization of the program and are executed only once, when the program is first run. The first instruction again uses index registers that were described on page 10.8. All three instructions set up the registers for the indexed access to the input data delay line. The ‘hat’ symbol seen in $i0 = \text{^circ_data_buffer}$ should be read as “the address of” and creates a constant that can be automatically determined when the program is assembled and linked.

The remainder of the instructions for the FIR filter are executed periodically when new data points are available. The new signal value arrives in the $ax0$ register as shown in Box 2.

The filtered output is in the multiplier accumulator register, $mr1$. The instruction $dm(i0, m0) = ax0$; uses the index registers to place the new data point into our buffer

and, importantly, to increment $i0$ to the next location in the buffer. Since the buffer is circular the new data point will replace the oldest data in the buffer and leave the address in $i0$ pointing to the next oldest data point.

Next are three instructions to setting up the index register, $i4$, which is the address of a series of constants that are our FIR filter coefficients. These registers could have been set up at initialization time by making $i4 = 10$, but are shown this way to emphasize that the FIR filter calculation always start with the same coefficient. The coefficients are, interestingly, stored in program memory, $pm(i4, m4)$. This is a convenience for speeding up the calculation as will be seen below.

Proceeding in the program, we encounter $mr = 0, mx0 = dm(i0, m0), my0 = pm(i4, m4)$; which is a multifunction operation executed entirely within one instruction cycle. This clears the multiply

accumulator, mr which is a 40-bit register consisting of $mr0$ for the least significant 16 bits, $mr1$ for the middle 16 bits, and an 8-bit overflow register $mr2$. In addition two multiply input registers $mx0$ and $my0$ are loaded with data from the delay line, $dm(i0, m0)$ and a coefficient $pm(i4, m4)$. Here is where the efficiency of storing the coefficients in program memory occurs. Separate hardware exists inside the DSP microprocessor for accessing data and program memory. This allows the loading of $mx0$ and $my0$ to occur simultaneously.

The do-loop counter, $cntr$, is loaded with 9, the number of coefficients, less 1. Do firloop until ce ; is an instruction that does housekeeping chores necessary to do repeating calculations and prepares us for the FIR filter.

With everything in place we are ready to do the actual FIR filter calculation:

Firloop: $mr = mr + mx0 * my0$ (ss), $mx0 = dm(i0, m0)$, $my0 = pm(i4, m4)$; is another multifunction operation that executes in a single instruction cycle. It multiplies the contents of registers $mx0$ and $my0$, adds these onto the contents of mr and then reloads $mx0$ and $my0$ with new values from data and program memory. The designation (ss) indicates that both $mx0$ and $my0$ are to be treated as 2’s complement signed numbers. The label ‘Firloop.’ indicates that this is the end of our do-loop. In this case, the loop is only one instruction long, and so this multiply and accumulate operation is repeated 9 times.

After the multiply and accumulate operations, we fall through to one last multiply and accumulate. This one uses the (rnd) designator that still treats the inputs as signed numbers, but also rounds the $mr1$ register (the output) according to whether $mr0$ is more or less than a half. Rounding is done on only the last accumulate. Note that at this point we have used all 10 coefficients.

Box 1 – DSP program for FIR filter initialization

```
i0 = ^circ_data_buffer; { Points to a circular buffer, i.e., a delay line }
i0 = 10; { i0 points to a circular buffer of length 10 }
m0=1; { Increment i0 by m0=1 after use }
```

Box 2 – DSP program for FIR filter computation

```
dm(i0, m0) = ax0; { Enter the new data point into delay line }
i4 = ^fir_coeffs; { Points to start of a table of 10 constants }
i4 = 0; { This buffer need not be circular }
m4 = 1; { Increment i4 by 1 after use }
mr = 0, mx0 = dm(i0, m0), my0 = pm(i4,m4); { Initial data load }
cntr = 9; { This sets the number of 'do' loops }
do firloop until ce; { Loop 9 times, ie, until counter empty (ce) }
Firloop: mr = mr+mx0*my0 (ss), mx0=dm(i0,m0), my0=pm(i4,m4);
mr = mr + mx0 * my0 (rnd); { This is the tenth calculation }
```

Table 10.1
List of operations for 10 coefficient FIR filter showing memory locations

```
dm(3)=New data value
mr=0
mr=mr+dm(4)*pm(1)
mr=mr+dm(5)*pm(2)
mr=mr+dm(6)*pm(3)
mr=mr+dm(7)*pm(4)
mr=mr+dm(8)*pm(5)
mr=mr+dm(9)*pm(6)
mr=mr+dm(10)*pm(7)
mr=mr+dm(1)*pm(8)
mr=mr+dm(2)*pm(9)
{ End of loop }
mr=mr+dm(3)*pm(10)
```

Table 10.1 shows what is happening. Here we have used the shorthand terminology of $dm(i)$ being the i th memory location in our circular buffer. Likewise $pm(j)$ is the j th coefficient in the program memory table. We assume that we came upon this calculation at a time when $dm(2)$ had just been read and we next need to use $dm(3)$. This is where we put the new data point. The multiply and accumulates can be seen to occur 10 times. At the eighth of these we have reached $dm(11)$, which is outside our buffer, so we “wrap around” to the start of the circular buffer at $dm(1)$.

Observe that we have incremented the i_0 value 11 times for our 10 coefficients. This causes the operation to start one location further around in the circular buffer next time a data point is processed. This is equivalent to pushing the data through a delay line, but requires no actual movement of data, only the pointer to the data, i_0 .

The FIR filter calculation can be seen to be straightforward. In the ADSP-2181 it requires about $10+N_f$ instruction cycles for a filter with N_f coefficients. A complex, high performance filter of 200 coefficients would need 210 instruction cycles. If this was repeated at an 8-kHz rate we would be using $8000 \times 210 = 1,680,000$ cycles out of a possible 33.3 million, or only about 5% of the available processing time.

So far we have a way to compute the filter output if we could find out what coefficients to use. The next section shows a way to find them.

FIR Filter Design by the Window Method

The relationship between the frequency response of a FIR filter and the coefficient values is a mathematical formula called the discrete Fourier transform.¹⁰ The details of the transform will not be dealt with here since for most purposes it is not necessary to actually evaluate it. Instead, one can start with a general transform of an ideal rectangular frequency response. For instance, if we wish to pass 400 to 800 Hz the ideal frequency response would be 1.0 within that frequency band and 0 elsewhere. The Fourier Transform of this simple response shape has been done for us, and all we need to do is to plug in the values corresponding to 400 and 800 Hz. Since this is a sampled data operation the sample frequency, say 8000 Hz, is involved as well. In equation form the coefficients are:

$$c_k = \frac{\sin\left(2\pi k \frac{f_H}{f_S}\right)}{\pi k} - \frac{\sin\left(2\pi k \frac{f_L}{f_S}\right)}{\pi k} \quad \text{Eq 10.6}$$

for $k=0$ to $N_f/2-1$, and N_f is the number (an even number*) of coefficients to be found. A special case is $k=0$:

$$c_0 = 2 \cdot \left(\frac{f_H - f_L}{f_S} \right) \quad \text{Eq 10.7}$$

* The formulas are shown here for an even number of coefficients. The form for an odd number is slightly different and although not covered here, is included in the design program.

f_L and f_H are the lower and upper band-pass cutoff frequencies, and f_S is the sample rate, all in Hz. Only half of the coefficients are calculated since they divide into halves that are symmetric, as shown in **Fig 10.19**. This same formula applies equally well to low-pass and high-pass filter design by setting $f_L=0$ or $f_H=(f_S/2)$ respectively.

Unfortunately, filters designed by this formula have several flaws. The response curve of **Fig 10.20** is the result of analyzing our filter. The pass-band is not flat, the sides of the filter are not vertical and probably worst of all, the out-of-band response is only 20 to 30 dB below that of the pass-band. What went wrong? Well, we have tried to describe the filter response with too few elements. Our sampled data cannot describe the extremely fast transitions such as occur at the edges of the pass-band. This design approach compromises the out-of-band attenuation in favor of small transition bands.

Fortunately, it is possible to easily cure the poor out-of-band attenuation. By systematically adjusting the c_k coefficient values, it is possible to push down the out-of-band response. The process for doing this is called windowing. The price that we pay for improved out-of-band rejection is a more gradual transition between the pass-band and the stop-band. This is usually an acceptable tradeoff.

Most FIR filter design descriptions include a variety of windowing methods. Here we will only show one method, the Kaiser window. This is a particularly useful technique:

- It provides an adjustable method for trading off maximum out-of-band response, in dB, for cutoff rate at the pass-band edge.

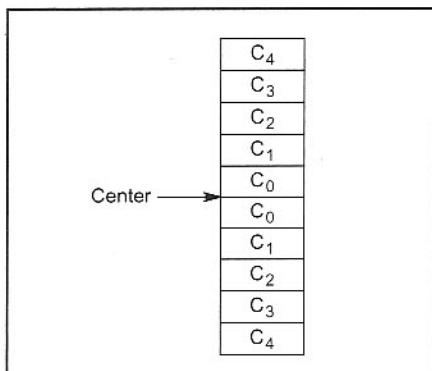


Fig 10.19—Table of FIR filter coefficients for $N_f=10$. Only half of the coefficients are calculated and are placed in the second half of the table. The first half of the table is arranged symmetrically as shown. The design program performs these operations automatically. If the number of coefficients is odd, the symmetry remains about the middle coefficient, which must then be doubled in value, since it only occurs once.

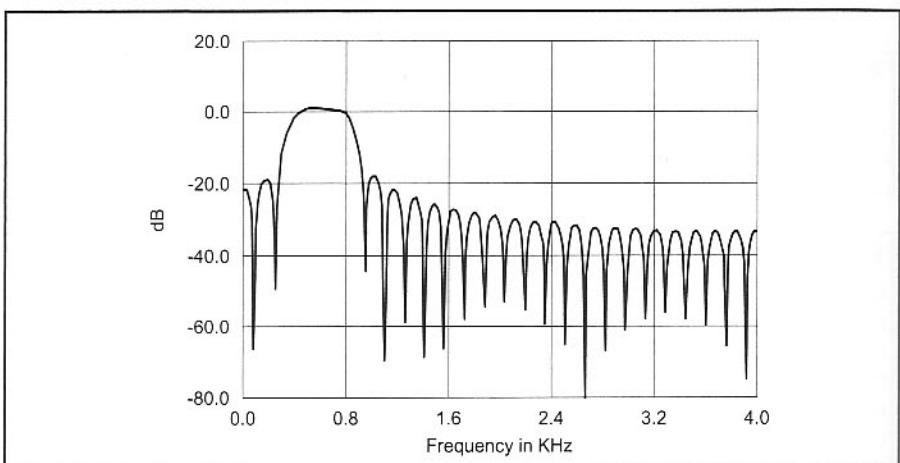


Fig 10.20—Response Curve for a 50-coefficient FIR filter designed to pass 400 to 800 Hz with an 8-kHz sample rate. No windowing function was used with a resulting high out-of-band response.

- The out-of-band response drops rapidly as one moves away from the passband edge. Typically, close-in responses are not as troublesome as those far out.

- The design process, though not trivial, involves a computation not a great deal more complicated than other standard windowing methods.

Implementation of a Kaiser window involves choosing a dB level for the maximum out-of-band attenuation response, K_{db} . This would typically be a number in the 30 to 80 dB range. A BASIC program¹¹ can be used for determining the Kaiser window as well as the coefficient values for the FIR filter. The results of using this program to apply a 30-dB Kaiser window to our band-pass filter can be seen in Fig 10.21.

To better understand the design of a FIR filter using the Basic program, we will show the details for a simple 10 coefficient low-pass filter. Keep in mind that our performance will not be particularly good and most FIR filters use more coefficients, perhaps 30 to 300. Assuming our sampling rate is 8 kHz and we want the low-pass to cutoff at 2.5 kHz, we run the program as follows:

```
FIR Filter Design, Low-pass, Band-pass
or High-pass
Number of FIR coefficients? 10
Sample rate, Hz? 8000
Lower Cutoff Frequency, Hz, between 0
and half of sample rate? 0
Upper Cutoff Frequency, Hz, between 0
and half of sample rate? 2500
Stop-band Attenuation, dB (e.g. 55.0)? 30
Coefficient 1 = .0158115
Coefficient 2 = .0304284
Coefficient 3 = -.0976571
Coefficient 4 = .0379926
```

```
Coefficient 5 = .5243738
Coefficient 6 = .5243738
Coefficient 7 = .0379926
Coefficient 8 = -.0976571
Coefficient 9 = .0304284
Coefficient 10 = .0158115
```

The coefficients are decimal numbers and not the integers required by many DSP. Conversion to integers is accomplished by the following part of a Basic program that could be attached onto our FIR design program:

```
FOR j = 1 TO nf
b(j) = INT(32768 * b(j))
IF b(j) < 1 THEN b(j) = b(j) + 1
PRINT "Coefficient "; j; "="; b(j)
NEXT j
```

This works for 16-bit integer arithmetic. For 24 bit integer arithmetic we replace the 32768 which is 2^{15} by 8388608 which is 2^{23} . Here is what we get from running this program on our 10-coefficient filter (because of the symmetry we will only show the first 5 coefficients):

```
Coefficient 1 = 518
Coefficient 2 = 997
Coefficient 3 = -3200
Coefficient 4 = 1245
Coefficient 5 = 17183
```

FIR filter coefficients will normally be placed into program memory (PM) for the Analog Devices ADSP-2100 series of DSP. The assembler for the Analog Devices EZ-Kit requires that this data be presented in 24-bit format, left justified and right padded with zeros. This is most easily handled in hexadecimal since the right zeros appear

as '00' on the end, each corresponding to four binary bits each equal to zero. A Basic program to convert the original decimal $b(j)$ coefficients would be:

```
DIM H$(301)
FOR j = 1 TO nf
H$(j) = HEX$(b(j))
IF b(j) >= 0 THEN GOSUB POSH ELSE
GOSUB MINH
PRINT H$(j)
NEXT I%
STOP
```

```
POSH:
G$ = H$(I%)
IF LEN(G$) = 1 THEN G$ = "000" + G$ +
"00"
IF LEN(G$) = 2 THEN G$ = "00" + G$ +
"00"
IF LEN(G$) = 3 THEN G$ = "0" + G$ +
"00"
IF LEN(G$) = 4 THEN G$ = G$ + "00"
H$(I%) = G$
RETURN
```

```
MINH:
H$(I%) = RIGHT$(H$(I%), 4) + "00"
RETURN
```

Again the resulting hex output for the first 5 coefficients is:

```
020600H
03E500H
F38000H
04DD00H
431F00H
```

These coefficients would normally be placed into a separate data file, rather than cluttering up the assembly listing.

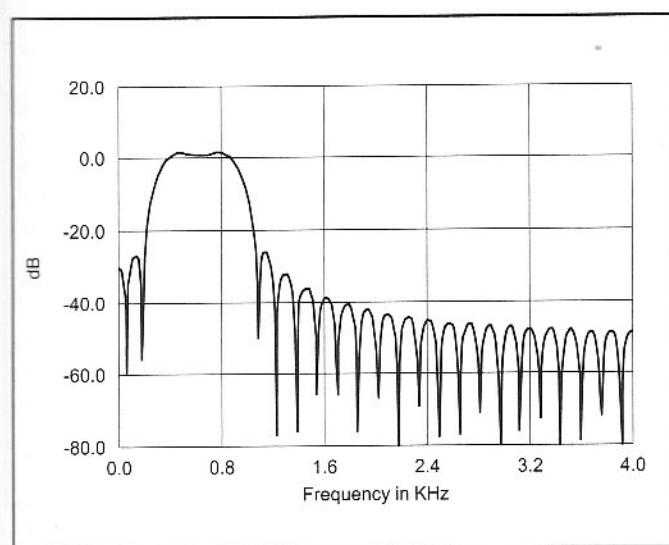


Fig 10.21—Response Curve for the 50-coefficient FIR filter of Fig 10.20 when using a 30-dB Kaiser windowing function to reduce the out-of-band response.

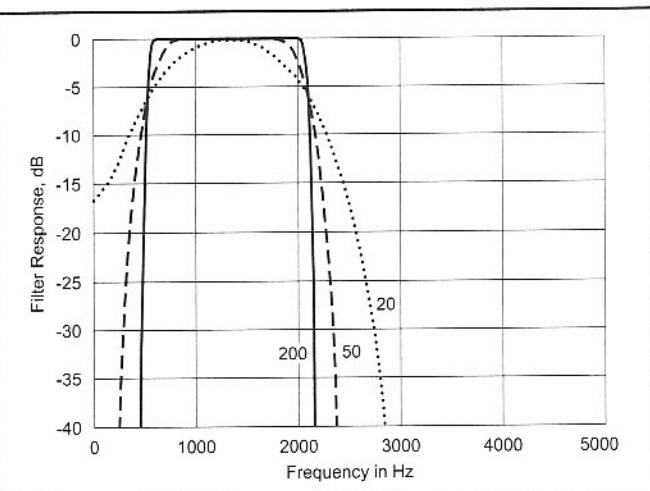


Fig 10.22—Response of three FIR filters designed to cover 500 to 2000 Hz at 6 dB points. The number of coefficients has been set to 20, 50 and 200. The sampling rate for the system was 9600 Hz. The sharpness of the filter is seen to be strongly dependent on the number of coefficients.

FIR-Filter Performance

In Chapter 3, it was shown that passive filters designed from LC components, or active filters using op-amp circuitry, all become sharper in response as their complexity increased. Not surprisingly, this follows for FIR filters as well where the complexity is measured in terms of the number of coefficients.

Fig 10.22 shows the response curves for three FIR filters using 20, 50 and 200 coefficients. All filters were designed to cover 500 to 2000 Hz at -6 dB relative response. With 200 coefficients, the response drops to -40 dB in about 80 Hz, whereas with 20 coefficients the same amount of attenuation occurs over about

680 Hz. This change in performance is very much like that seen in Chapter 3 as the number of resonators was changed.

It might also be noted from the figure that the responses at the high and low cutoff frequencies are nearly mirror images of one another. The rate of cutoff of the filter depends on the number of coefficients, the side lobe levels and the sampling rate of the system, but not on the width of the filter. This can be seen further in **Fig 10.23**, where the bandwidth of the filter was changed, but the number of coefficients was kept at 200. The frequency scale has been narrowed to show the response details better. Note that the cutoff shape is very similar for the different bandwidths.

An interesting characteristic is that the very narrow filters start showing insertion loss, as can be seen with the 100-Hz bandwidth. This happens when the top portions of the response curve from the high and low frequency sides start to overlap.

Figure 10.24 shows the details of the out-of-band response for the 500-Hz filter of Fig 10.23. The design value for the side lobes was -50 dB. As is characteristic of the Kaiser-window FIR filters, the first out-of-band side lobe is at the -50 dB level, but as the frequency gets farther from the pass band, the side lobes continue to drop. For many receiver applications, this is a reasonable response. Interfering transmitter spectrums tend to be

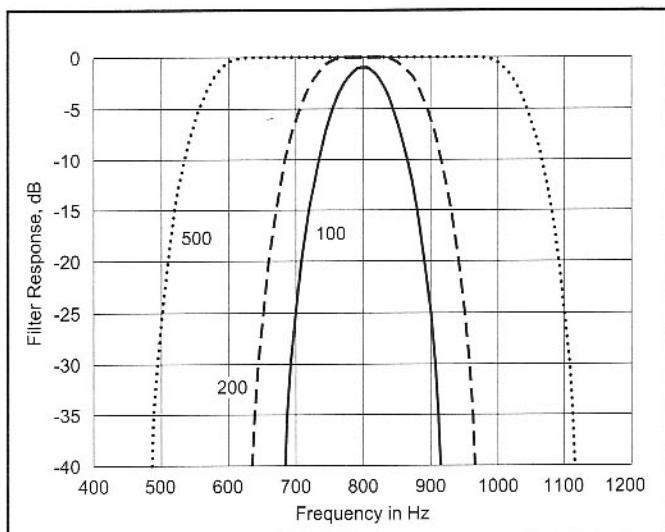


Fig 10.23—Response of three FIR filters designed for a center frequency of 800 Hz, using 200 coefficients and a sampling rate of 9600 Hz. The -6 dB bandwidth was designed to be 100, 200 and 500 Hz.

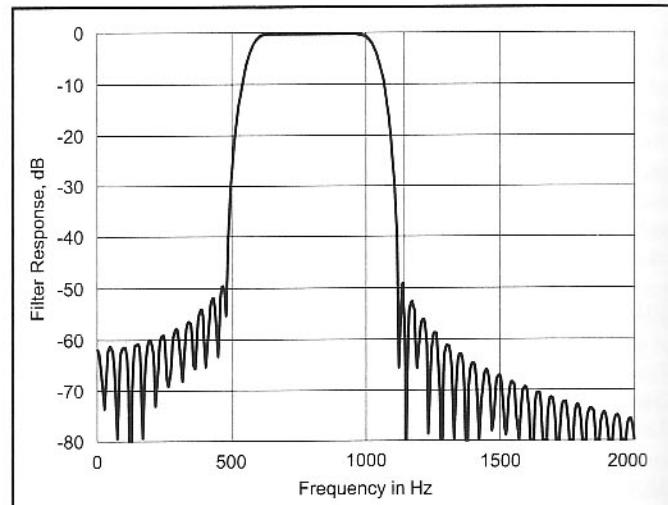


Fig 10.24—The out-of-band response for the 500-Hz filter of Fig 10.23. The design value for the side lobes was -50 dB.

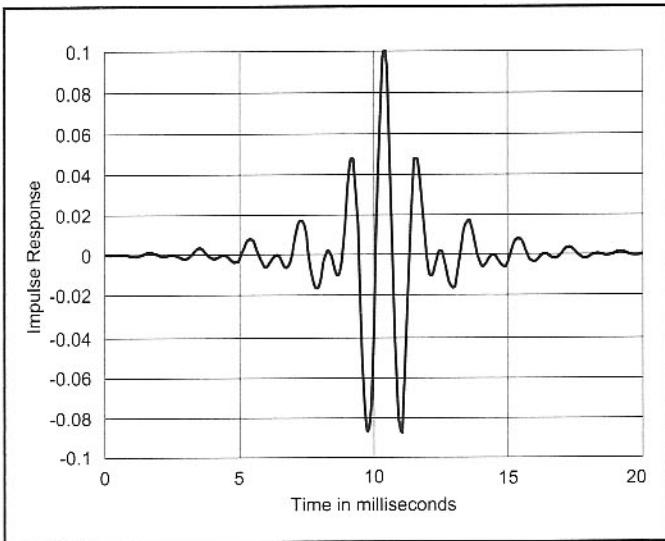


Fig 10.25—Impulse response of a Kaiser-window FIR filter designed for a center frequency of 800 Hz, using 200 coefficients and a sampling rate of 9600 Hz. The -6 dB bandwidth was designed to be 500 Hz.

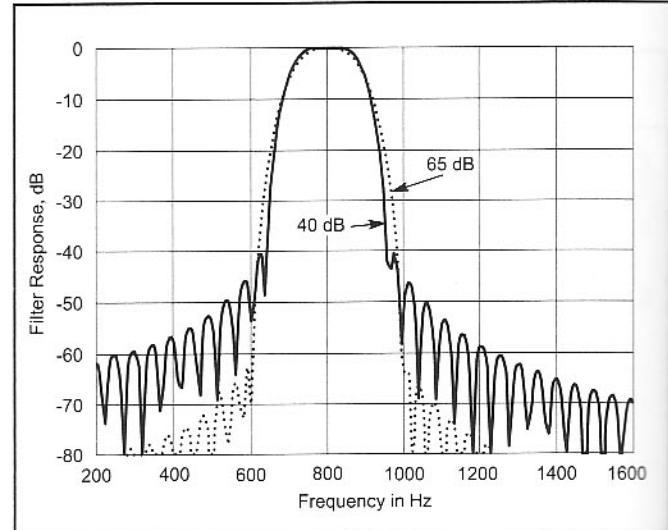


Fig 10.26—Response of a Kaiser-window FIR filter designed for a center frequency of 800 Hz, using 200 coefficients and a sampling rate of 9600 Hz. The -6 dB-bandwidth was designed to be 200 Hz. The two response curves correspond to design side-lobe levels of 40 and 65 dB.

Alternate DSP Devices

The examples in Chapters 10 and 11 are all built around a single DSP processor, the Analog Devices ADSP-2181. This makes the programs easier to follow since the language is not changing from example-to-example. However, it obscures the fact that a number of excellent alternate devices are available from several manufacturers. For specific applications, a particular device may excel over others.

At 33 MHz, the ADSP-2181 does not represent the fastest available processor, either. For audio applications, this is often not important. With a little care in programming, it is usually possible to pack the last IF and audio functions of a communications receiver and transmitter into a device such as this. Examples of this are in Chapter 11 of this book.

Bread-boarding of fast processors such as used for DSP is not simple. Multi-layer PC boards are of major benefit and the IC packages most often use a large number of fine-pitch pins, making connections unsuitable for wires. For these reasons, the use of a "demo board" makes experimentation much easier. Most manufacturers offer demo boards for their DSP devices, often bundled with some collection of support software. Before selecting a particular DSP device for a project, it is best to determine the current offerings of these boards. The prices vary widely, often reflecting the bundled software.

Representative families of low-cost DSP processors are reflected in the table below. These are not the high-end products from the various manufacturers, since these often represent unneeded expense as well as higher power consumption. The changing nature of these processor families suggests that one should

Manufacturer	DSP Processor	Number of Bits	Floating Point	Processor Rate, MIPS
Texas Instruments	TMS320VC5416	16	No	160
Texas Instruments	TMS320C31-50	32	Yes	25
Motorola	DSP56309	24	No	100
Analog Devices	ADSP2181	16	No	33*
Analog Devices	ADSP2191	16	No	160
Analog Devices	ADSP21065	32	Yes	40

*This is the ADSP2181 as used in the EZKIT Lite, put here for comparison purposes. Versions are available that operate at 50 MIPS.

strongest close to their center, and are therefore not filterable when close to the receiver pass band. When there is greater separation between the interfering transmitter and the receiver pass band, where filtering is more effective, the attenuation of the Kaiser-window filter is greater.

In Chapter 3, it was noted that LC filters tend to have added group delay near the edges of the pass band. This is associated with undesirable "ringing" for the filters. FIR filters are usually designed with coefficients that are symmetrical about their center values. This produces a group-delay response that is exactly flat with frequency. The amount of delay is half the number of filter coefficients, multiplied by the sampling period. The response of the filter to a very short

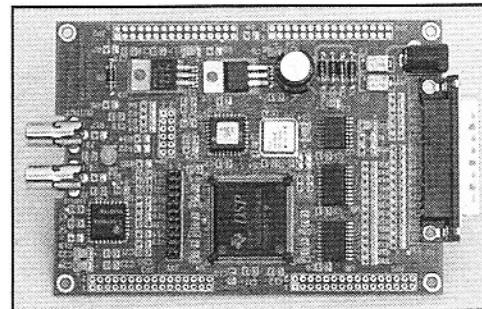
impulse is easy to find as it is just the values of the filter coefficients. Fig 10.25 shows the impulse response for the 500-Hz bandwidth filter of Fig 10.24. The vertical scale shows the coefficient values for a filter with a gain of 1.0 and should be examined here for relative values. The horizontal axis has been scaled in time to correspond to the 9600-Hz sampling rate, i.e. a sampling period of $1/9600=0.1042$ milliseconds. The figure shows a considerable amount of ringing still exists, although the group delay is flat. This ringing is a fundamental consequence of the fast cut off characteristic of the filter. Other filter designs can have less ringing, but only by sacrificing the sharp frequency response.*

A further parameter that is available to

check the manufacturers Web sites for the current data.

In addition to specialized DSP processors, it is quite practical to use a PC directly. High-end Intel, AMD or Motorola processors are able to provide performance levels comparable to the better dedicated DSP device. A sound board provides the CODEC functions. This is not as compact a solution as the dedicated DSP board and thus can't easily be regarded as a "component." The programming environment is complicated by the general-purpose operating systems in use.

An example of an alternate demo-board is the "TMS320C3x Starter Kit" from Texas Instruments. The hardware consists of a 3.5 by 5.0 inch PC board with a TMS320C31 32-bit floating-point processor and a TLC32040 A/D and D/A converter. It is bundled with an assembler and an emulator type of debugger. An interface is provided to control the board from a PC.



The TMS320C3x Starter Kit from Texas Instruments.

* An example of a non-ringing filter is given by C. R. MacCluer, W8MQW, "A Matched Filter for EME," *Proceedings of the Central States VHF Society*, 1995, p24 and is included on the CD that accompanies this book. These filters have a frequency response, at frequency f , of $\sin[2\pi(f-f_c)T]/[2\pi(f-f_c)T]$, where f_c is the center frequency and T is the length, in seconds, of the sine-wave burst (CW dot). This " $\sin(x)/x$ " response creates a slow fall-off with frequency, but the peak signal-to-noise ratio of a CW dot is maximized. The non-ringing characteristic produces an interesting and pleasant "sound" when used in the audio path of a receiver. Because of the spectral side lobes, it can be difficult to tune in a signal by ear. However, when on-frequency, the filter provides excellent CW copy. Another example of this filter implementation is included with the DSP-10 transceiver software that is part of the *Experimental Methods in RF Design* CD.

the Kaiser-window FIR filter designer is the side lobe level. **Figure 10.26** shows the frequency response of filters designed to 40 and 65 dB levels. These filters both have the same nominal 200-Hz bandwidth at -6 dB points. The most obvious feature is the side lobe response far from the pass band, which is about 20 dB lower for the 65 dB case. In addition, it can be seen that the design with the lower out-of-band response is also less sharp around the pass band. The response at 40 dB below the peak is 296 Hz wide for the 40-dB filter and 344 Hz for the 65-dB filter. Thus the

penalty for having the lower out-of-band side lobes is poorer passband shape.

Hilbert Transforms

One of several specialized applications for FIR filters is the Hilbert 90-degree transform. These are a close counterpart to the broadband 90-degree phase-shift networks discussed in Chapter 9. They are characterized by a constant 90-degree phase shift and an amplitude response that covers a wide frequency range. The flatness of the frequency response as well as

the bandwidth that can be covered depend on the size of the FIR filter, i.e., the number of coefficients.

The Hilbert transform has a fixed delay in addition to the 90-degree phase shift. In order to produce two signals differing in phase by exactly 90-degrees, it is necessary to place a fixed delay in the second path. A DSP implementation of the fixed delay requires only a few instructions. The interested reader should study the 18-MHz transceiver in Chapter 11, which uses one of the Hilbert transforms in the SSB generation and detection.

10.7 DSP IF

Computers, and specifically DSP microprocessors, are limited in their processing speed. The instruction set for the DSP makes it faster for signal processing, but DSP is still best suited for signals in the 10's of kHz or less.* Audio processing is easily in this range and not surprisingly, has been a major application for DSP in radio systems. Interesting applications are possible by use of a low frequency IF, however.

Fig 10.27 is a block diagram of a radio receiver, implemented with the last IF in a DSP at 7.5 kHz. One would prefer an IF as low as possible, which is often quite practical. For instance, if the analog IF has a bandwidth of 5 kHz, the 60-dB points for a reasonable crystal filter might be 15 kHz apart. This will allow the use of an IF as low as 2.5 to 7.5 kHz with the image rejection being always greater than 60 dB (see **Fig 10.28**). With the proper A/D converter, this would be supported by a sampling rate of about 20 kHz.

Fine Tuning

A major advantage of the DSP IF is the simplicity of fine frequency control. We have already seen that we can easily generate a sine wave in software with good frequency resolution. This is ideal for use as the oscillator for frequency conversion. This can be a shift in the IF, or more often,

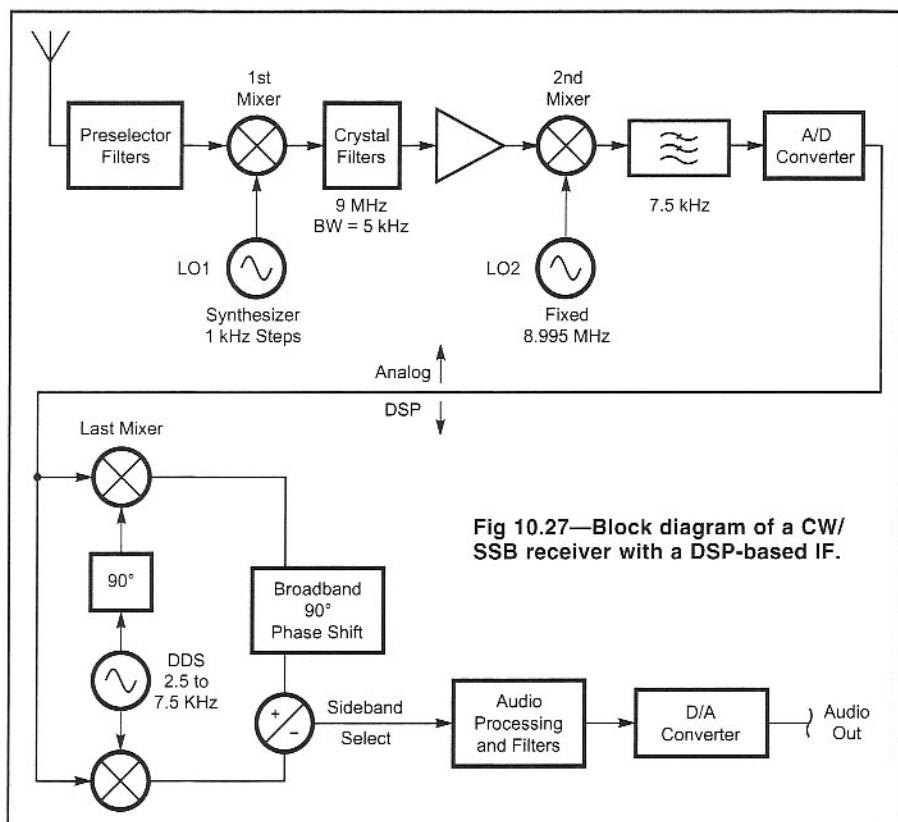
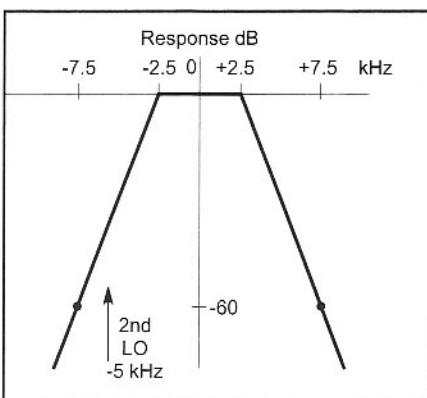


Fig 10.27—Block diagram of a CW/SSB receiver with a DSP-based IF.



it is the final conversion often called the BFO. As we will see, the input and output frequencies of the conversion process can overlap and so there is considerable freedom in choosing the IF.

* The ADSP-2181 in the EZ-Kit Lite that has been used for the examples executes 33 instructions per microsecond. Each instruction can be a simple operation, such as adding of two numbers, or it can be a multiple part instruction that multiplies two numbers together, adds these to an existing sum, fetches two different values from memory and updates a loop counter. This latter type of instruction is an example of the specialized instructions that allow high computation rates in a DSP microprocessor.

Fig 10.28—The required response curve for the crystal filter used in the receiver of Fig 10.27. The frequencies shown are relative to the IF center. Image responses are limited by having 60 or more dB of rejection at 5 kHz from the band edge.

10.8 DSP MIXING

The double-balanced mixer of Chapter 5 has wide application as an analog component. The simplicity of a DSP implemented mixer can be surprising at first introduction:

$$mr=mx0*my0 \text{ (ss);}$$

That is, only a simple signed multiply

is required. If $mx0$ and $my0$ registers represent sine waves, then mr will represent a signal containing only the sum and difference frequencies. The rejection of signals passing from the inputs ($mx0$, or $my0$) to the output (mr), called port-to-port isolation in conventional mixer descriptions, is for practical purposes perfect.

This very high isolation allows the input and output frequencies to be in overlapping bands. Additional processing is needed since one usually only desires only the sum or the difference frequencies. An example of this is a Hilbert Re-tuner described by Forrer.¹² This process corresponds to the Phasing method of SSB detection, described in Chapter 9.

10.9 OTHER DSP COMPONENTS

There are many functions that lend themselves to DSP implementation in a radio. We only touch upon many of them here. The following should be thought of as a starting point for further exploration!

Automatic Gain Control (AGC)

Figure 10.29 is a block diagram of a DSP implementation of a classical AGC feedback loop. The control point for the loop, shown in the figure, is the IF signal after A/D conversion. The function of the loop is to keep the control-point amplitude close to constant. A detector is used to measure the envelope of the IF signal. This is low pass filtered and adjusted in level by the AGC Filter. The filter output goes back through a D/A converter to control the gain of an IF amplifier. In addition, the AGC controls a digital gain multiplier that is within the loop.

The analog gain control is used to ensure that the A/D converter is operated

well into its operating range, while still preventing overload. The digital part of the loop keeps the total signal level near a constant level at the output.

The response of the filter going to the analog IF amplifier, referred to in the figure as the slow loop must cutoff at a low enough frequency to allow stability, including the delay effects of the A/D converter. The converter delay is often many hundreds of microseconds resulting in a maximum AGC bandwidth in the tens of Hertz. This is too slow to provide adequate attack response on a rising strong signal, and requires that the A/D converter not be set to operate too close to its overload point. This is usually possible to arrange in the design.

Improvement comes from the internal DSP fast loop in Fig 10.29. This feedback loop does not include the A/D converter and is limited only by the sample rate of the data. The signal levels should be set so that this loop is the gain controlling function for normal operation.

One of the big advantages of a feedback AGC system is its ability to work with highly inaccurate gain control functions. In the case of the DSP, however, this is not needed. Gain can be controlled by either multiplication, or multiplication along with a binary shift. Either of these functions are accurate to a fraction of a dB and can be used with open loop control. The general scheme for this AGC system is Fig 10.30. The analog feedback slow loop is maintained for very strong signals, but the DSP gain control is placed after the detector. This allows a delay to be placed in the signal path, so that the signal levels are well known when the control is applied. That is, the gain is reduced in a "circuit" before the signals arrive at that point. This feed forward approach is capable of very good sounding AGC, since the accuracy of the control and the response time have been made independent. Methods of this sort have been in use for several years in DSP based transceivers offered by Rohde and Schwarz.¹³

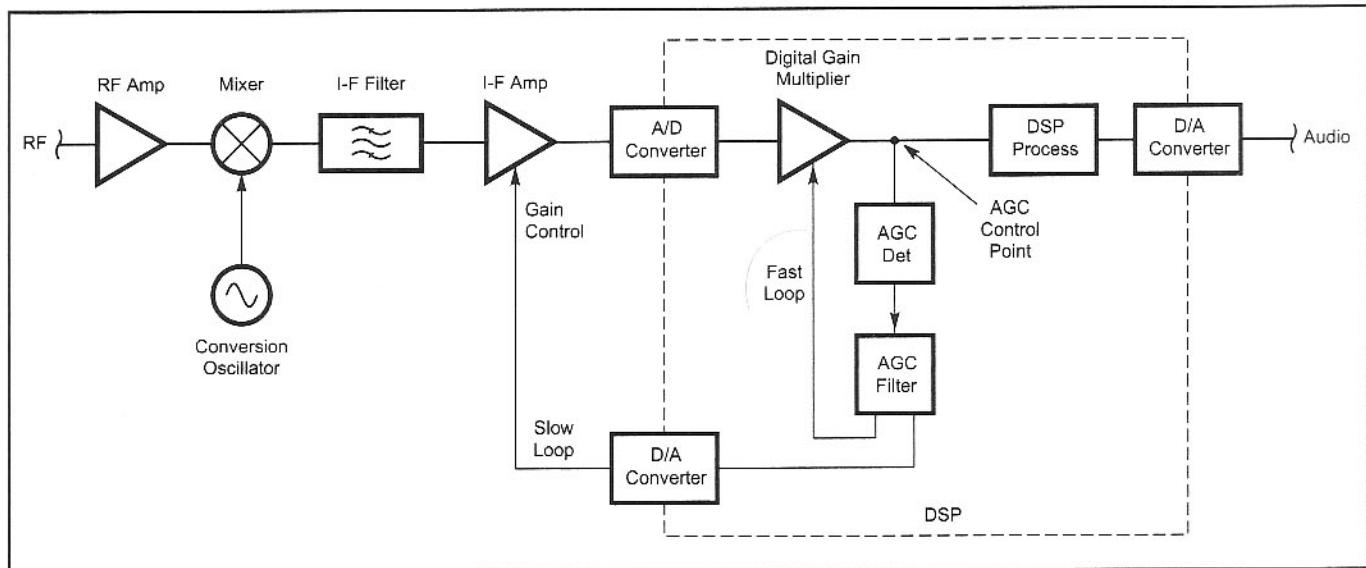


Fig 10.29—DSP-based feedback type of AGC showing a combination of analog and digital gain-control points.

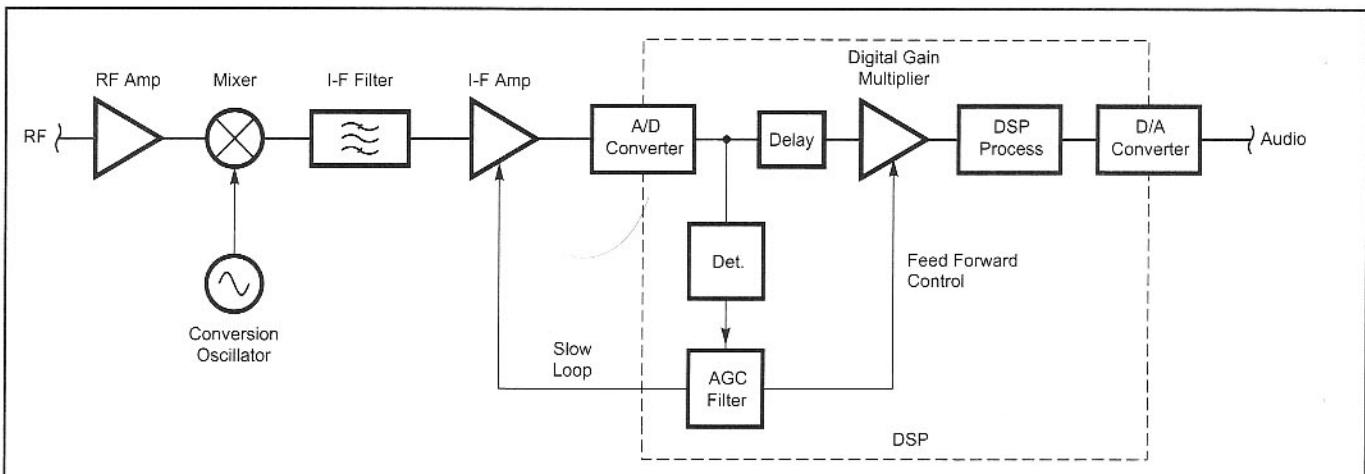


Fig 10.30—DSP-based AGC with analog feedback and digital feed forward control.

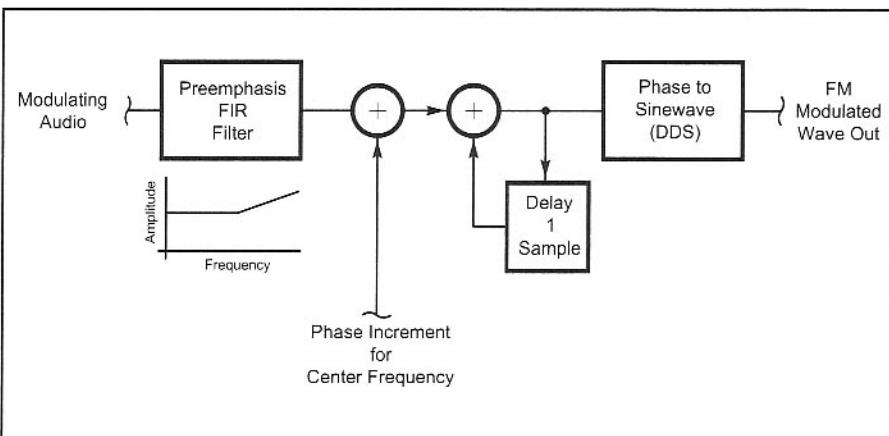


Fig 10.31—Direct generation of FM signal.

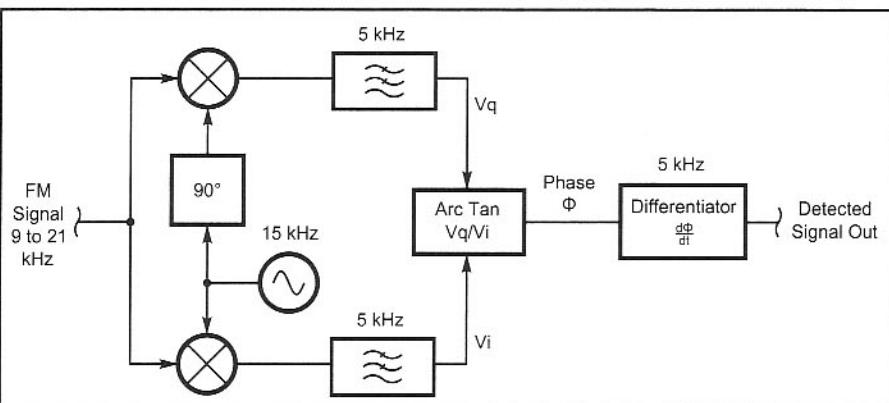


Fig 10.32—An FM detector built using an arctangent phase detector and a differentiator.

FM Transmission

Earlier in this chapter the DDS method of generating sine waves was described that was based on incrementing a phase value by a constant amount called a phase increment. The frequency of the sine wave is proportional to the phase increment. FM modulation can be accomplished by vary-

ing the phase increment in accordance with the modulation waveform. This is inherently of very low distortion. Most FM systems employ some preemphasis for the higher modulation frequencies that can be accomplished by placing a FIR or IIR filter ahead of the modulator. Fig 10.31 shows the overall arrangement.

FM Reception

As is the case for analog Frequency Modulated (FM) discriminators,¹⁴ a number of methods exist for the DSP-based detection of an FM signal. FM is a special case of phase modulation and one of the best FM detectors starts with a phase detector, as shown in Fig 10.32. The FM signal at IF, shown here as 9 to 21 kHz, is mixed with a pair of constant frequency signals at mid-band (15 kHz). These two mid-band signals differ in phase by 90 degrees and, with DSP, can be generated as two separate signals. Low pass filters, in this case at 5 kHz, remove the signals at the sum frequency, leaving just the difference signals. Since these two signals were derived from the 90-degree mixing process they are called quadrature signals (see Chapter 9) and can be shown to retain all of the information that was originally in the IF signal.

The phase angle of the input signal, relative to the 15-kHz center sine wave, can be determined from the two quadrature signals, v_i and v_q by:

$$\varphi = \tan^{-1} \frac{v_q}{v_i} \quad \text{Eq 10.8}$$

Arc tangent functions can be computed by polynomial approximations, in a fashion very similar to that used to compute a sine wave earlier in this chapter.¹⁵

Frequency is defined as the rate-of-change of phase. The mathematical term for this operator is the derivative and the functional block for finding it is the differentiator. When reduced to a DSP program, all that is required is to subtract the current phase value from the previous value. In general it is necessary to watch the phase value where it passes through 360 degrees, since that point and 0 degrees are the same. If the phase value has been

scaled so that 360 degrees is the entire range of the 2's complement arithmetic (0 to 65535 for 16-bit arithmetic) then the rollover at 360/0 degrees is automatically

treated correctly for either direction of rollover.

Thus the output of the difference operation is the FM demodulated signal. In general,

it is necessary to place this through an appropriate de-emphasis filter to reduce the high frequency boost introduced at transmission time. This could be the simple RC IIR filter described earlier.

10.10 DISCRETE FOURIER TRANSFORM

In Chapter 7 we explored using Spectrum Analyzers to observe the content of signals in the frequency domain. They consisted of a detector for measuring signal amplitude coming from a receiver along with a local oscillator for tuning the receiver. The local oscillator was made voltage tunable so that it could be swept across a range of frequencies. When com-

bined with an oscilloscope for displaying the signal amplitude, analysis of the signal spectrum was possible.

An alternate DSP implementation of the

Spectrum Analyzer, using the Discrete Fourier Transform (DFT), has some attractive features. The swept local oscillator and associated mixer are not needed in

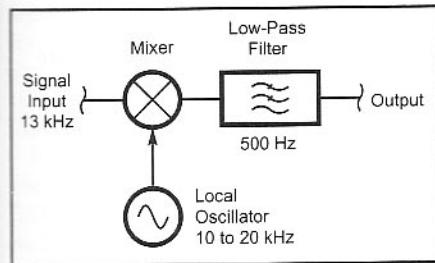


Fig 10.33—A first implementation of a circuit to measure signals in the 10- to 20-kHz frequency range. The output of this circuit is sensitive to both the frequency of the input signal and its phase, relative to the local oscillator.

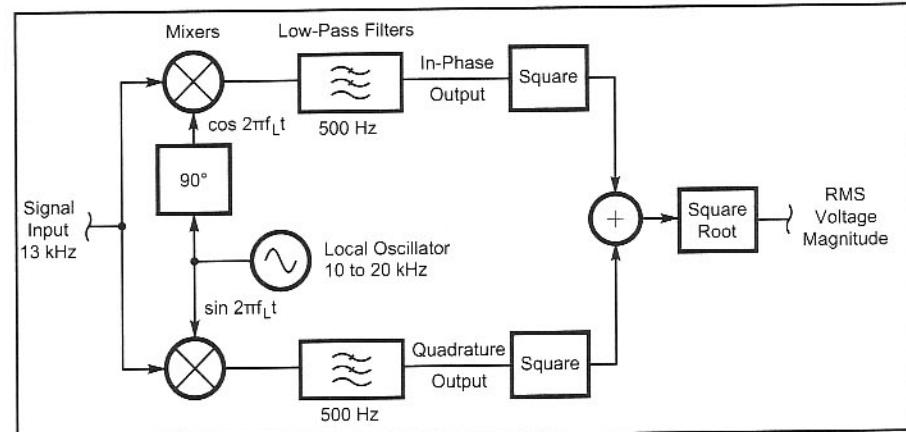


Fig 10.34—An improved implementation of the circuit of Fig 10.33. The in-phase and quadrature outputs will never be zero simultaneously, regardless of the input phase relative to the local oscillator. Blocks have been added to square the in-phase and quadrature outputs, add these together and then take the square root. This produces the RMS voltage of the signal input at the frequency of the local oscillator.

Mathematics of the Discrete Fourier Transform

Mathematical formulations of the Fourier transform are given in many books. In general, the DFT has inputs and outputs consisting of complex numbers described as $V_{Rk} + j V_{Ik}$ where V_{Rk} and V_{Ik} are called the "real" and "imaginary" parts of the complex number. This use of complex numbers has considerable convenience in writing and evaluating equations. However, the mystical sound of "imaginary" numbers and associated use of $j=\sqrt{-1}$ can be removed if an alternate description of the complex number as "an ordered pair of real numbers" is used. This illustrates that each input to the DFT is a pair of real numbers that are treated by a specific set of rules (equations) to produce a set of ordered pairs of real numbers at the output. Ordered pairs merely means that the first number (real) is not to be interchanged with the second number of the pair (imaginary).

With this in mind, we can examine the kth outputs of the DFT with a complex input:

$$X_{Rk} = \sum_{n=0}^{N-1} V_{Rn} \cdot \cos\left(2\pi k n / N\right) - \sum_{n=0}^{N-1} V_{In} \cdot \sin\left(2\pi k n / N\right)$$

and...

$$X_{Ik} = \sum_{n=0}^{N-1} V_{Rn} \cdot \sin\left(2\pi k n / N\right) + \sum_{n=0}^{N-1} V_{In} \cdot \cos\left(2\pi k n / N\right)$$

Here we have separated the real and imaginary inputs, V_{Rn} and V_{In} as well as having separate equations for the real and imaginary output parts, X_{Rk} and X_{Ik} . Notice that all mention of j disappears and the real and imaginary parts are kept separate by placing a subscript R or I on the variable.

We show the kth output pair, but there are a total of N of these output pairs corresponding to k values from 0 to N-1.

If the inputs have zero imaginary parts, such as is the case for a time waveform, the second sum in each equation will become zero and the DFT outputs simplify to:

$$X_{Rk} = \sum_{n=0}^{N-1} V_{Rn} \cdot \cos\left(2\pi k n / N\right)$$

and...

$$X_{Ik} = \sum_{n=0}^{N-1} V_{Rn} \cdot \sin\left(2\pi k n / N\right)$$

These are the versions that are described by circuit analogs in the text.

hardware form. The output spectrum is being constantly generated instead of waiting for the tuning to sweep by, providing higher sensitivity and faster update rates. However, the DFT is limited, by both A/D encoding and computing rates, in the frequency range that can be covered.

The operation of the DFT can be understood by a thought implementation of an analogous traditional hardware circuit. This starts by assuming we wish to examine the output of a receiver IF in the 10- to 20-kHz range. Initially, assume that the only signal present sits at 13 kHz.

We wish to find out what signals are in this IF band and what their strength might be. We begin with a balanced mixer capable of operation at these low frequencies, as shown in Fig 10.33. We drive the mixer with a suitable local oscillator, capable of covering 10 to 20 kHz and run the output through a very narrow low-pass filter. As we tune the LO, we see no output until we get close to 13 kHz, due to the low-pass filter. Then we start to see low frequency outputs. When the LO is exactly at 13 kHz, the output is a dc signal that we can measure with a voltmeter.

We might be tempted to note the dc level coming from the mixer and use this to infer the strength of the incoming 13-kHz signal. However, this would generally produce an error, for we know nothing of the phase of the LO with respect to the signal we are trying to measure. Recall the phase detector characteristic investigated in Chapter 4, section 7 shows that the mixer output depends on the phase angle between the RF and LO signals. For 90-degree phase differences this output will be zero, clearly the wrong answer! This dilemma can be solved by replacing the single mixer with a pair of identical mixers, both driven from a common signal or RF port, but driven with a pair of LO signals with 90-degrees phase difference. This is illustrated by the block diagram of Fig 10.34, where we have simplified the circuit by using a single oscillator and a 90-degree phase shifter. Now, as the phase of the input is varied, we will see the output of one mixer go to zero while the other peaks. The true (RMS) output voltage magnitude is obtained by squaring each of the two mixer output voltages, adding, and taking the square root.*

Clearly, we can replace the hardware mixers with a DSP version. The 10-to-20-kHz signal is applied to an A-to-D converter to produce a time-sampled version of the signal. This is applied to a pair of

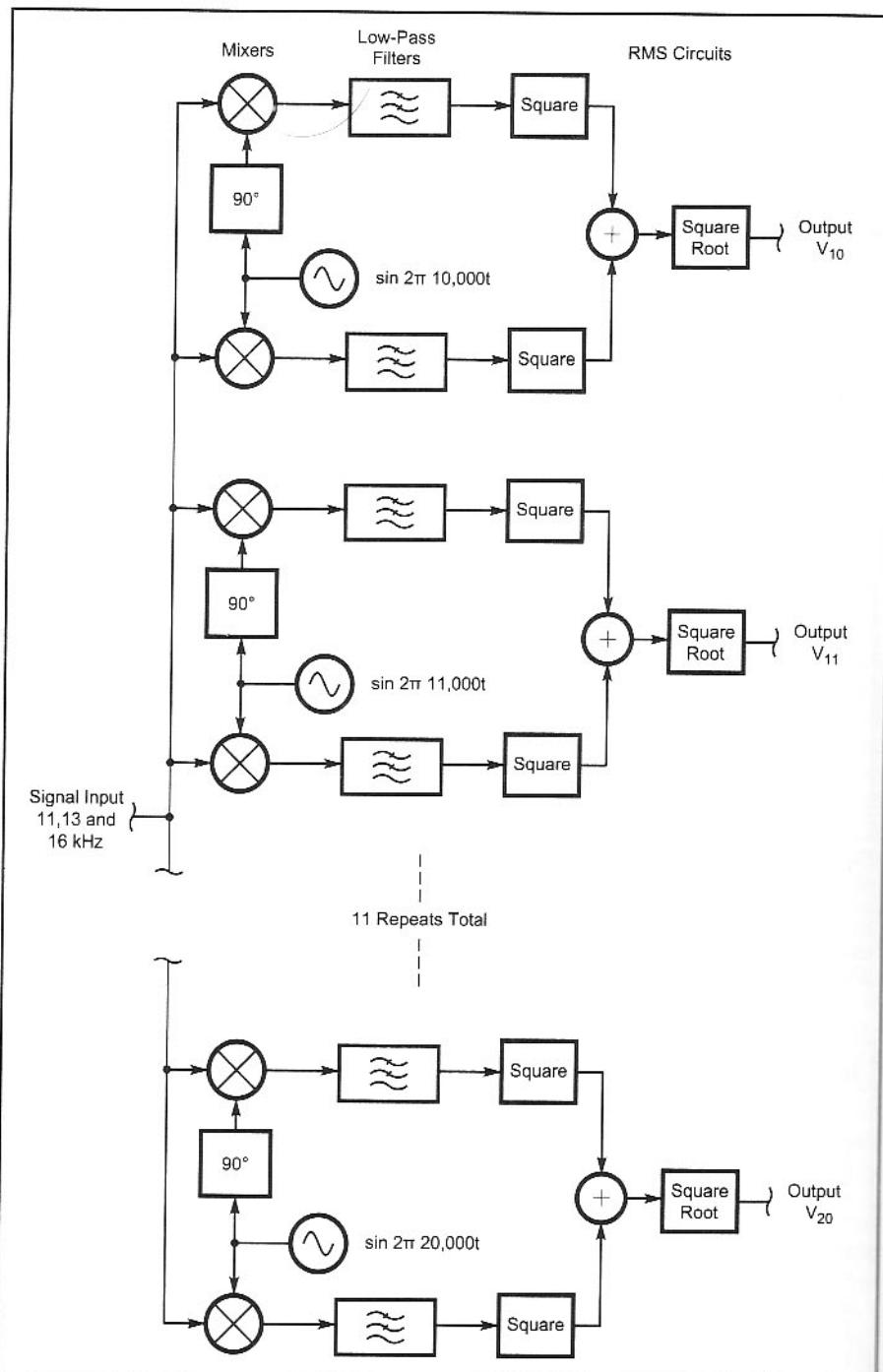


Fig 10.35—A filter bank type of Spectrum Analyzer, built from multiples of the in-phase/quadrature filters of Fig 10.34. As discussed in the text, this structure is equivalent to a Discrete Fourier Transform, followed by the RMS squaring and square-root circuits.

DSP mixers, one driven with a $\cos(2\pi f_L t)$ signal while the other is driven in quadrature by $\sin(2\pi f_L t)$. The outputs are low pass filtered to eliminate any sum terms, leaving only the base-band outputs. These can be used to calculate the output voltage, just as we did with the hardware mixer. This is just a phasing method receiver as discussed in Chapter 9.

Let's continue our thought implementation by adding more signals in the 10- to

20-kHz band. The original 13-kHz signal is supplemented with a weaker one at 11 kHz, and perhaps another at 16 kHz. One way to estimate the overall spectra would be to add two more mixer pairs with a pair driven at each of the new input frequencies. However, let's get even more general. Instead of adding just two more mixer pairs, we will assemble a collection of 11 of these circuits with a quadrature pair at each 1-kHz increment from 10 to 20 kHz.

*If one only wants the power of the signal as an output, the square-root block can be omitted.

Fig 10.36—A detailed block diagram of the DFT with only “real” input data, such as from samples of a time waveform. The multiplying (mixing) signals are calculated sine and cosine values with frequencies spaced every f_s/N Hz, where f_s is the sampling rate for the data. The resulting outputs are referred to here as “In-phase” and “Quadrature” data.

Figure 10.35 shows a block diagram of our growing collection of thought hardware. Most outputs will be close to zero, but we will see substantial outputs corresponding to 11, 13 and 16 kHz.

We now have a “bank of filters” type spectrum analyzer. We could have achieved the desired result by actually building 11 band-pass filters, each followed by a suitable detector. Instead, we have achieved the same result with mixers driven by quadrature-local-oscillator signals.

These systems are fundamentally different than the usual “swept front-end” spectrum analyzer. If we were to build one of those for this example, we might use a swept local oscillator that tuned from, for example, 60 to 70 kHz. A single mixer would heterodyne the input up to a narrow band-pass filter at 50 kHz, followed by a suitable detector. As the oscillator sweeps the input frequency from 10 to 20 kHz, the signal-amplitude output for the incremental kHz points will be virtually the same as we obtained from the banks of mixer pairs. However, while the swept system provides information for one frequency at a time the filter bank provides all outputs simultaneously.

Banks of oscillators, mixers and low-pass filters become unwieldy if built from hardware. But we can build up their equivalent DSP components as is shown in Fig 10.36. As shown in Fig 10.37, oscillators are replaced by quadrature sine and cosine wave computations. Numerical multipliers replace the mixers. The low-pass filters are replaced by summing several multiplier outputs. This needs to be repeated for each of the frequencies of interest, such as our integral frequencies from 10 to 20 kHz. Put into this mathematical form, we have recreated the DFT algorithm.* Those inclined towards mathematical descriptions can also see this from the equations in the sidebar, “Mathematics of the Discrete Fourier Transform.” Most implementations of the DFT would compute the spectral outputs from 0 to 9 kHz as well as the 10- to 20-kHz outputs shown, but this is not required to be a DFT.

*As will be discussed, the full DFT is more general and allows the input to be a complex number. Here, we are dealing with a simplified case where the “imaginary part” of the input is zero.

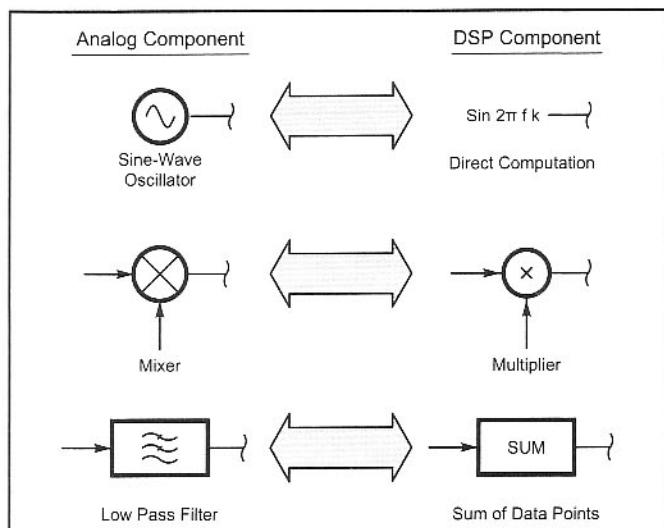
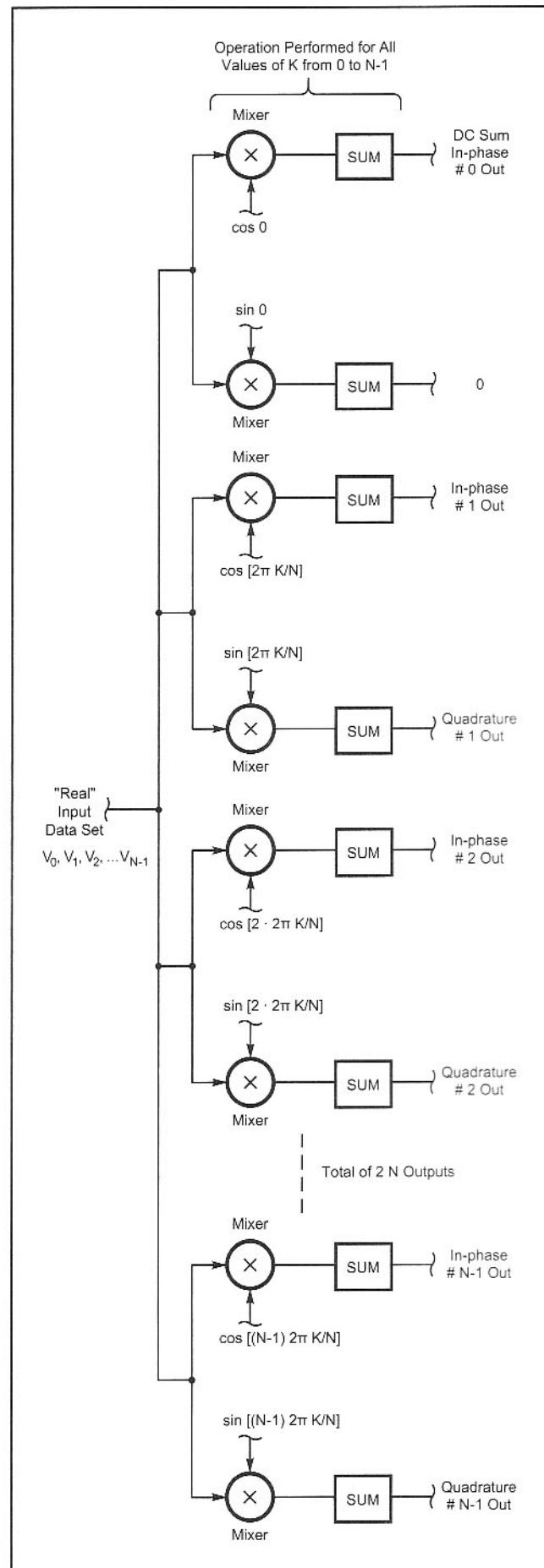


Fig 10.37—Equivalent analog and DSP components that are used to create an “equivalent circuit” for the discrete Fourier transform (DFT).



Terminology for the DFT differs from that used for hardware. Our block diagram of Fig 10.35 is in the latter term. Restructured in conventional DFT terminology, Fig 10.36 shows the same filter bank implementation. The RMS voltage blocks have been removed to show only the DFT.

Implementing the DFT

The “discrete” in DFT tells us that the system is only using data samples, as we would get an A/D converter. The Nyquist criteria requires the sample rate to be at least twice the highest frequency of interest. This would require a sample rate greater than 2×20 kHz for the thought implementation above.

The more points in the sample, the greater resolution we can achieve in estimating the related spectrum. This can be put into the formula:

$$B = f_s / N \quad \text{Eq 10.9}$$

where B is the frequency spacing between adjacent spectrum samples (filter-bank centers), f_s is the sample rate, and N is the number of sample points being averaged. One divided by B gives the length of time over which samples were collected. The frequency spacing B can easily be made quite small. For example, if the sampling rate is 10 kHz and there are 1024 samples in the DFT, the resolution B will be $10,000/1024$ or 9.77 Hz. By selecting suitable f_s and N it is practical to have resolutions of less than 1 Hz.

The streamlined class of algorithms most often used to compute the DFT is called the Fast Fourier Transform (FFT).¹⁶ These algorithms eliminate the redundant calculations that occur when N equals 2 raised to an integer power. The efficiency of the FFT allows large numbers of points to be included in a DFT computation. N values of 64 to 4096 are common. The details of the FFT require some study to follow, but for most applications this need not be done since prewritten subroutines can be used.¹⁷ Rather than focusing on the details of the FFT, the important element is to understand the general nature of the DFT and the meaning of the resulting data.

FFT implementations usually compute N quadrature pairs of outputs. If only a few outputs are needed, it is often simpler to implement a band-pass filter bank. An efficient implementation of this is the Goertzel algorithm.¹⁸

The Ins and Outs of the DFT

When one uses the DFT, interpretation of the input and output data can be confus-

ing. To understand how these data are used, we will examine finding the frequency spectrum of a time waveform.

The DFT algorithm operates on a block of N input-data points, each of which is a sample of a time waveform, such as an IF or AF signal. The DFT is expecting N complex input numbers that are divided into two groups, the “real” and the “imaginary” values. These are historic names used with complex numbers and should be thought of as merely a way to keep the groups separate. For our case, the N real values will be the waveform time samples and the imaginary group will all be zero.*

After the DFT calculation is completed, there will be non-zero values in each of the real and imaginary groups. These represent the zero-degree and 90-degree amplitude components of the frequency spectrum, referenced to a sine wave at the center frequency of each of the output frequencies.

The spacing between spectral data points is $B = f_s / N$. If we have N outputs from the DFT these will seem to extend from 0 frequency to $N \times f_s / N$ or f_s which is the sampling frequency. This is inconsistent with the Nyquist sampling theorem, which says the highest frequency for which we can extract unambiguous information is half of the sampling frequency. This is resolved when we look at the DFT output. It will be seen that each output point appears twice. The first $N/2$ data points apply for frequencies up to half the

*Operating the DFT with half the inputs set to zero suggests wastefulness! It is possible to place a second time waveform in place of the zeroed imaginary group. The output values then contain co-mingled spectral data that can be sorted out with simple additions and subtractions. This can be a major computational saving for some applications, but with some possibility of added noise for fixed-point DSP.

sampling frequency and the second half are their mirror image. The practical result is that one merely discards the redundant data to the right and uses the left data.

An example of this is in Fig 10.38 showing a time waveform with $N=16$ and the resulting spectral power from a DFT. The output power values to the right of center are seen to be mirror images of those to the left.

Fig 10.39 illustrates this operation of the

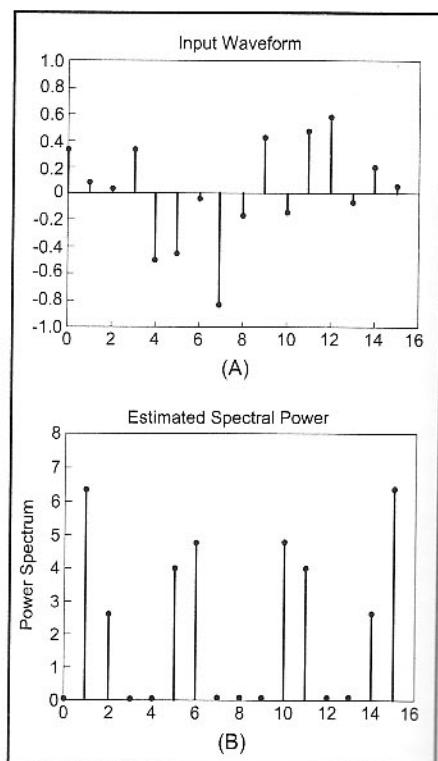


Fig 10.38—This diagram shows (A) 16-member time waveform and the power for the DFT output. To emphasize the discrete nature of the data involved, the values are shown as dots with attached vertical lines. Note that the spectral power is symmetrical about the 8th output.

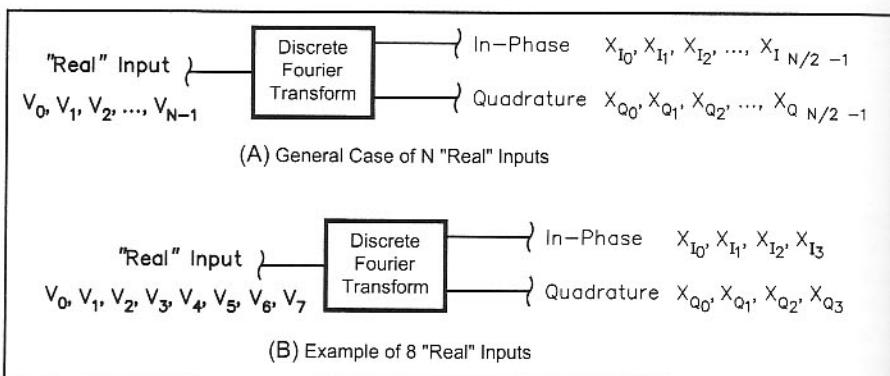


Fig 10.39—Block diagram of the Discrete Fourier Transform with a time waveform input. The output information is referred to here as “In-phase” and Quadrature.” For this case of all “real” inputs, the number of output pairs is half the number of input samples. The upper figure applies to any number of sample data points. The lower figure is specific to 8 input sample data points.

DFT on a real time series in block diagram form. This is shown with a “real” input since the imaginary input was set to zero. To make their role more obvious, the outputs are now called “in-phase” and “quadrature.” N inputs numbered 0 to N-1 will produce pairs of outputs numbered 0 to (N/2)-1. The lower figure shows this for the specific case of N=8. There are 8 inputs, numbered 0 to 7 and 4 pairs of outputs numbered 0 to 3.

DFT Spectral Frequency Response

Since the DFT of a time waveform is equivalent to a bank of band-pass filters, they must have a frequency response. We can use the mixer/low-pass filter (LPF) analogy to find this response. Fig 10.40 shows the response of a LPF constructed by adding 16 points together, just as is done for a 16-point DFT. The data sample rate was set at 1000 Hz producing a frequency bin spacing of:

$$B = f_s / N = 1000/16 = 62.5 \text{ Hz} \quad \text{Eq 10.10}$$

The 3-dB point on the response curve is at 27.8 Hz. The mixer input signal that produces this LPF input can be on either side of the LO. Thus the overall 3-dB bandwidth is twice the LPF response or 55.6 Hz, or 89% of the bin spacing.

At the bin spacing the response is down 3.92 dB. The fall-off rate of this low-pass filter response is not particularly fast, with the first side-lobe response down only about 13 dB. This means that the output of the DFT will tend to respond to signals far from the associated LO frequency. The use of “windowing” functions to improve this off-frequency response is discussed below.

Power from the DFT

Often it is desirable to estimate the power associated with each of the output frequencies of the DFT. The in-phase and

quadrature outputs correspond to the sides of a right triangle and the power to the hypotenuse squared:

$$P_i = V_{I,i}^2 + V_{Q,i}^2 \quad \text{Eq 10.11}$$

An example of a spectrum analyzer built using the power outputs from the DFT is the DSP-10 2-M radio, originally described in *QST*.¹⁹ The narrow bandwidths that are achieved with the DFT are useful for detection and observation of weak signals. Fig 10.41 is the Spectrum Analyzer display from that radio while receiving weak carriers. Signals below about -150 dBm are too weak to be heard by the ear, but narrow bandwidths of the DFT make these easily

seen on the display. The DSP-10 also uses the DFT outputs to provide weak signal communications modes. This is illustrated by examples in Chapter 12.

Other DFT Applications for Signal Processing

The spectral power data is useful for understanding the nature of signals being received. There are characteristic signatures or “looks” for particular modulation forms. CW, SSB, FM and data signals can be identified by their spectrum, without knowing any details of the information content. In addition, the DFT can be used to provide data for other functions, such as FM squelch, noise blankers and a transmitter predistorter that is discussed below. In the case of the FM squelch, the presence of a signal causes a reduction in the high frequency noise from the FM detector. By examining the power in various DFT outputs it is possible to sense the presence of a signal. In a similar way, comparing the various outputs of the DFT can sense the broadband nature of impulsive noise.

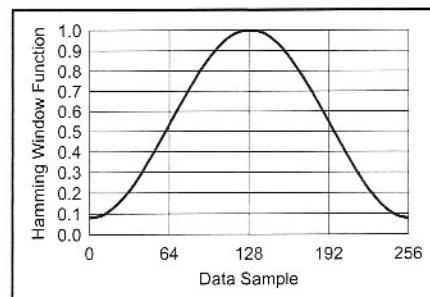


Fig 10.42—The Hamming window function, used to weight data sets to reduce spectral spreading. The data point values are multiplied by the corresponding window function to taper the values to small levels at the beginning and end of the data set.

Windowing of DFT Data

A DFT operates on a fixed number of data points, collected at a uniform rate. The DFT behaves as though the signal went on forever, but with the assumption that the next set of samples will look exactly like the set we measured. And the next, as well... This is all fine except that it is highly

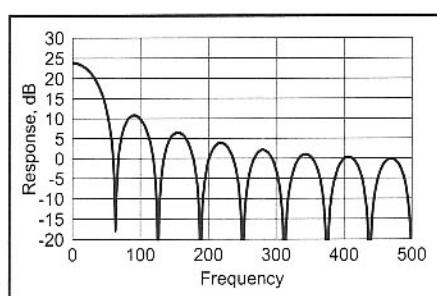
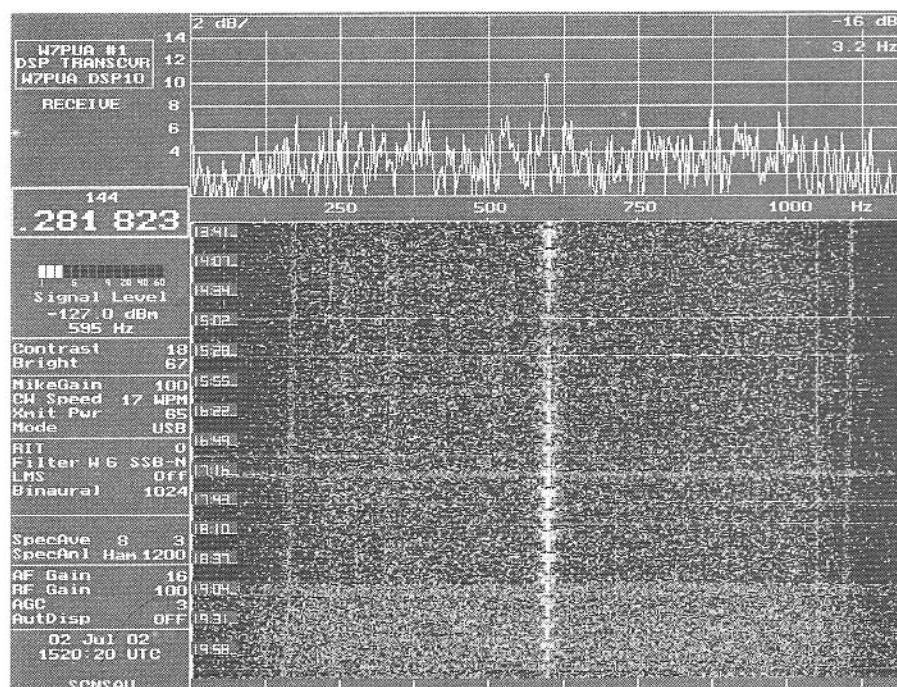


Fig 10.40—Response of a Low-Pass filter constructed by summing 16 data samples together, as occurs in the DFT. The data was sampled at 1000 per second.

Fig 10.41—A Spectrum Analyzer display while receiving weak signals with the DSP-10. Signals below about -150 dBm are too weak to be heard by the ear, but the narrow bandwidths of the DFT make these easily seen on the display.

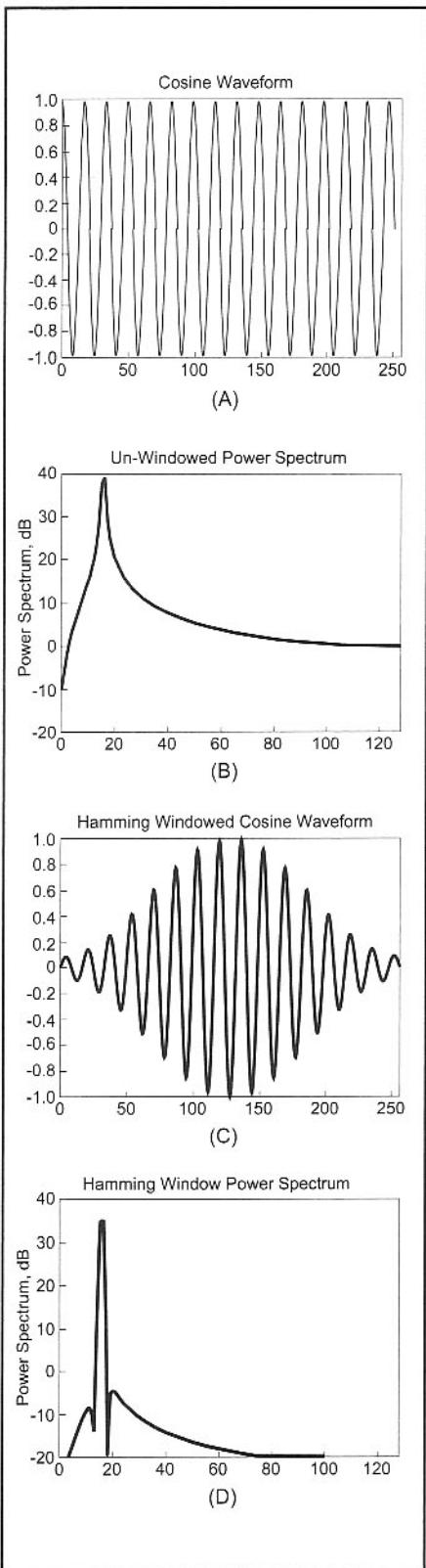


Fig 10.43—Illustrating the use of windowing to minimize spectral leakage, the figures show (a) a cosine waveform, chosen to not meet up at the endpoints, (b) the resulting unwindowed DFT power spectrum, (c) the same cosine waveform with a Hamming window applied, and finally, the much narrowed DFT power spectrum from the windowed waveform (d).

unlikely that the last point of the data set will end on the same value as it started with, or with the same slope, and the same curvature as it started. As a result, there is almost always a major jump (discontinuity) when passing between the end points. The spectral energy of this jump is spread over all frequencies and tends to be strong enough to overwhelm a low-level signal near the frequency of a strong one. The jump causes a “sidelobe structure” that drops off very slowly in frequency. The term “leakage” is often used, as the signal at one frequency appears to leak to other frequencies. This makes for a measurement of limited utility.

The best solution to this jump problem is to taper the data towards zero in the region near the edges of the sample period. If the data at the edges is zero, then the jump will also be zero. There are endless ways to taper the data and they are called *windowing functions*. A classic curve, shown in Fig 10.42, is the Hamming window. It has a first sidelobe down 43 dB. Many alternative windowing functions have been devised with an excellent summary in the book by deFatta, et.al.²⁰

Experimentation is involved in select-

ing a windowing function. Each of these functions represents a distortion of the input data and a tradeoff must be made between distorting the data and the spreading of the spectrum from leakage. The usual data distortion makes spectral widths appear wider than they are; this is often quite an acceptable compromise.

Figure 10.43 shows the DFT of a cosine wave, with and without a Hamming window. The waveform without windowing (a) has been chosen to not have the last data point line up with the first one. This results in the wide and poorly defined power spectrum in (b). Application of the Hamming window results in the tapering of the data as seen in (c). The improvement in the associated power spectrum is seen in (d). Several imperfections remain. The spectral width is not a single narrow line, but overlaps 2 bins at the top and more down the sides of the spectral estimate. In addition, once 40 dB below the peak of the spectrum, the width gets quite broad. To some extent, these imperfections are part of having only a sample of the waveform and therefore making only an “estimate.” However, by changing the windowing function, one can trade off the areas where a compromise is made.

10.11 AUTOMATIC NOISE BLANKERS

Noise blankers attempt to determine when a broadband noise pulse is present and during that period to “turn off” the receiver processing. Both of these functions can be performed in DSP. Two general problems exist in the operation of this type of noise blunker. Signals can be interpreted as noise, causing cross modulation onto the desired signal from the interfering signal, and the blanking process may introduce unwanted signals that resemble the interference. The design must attempt to minimize these problems, but to some degree noise blankers will have these characteristics.

Most noise blankers attempt to use the bandwidth of the interfering noise as an identifying criteria. Impulsive types of noise tend to have short duration, and to be quite strong in a wider-band receiver. This type of signal produces a rapidly rising pulse, limited by the bandwidth of the measurement. For instance, an IF bandwidth of 10 kHz can pass an impulse noise signal with a rise time of about 70 micro-

seconds. The fastest rise time for a 3-kHz SSB signal is over 200 microseconds. A satisfactory blunker can result if one is able to provide the wider bandwidth and identify the strong signals with fast rise times. Often DSP IF bandwidths may not be as wide as desired and this can be a limitation of the noise blunker operation.

The blanking operation is ideal for DSP implementation. As was discussed in mixer operation, the simple act of multiplying two signals together is “double balanced” and neither input signal is fed through to the output. When the blanking operation is in an off state, the signal can be completely removed. Alternatively, a substitute signal can be created that is the prediction of the desired signal, based on its past characteristics. For a simple example, if the input signal was a CW tone, it would be logical to continue the last tone that was not blanked. Some delay is needed to give time for the blanking decision to be made. This delay can be implemented in DSP in a few proces-

sor instructions. More general predictors are also possible for cases such as noise input or a SSB signal.

Fig 10.44 shows a block diagram of a DSP implementation of a noise blanker. The envelope detector determines the maximum amplitude of the IF signal. It would look at both the positive and negative excursions of the signal in order to respond, as quickly as possible, to any rapidly rising noise burst. A 2500-Hz low-pass filters extracts the signal envelope. In a similar fashion, the output of a 12-kHz filter responds to all signals present in the pass band. If only the desired signal is present, the outputs of the two filters would be very similar. However, a noise burst would produce a greater response from the wider-band filter. This difference can be sensed by taking the ratio* of the two outputs. A comparator can sense if the noise response is over a threshold and then produce a blanking signal.

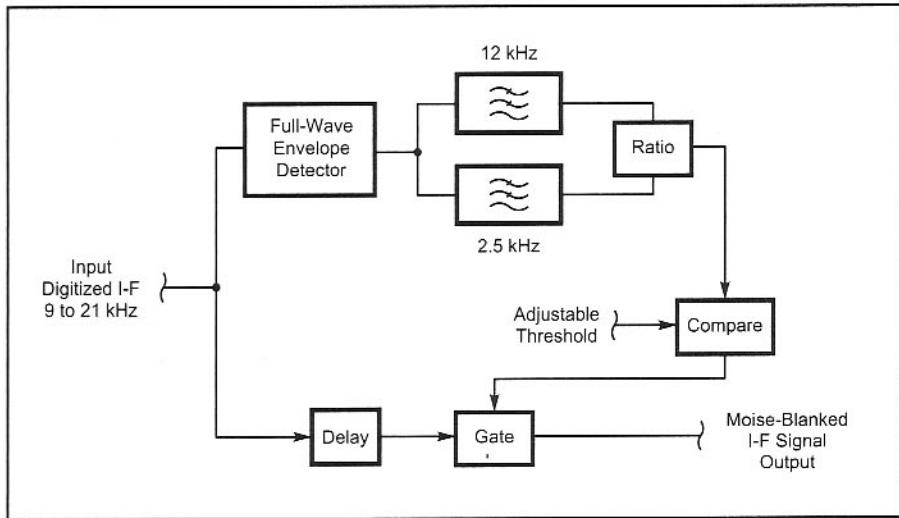


Fig 10.44—Block diagram of a noise-blanker suitable for implementation as a DSP function. An envelope detector follows the amplitude of the wide-band (12 kHz) signal. Two low-pass filters are used to determine the presence of a noise burst, which then gates the received signal. A signal delay allows time for the decision making.

10.12 CW SIGNAL GENERATION

We have discussed the generation of a sine wave and gating this on and off can generate crude CW signals. It is well known that spectral broadening (key clicks) will result from sudden on/off transitions. The keying can be made to have much better transitions by treating the process as amplitude modulation as shown in **Fig 10.45**. Here the logical signal from the keying device is placed through a low-pass filter to convert it to an analog signal of limited bandwidth. The process of amplitude modulation then produces a spectrum that is twice as wide as the limited bandwidth.

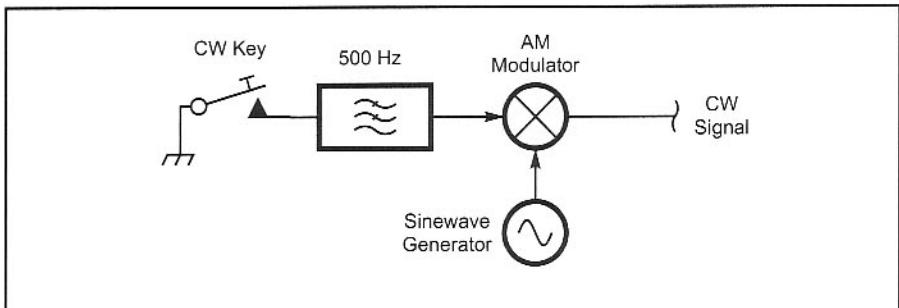


Fig 10.45—Block diagram of a CW generator using pulse shaping and an amplitude modulator. This limits the spectrum of the keyed waveform. The AM modulator in its DSP implementation is a multiplication of the two signals.

10.13 SSB SIGNAL GENERATION

All of the techniques for SSB generation shown for analog equipment in Chapter 6 can be implemented in DSP. Often the most attractive approach is the phasing method as was discussed in Chapter 9. The challenges of tight component tolerances and component drift are not problems in the software implementation and high carrier and opposite sideband rejections are

easily achieved.

As an alternative to the phasing method, it is practical to implement a filter type of SSB generator. Typically this would utilize an IF in the 5- to 25-kHz range and analog mixing to convert the results to the operating frequency.

The FIR filters, mixers and sine wave generators shown above can be combined to implement a DSP IF sideband generator.

Alternatively, it is practical to have a hybrid analog/digital approach where the two quadrature audio signals are generated in the DSP and the mixers and conversion oscillator are conventional analog components. This approach lends itself to error compensation for the analog compo-

nents. An example of this approach is the 18-MHz transceiver of Chapter 11.

Predistorter Distortion Reduction

SSB signals are raised in power level by amplifiers that often have intermodulation distortion products only 25 to 35 dB below the peak transmitted level. These distortion products are spread in frequency and can cause interference in adjacent channels. One can limit these product levels by reducing the output level of the amplifier or operating the amplifier in Class A; doing this results in poor dc-to-RF power efficiency for the amplifier.

*Division is not usually a fast operation in a fixed point DSP microprocessor. It is often desirable to find the logarithm of two values and subtract them. For applications such as the noise blanker, the logarithm function does not need high accuracy and can be implemented as a series of straight lines. This can be a relatively fast process.

One alternate solution that allows the efficiency to remain high while reducing distortion is called predistortion. For example, if the only amplifier distortion was gain compression, as shown in Fig 10.46, one can imagine that the distortion could be removed, if a gain-expanding pre-distorter was placed ahead of the amplifier. The predistorter would have the opposite gain characteristic to the amplifier, as shown in the upper part of the figure. For an analog implementation, it might be possible to use some diodes ar-

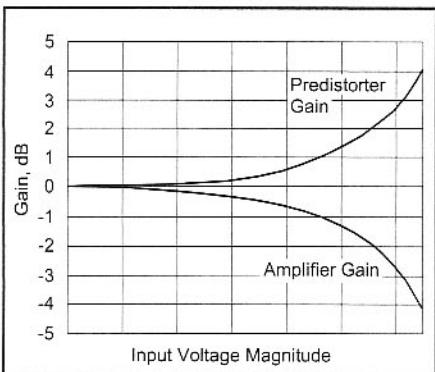


Fig 10.46—Amplifier (lower graph) and predistorter gain characteristics. The two devices are cascaded to result in a net gain that is always 0 dB. The gain of the devices is shown as 0 dB for low-levels, which is not usually the case and these, should be thought of as relative gains.

ranged as shown in Fig 10.47. If we were fortunate, the diodes would provide the proper amount of gain expansion to remove the inherent gain compression of the amplifier, at least over a restricted operating range.

A more elaborate gain expander can be built using the computational ability of a DSP device. It is presented here to indicate the potential for DSP components to improve the distortion performance as well as to suggest some possible directions that could be explored. This is not an implementation of a predistorter, but rather a conceptual treatment. The ambitious experimenter is encouraged to pursue this area since the potential benefits are substantial.

An example of such an implementation is shown in Fig 10.48. A polynomial is shown as the gain expansion curve. Within broad restrictions, it is possible to approximate a gain expansion curve to any precision by using enough terms in the polynomial. Results from a simulation* of an amplifier and predistorter are in the shown in Figs 10.49 through 10.52. In this example, the amplifier is modeled as a linear amplifier of gain 1.0 (0 dB) along with a cubic distortion term, which is often the dominant distortion for amplifiers. For those inclined to describe this mathematically, the output voltage, v_o , in terms of the input voltage v_a is:

$$v_o = v_a - 0.1v_a^3 \quad \text{Eq 10.12}$$

where the 0.1 multiplier is chosen to be convenient as an example. If two sine waves of equal 1.54-V peak-to-peak input are applied to the amplifier without predistortion, the resulting intermodulation spectrum will be that shown in the Fig 10.49. Here the intermodulation products are about 31 dB below the peak output; this is probably typical of the levels found in linear power amplifiers.

Next a mathematical predistorter was

placed ahead of the amplifier. It is a simple polynomial device that has an output/input relationship:

$$V_a = V_i \times (1.0147 - 0.0409V_i^2 + 0.1930 V_i^4) \quad \text{Eq 10.13}$$

The coefficients for this predistorter were found by curve fitting with a spreadsheet program to be close to the inverse of amplifier distortion. The squared and fourth power terms treat the positive and negative waveform values in an identical manner, which is a computational convenience. This is only an example of a predistorter polynomial. The selection of the polynomial complexity, or choosing a different form of predistorter, is all part of the design process.

Fig 10.50 shows the input waveform for

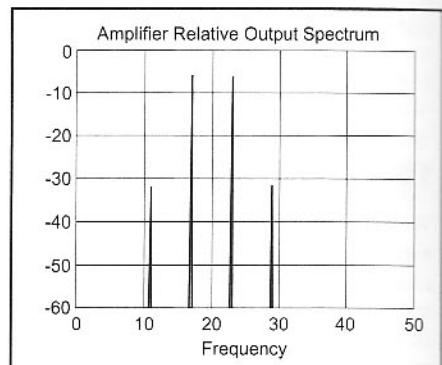


Fig 10.49—Amplifier output spectrum showing the two desired signals at frequencies of 17 and 23 and the third-order intermodulation products at frequencies of 12 and 29. These frequencies were chosen to be easy to simulate, but the results apply generally to any two-tone test frequencies. There are no intermodulation products of order higher than three, for the amplifier as it was modeled.

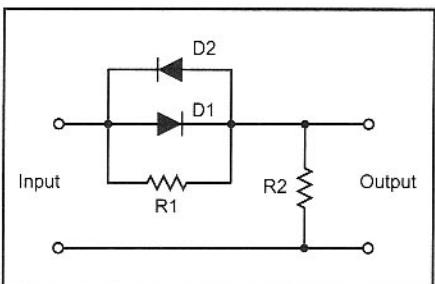


Fig 10.47—Schematic diagram of a simple gain expanding predistorter. This analog circuit is constrained by available diode types, but does provide a general gain characteristic that is opposite to that of amplifier gain compression.

* The simulation was done with MATLAB. The script is included in the *Experimental Methods in RF Design CD* as the file "predis1.m."

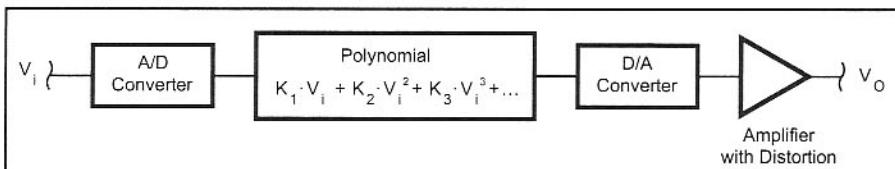


Fig 10.48—Block diagram of a gain expander that could be implemented in a DSP system. The A/D and D/A converters are shown to emphasize the points where the signal has a digital form. In general, it would be combined with other digital blocks. As the complexity of the polynomial gets greater, the potential for reducing distortion improves.

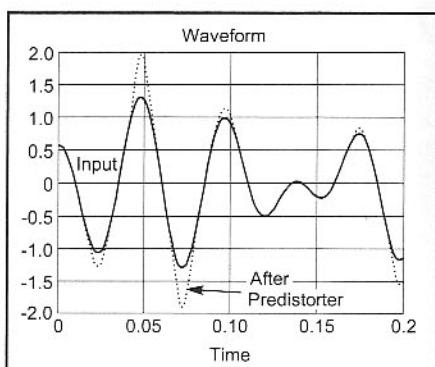


Fig 10.50—Waveforms before and after the predistorter. Only the extreme voltages are increased by the predistorter. This increases the drive to the amplifier to overcome the amplitude compression in the amplifier.

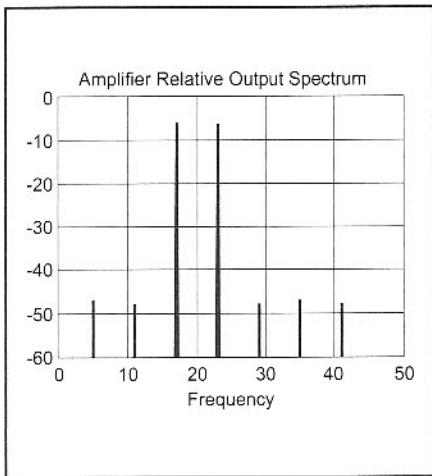


Fig 10.51—Output spectrum for the same amplifier as used in Fig 10.49, except with the predistorter ahead of the amplifier. The third-order products have been reduced by about 17 dB. Fifth and seventh order products can be seen on either side of the third-order products. The predistorter and its interaction with the amplifier characteristics introduced these.

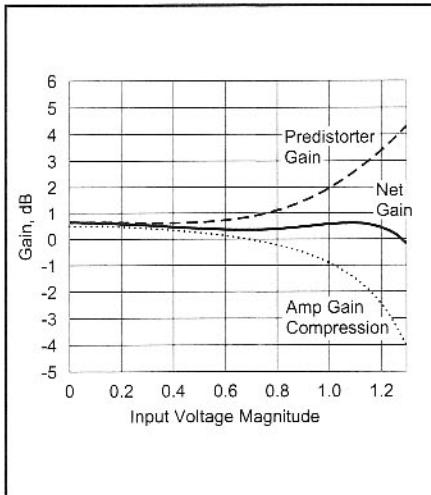


Fig 10.52—Simulated amplifier and predistorter gain characteristics. The predistorter has been designed to minimize the error in the net gain for voltages from 0 to 1.25. All voltages are referenced to the input to the predistorter, and the input to the amplifier can be greater due to the predistorter gain expansion.

the simulated amplifier, both with and without the predistortion. For small signals the predistorter has no effect on the waveform. This seems reasonable, since small signals tend to have very little amplifier distortion. As the signal levels exceed 0.5 V the effect of the predistorter become significant. The drive level is increased considerably on the waveform peaks. As the amplifier output tries to compress, the predistorter drives it enough harder to bring it back to linearity. **Fig 10.51** is a plot of the resulting amplifier spectrum when the two desired outputs have the same level as for Fig 10.49. The third order intermodulation products are now about 48 dB below the peak output, an improvement of 17 dB.

The gain characteristics for this example are shown in **Fig 10.52**. The amplifier gain is down about 2.6 dB for an input level of 1.20 V. For this same level, the predistorter has a gain increase of 2.6 dB and the net gain is about 0 dB, representing no distortion. Below this level, the correction is not perfect, but stays within about 0.2 dB of 0 dB.

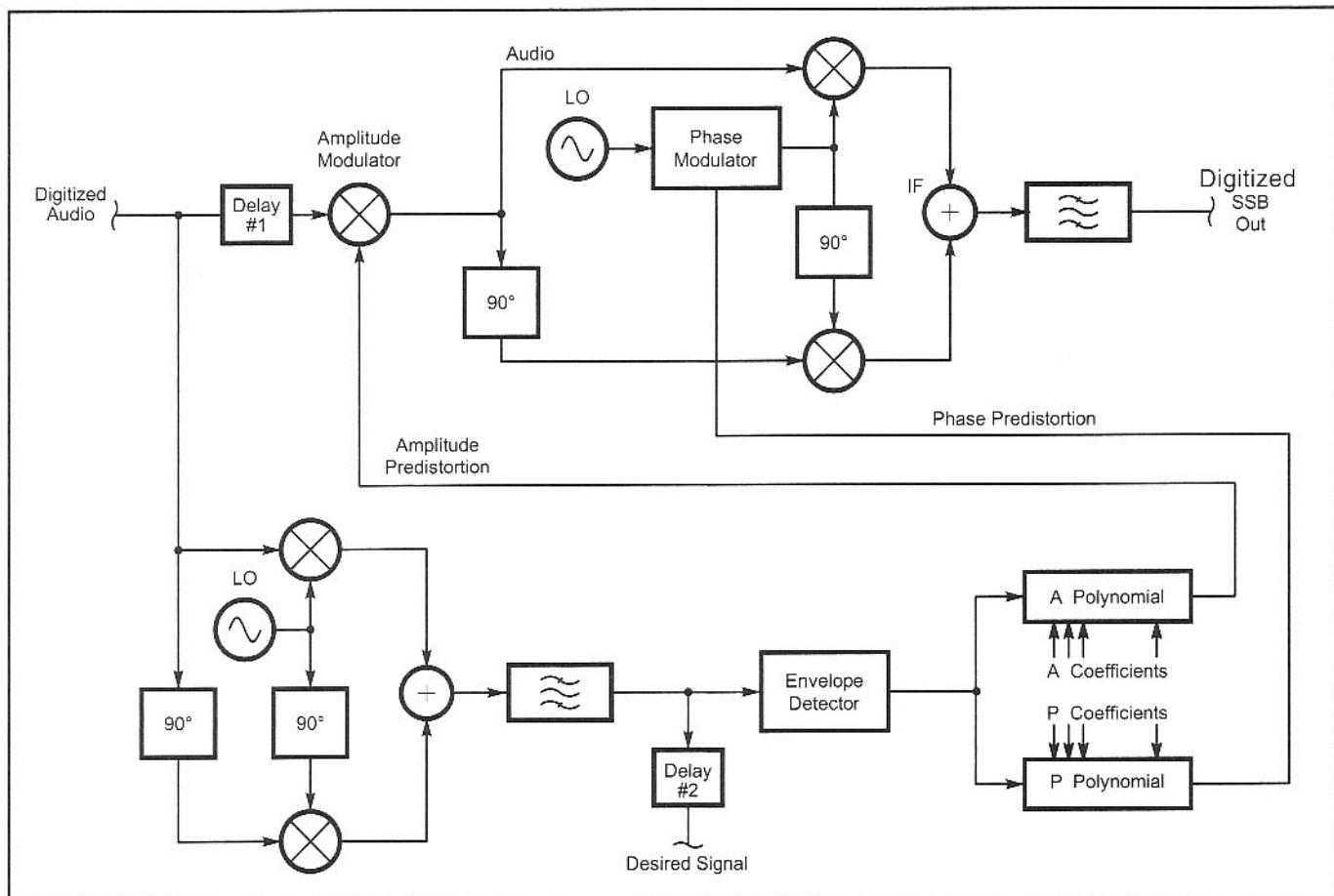


Fig 10.53—Block diagram of a SSB transmitter with predistortion in both amplitude and phase. The lower portion of the diagram is conventional phasing type of SSB generator that serves to determine the desired envelope amplitude, which determines the polynomial predistortion. All components shown are implemented in DSP.

If this predistorter was applied to a real amplifier, the results would be disappointing. This is because we have built a paper amplifier that has no phase distortion at large signal levels. Transistor amplifiers are not this simplistic and require correction for phase as well as for amplitude. However, the technique shown above works equally well for phase corrections. A polynomial of the input voltage can be used to determine the needed phase predistortion. **Fig 10.53** is a block diagram of a SSB transmitter with both amplitude and phase corrections being applied. It is necessary to know the envelope of the desired signal and the lower SSB generator in the figure serves this purpose. Amplitude and phase modulation for the predistortion can be applied to a second SSB generator as shown. All local oscillators (LO) are at the frequency of the (suppressed) transmit I-F carrier.

In general, it is not satisfactory to use a fixed set of coefficients for the polynomials. Time, temperature, load impedance and other factors will change these. This suggests a feedback process that can observe the success of the predistorter and attempt

to improve this by changes in the coefficients. The first step in such a process is to make a measurement of the amplifier output distortion. This could be a spectral analysis of the output spectrum, since we desire to not have any power outside a particular frequency band. The spectral analysis can be done by converting the frequency of the amplifier output back to a low frequency and applying a DFT to the signal, using DSP. Alternatively, one could take the converted signal and compare it with the desired signal in Fig 10.52, attempting to make the amplifier output a multiplied replica of the drive signal. This again is straightforward in a DSP implementation, but one must allow for delays and constant phase shifts that occur in the amplifier.

Next, a process for changing the predistortion polynomial coefficients must be designed. This can proceed at a slow rate relative to the changes in the transmitted signal. It is only necessary to follow temperature or other long-term affects. A number of sophisticated procedures exist for determining the coefficients.²¹ But, it is possible to get good performance from operations as simple as

trial-and-error. This, easy-to-follow procedure changes one of the coefficients by a small amount and then observes the amplifier output. If the distortion is reduced, the change is left. If not, a trial in the opposite direction is made. A lack of improvement at this point means that the original coefficient was satisfactory. Then the procedure repeats the steps for the next coefficient. So long as the starting coefficients are not totally unreasonable, this will normally progress to the optimum set of coefficients.

Fig 10.51 shows that 5th and 7th order intermodulation products have been introduced by the predistorter. These high-order products are potentially more harmful than the original, but larger, 3rd order product. The high order products are controllable in amplitude by a combination of the operating level and the predistorter design. Care should be taken to evaluate these effects.

Predistortion systems can be seen to have some complexity in their operation. But the rewards are quite great. Not only does the amplifier distortion reduction mitigate "spectrum pollution," but the efficiency of the amplifier is effectively improved.

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1. D. Smith, *Digital Signal Processing Technology*, ARRL, 2001.
2. P. Horowitz and W. Hill, *The Art of Electronics*, Cambridge University Press, 1989, Chapter 9. This is a discussion of A/D converters including sigma-delta.
3. D. Garcia, "Precision Digital Sine-Wave Generation with the TMS32010," paper #8 in *Applications Manual, Digital Signal Processing with the TMS320 Family, Theory, Algorithms and Implementations, Volume 1*, Texas Instruments, 1986. This gives a good discussion of the approximation tradeoffs associated with lookup tables. Program listings are specific to the TMS32010, but the discussion is quite general.
4. *Digital Signal Processing Applications Using the ADSP-2100 Family, Volume 1*, Prentice-Hall, 1992.
5. D. J. DeFatta, J. G. Lucas, W. S. Hodgkiss, *Digital Signal Processing: A System Design Approach*, John Wiley, 1988. This is a great book, if you are comfortable with some college level math, but it is not a math book like some DSP books!
6. W. H. Press, S. A. Teukolsky, W. T. Vetterling, B. P. Flannery, *Numerical Recipes in C*, Cambridge University Press, 1992. This book discusses the background, implementation and limitations of the method, as well as a large number of computer methods for numerical calculations.
7. P. Horowitz and W. Hill, *The Art of Electronics*.
8. See Reference 4.
9. W. Davenport and W. Root, *An Introduction to the Theory of Random Signals and Noise*, McGraw-Hill, 1958, Ch. 5. The Central-Limit Theorem of statistics states that under some very general conditions, the sum of a number of random variables approaches the Gaussian distribution as the number gets large. Most college level statistics books cover this theorem as well as signal analysis books such as this one.
10. *The ARRL Handbook for Radio Amateurs*, ARRL, 2002. Chapter 18 contains an introduction to the Fourier transform.
11. The FIR filter design program is included on the CD-ROM for this book as FIRDES1.BAS. The Basic program will run on most Basic interpreters such as have been included with DOS and Windows™ operating systems up through Windows98™.
12. J. Forrer, "A DSP-Based Audio Signal Processor," *QEX*, September, 1996, pp 8-13.
13. U. Rohde, personal correspondence with Wes Hayward, 1997.
14. *The ARRL Handbook*, reference 10 above, includes examples of several types of FM detectors.
15. Reference 4, Chapter 4 includes an Arctangent routine that could be used as the basis for an FM detector.
16. E. O. Brigham, *The Fast Fourier Transform*, Prentice-Hall, 1974. For those comfortable with the concepts of calculus, this is a wonderful reference book. The Discrete Fourier Transform properties and the "fast" implementations are both well covered. Similar material is covered in R. W. Ramirez, *The FFT Fundamentals and Concept*, Prentice-Hall, 1985. In addition, there is a summary of the DFT in the *ARRL Handbook*, Reference 10 above.
17. Chapter 6 of Reference 4 contains a variety of FFT routines.
18. Section 14.5 of Reference 4 contains an implementation of the Goertzel algorithm for DTMF decoding.
19. R. Larkin, "The DSP-10: An All-Mode 2-M Transceiver Using a DSP IF and PC-Controlled Front Panel," *QST*, in three parts, Sep 1999, pp 33-41; Oct 1999, pp 34-40; Nov 1999, pp 42-45.
20. See Reference 5.
21. T. R. Cuthbert, Jr., *Optimization Using Personal Computers With Applications to Electrical Networks*, John Wiley & Sons, 1987. This book covers the mathematical side of optimization and is good for those wanting to spend some time on the subject. Knowledge of Calculus and Linear Algebra is required to fully use the material, but BASIC programs and examples are provided for those who wish to approach the subject experimentally.



DSP Applications in Communications

In Chapter 10 a number of DSP building blocks, such as oscillators, filters and modulators were explored. In many cases the blocks were alternatives to traditional analog functions, while in other cases, such as the discrete Fourier transform, we are introducing functionality that was not previously practical. In this chapter, we will explore methods for combining several blocks to produce a piece of communications equipment. We will be integrating three types of functions:

- Traditional analog components, such as RF amplifiers and RF mixers.
- DSP components, such as were covered in Chapter 10.
- Controls for both of these types of components. Most often this is associated with operator interaction, involving both displays and interface controls.

The control of the communications equipment can usually be improved by some sort of computer, which is often a dedicated microprocessor. This may be a good approach, depending on the complexity of the devices. An alternative, however, is to use the same DSP device that is processing signals to do the control functions. This approach will be used several times in this chapter, with the result of needing less total hardware and only a single computer program.

The journey of an experimenter who decides to investigate these DSP projects will begin with the EZ-KIT Lite from Analog Devices. The first things that might be done with this DSP board are simple demonstrations such as audio filters, which are well described in the manuals supplied with the board. Several of these can be tied into

an existing receiver and used directly for on-the-air experiments.

This chapter focuses on the processing of signals, but before getting to that we need to look at some basic control techniques. The first issue we will address is that of computer interrupts, which are fundamental to having the DSP programs operate in synchronism with the attached hardware.

All the DSP programs needed to bring life to these projects are included on the CD-ROM with the book and are not repeated in the text. Shown in this chapter are a few fragments of the programs to illustrate a number of detailed operations. It is recommended that the reader look at the complete program, on occasion. This gives a “big picture” view of combining fragments into a working DSP program.

11.1 PROGRAM STRUCTURE

All computer programs have some form of overall structure, ranging from trivial to excessively complex. Often times the structure is largely determined by a group of programs, collectively referred to as an *operating system*. For a PC, this constrains all programs to certain conventions while allowing multiple programs to share resources, such as memory or processor time. To the person writing a program this can be both a convenience as well as a source of anxiety. Having a set of subroutines available to handle standard operations can speed up program writing. However, if there are multiple users of resources, there may be no guarantee that a particular program will finish its task

when needed. “Real-time” programming becomes problematic under these circumstances.

For simple DSP programs, it is often possible to operate with no real-time operating system. All resources are allocated when the program is designed. The overhead of the operating system is avoided and the programs are guaranteed to complete their tasks on time. All the programs in this chapter will use this approach and have same structure. This consists of a background program that processes all data that has no time deadlines, and a single *Interrupt Service Routine* (ISR) that includes all routines that must be completed on a periodic basis.

Interrupts

As discussed in Chapter 10, data processing devices require some method to change the program operation, based on some electrical input. Called interrupts, these methods involve some internal dedicated hardware to make changes to the processor state. Normally the minimum operation is a change in the address of the program being executed. The programmer must have placed appropriate instructions at the interrupt-altered address.

A complication for interrupt programming is the potential for multiple interrupts. For example, in a DSP program, these might be an operation to output data to a D/A converter and a need to output

serial data to a serial port. The first interrupt might come from the D/A converter and the second from a hardware timer that is often built on the same IC as the DSP device. The programmer must ensure that these two interrupts will be processed correctly, regardless of when the interrupts occur, including the case of one interrupt occurring while a second interrupt is being processed. For our example, the data to the D/A converter must be processed before the next D/A request is received. If this is not done, there will large amounts of signal distortion associated with a missing data output.

A simple plan that ensures a minimum amount of time will be available for interrupt processing is to use only one interrupt that occurs on a periodic basis. Although this may require some planning to accommodate all processes, the simplicity of this

scheme opens additional interrupt processing time in two ways:

- There is no possibility of two interrupts occurring at the same time and therefore no worst-case timing constraints to allow all processes to be finished

- No communication is required between processes about tasks that need to be performed. That is, the operating system is built-in to the program at design time.

If there is only one interrupt, all interrupt processing should be completed in one period, leaving the system free at the time of the next interrupt. This is the way that communication between tasks is minimized. This processing should include everything that needs to be completed before the next interrupt.

Additionally, any process that does not need to be completed before the next inter-

rupt should be placed into the background process. Examples of this are the updating of data for a display or the reading of a knob or a switch. Again, these processes can be arranged in a sequential order with no need to monitor the time increment needed. So long as the interrupt process leaves any time at all, the background will be processed. Determining whether this is happening at a fast enough rate can be done at design time. It will only happen more slowly if it is being monitored by some part of the process.

Fig 10.6 in the previous chapter illustrates the single timed interrupt structure used for all of the projects in this chapter. Even more elaborate processes, such as the DSP-10 transceiver (only outlined in this chapter but included on the book CD), will continue to use the same structure.

11.2 USING A DSP DEVICE AS A CONTROLLER

The “S” in *DSP* is for *signal*, and one usually thinks of such a microprocessor as being for signal handling functions. However, applications usually need some form of control functions, in addition to processing signals. As will be seen it works quite well to use the same processor for control purposes, resulting in an overall reduction in hardware and software complexity by eliminating the need for a separate controller and the associated interfacing. All of the control program can be implemented as a background activity that essentially runs on a “time available” basis. This way the time critical functions such as signal generation or filtering are not affected. The following discussions of the rotary encoder and an LCD panel are examples of using the DSP device as a general-purpose controller.

Rotary Encoder

Simple control functions can use push buttons to communicate our desires to the DSP. But if a numerical value is to be transmitted push buttons can be awkward, and we must look to either a keyboard or a rotary knob as a control device.

A knob is often easier to use for applications such as changing a frequency. Reading the position of a knob is commonly done with a *rotary optical encoder*.¹ This operates by shining an LED light source through an encoding pattern onto a pair of optical sensors. The encoding pattern rotates with the knob. After conversion to logic level signals, the out-

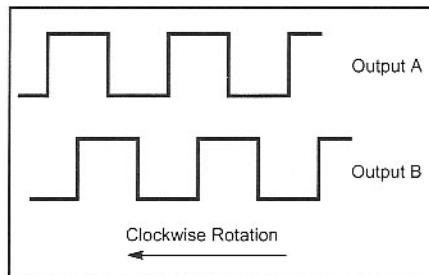


Fig 11.1—This diagram shows the logic levels that occur at the two rotary encoder outputs, as it rotates. At no time do both of the outputs change levels simultaneously.

puts of the sensors take on the pattern shown in **Fig 11.1**. The sequencing of the two outputs, A and B, prevent their changing at the same time. The logic that determines the direction of turning proceeds as follows. If output A and output B are both low, the next change will be to high on output B if the motion is clockwise. If instead, the next change is to high on output A, it would indicate counter-clockwise rotation. For all four combinations of high and low, we can make a similar determination by examining the figure.

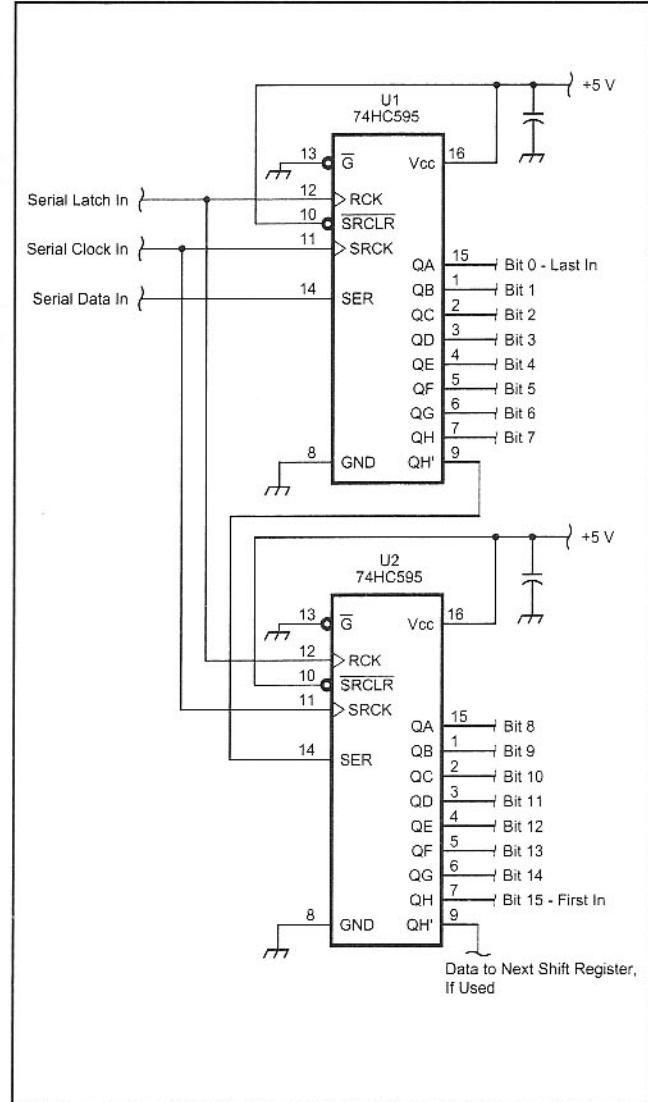
Once the direction of rotation is determined, a counter can be increased or decreased at each transition. Implementing this counter with digital hardware is a possibility, but the example here uses a DSP software implementation. The counter output can control the frequency of an oscillator or other such functions.

Three-Wire Serial Interfaces

Serial hardware interfaces are common for communicating between devices. This simple interface is often implemented using three wires, a **data** wire, a **clock** wire to tell when the data is valid and a **latch** wire to tell when the new serial data should be used. This is compatible with shift registers used as receiving devices. Since the data is never used until a latch signal is applied, it is possible to share data and clock lines, as will be seen below. In addition, serial devices are often built to be cascaded allowing multiple devices to be talked to with a single set of wires.

An example of expanding the serial interface to multiple devices is **Fig A** which uses two cascaded shift registers to double the number of parallel outputs to 16. The QH' output is intended for cascading the shift registers. The number of outputs can be increased this way without limit other than the increase in time required to make a change in the outputs.

Many standard functions, in integrated-circuit form, are available with a serial interface. Examples are frequency synthesizers, A/D converters and D/A converters. Often it is possible to cascade



serial devices using a common set of three serial programming lines. This requires more clocking events per program, but the time for this activity is often available.

For example, **Fig B** shows a serially programmed National LMX1501A frequency synthesizer cascaded with an 8-bit shift register. The shift-register arrangement is identical with that of Fig A, except that the cascading output QH' is used to send data on to the frequency synthesizer IC. The data passes through the shift register and on to the internal shift registers of the synthesizer. Common clock and latch lines are used for both devices. We need to be careful that all timing constraints for the various devices are met. An example of such a constraint is the RC network on the data line going into the synthesizer. This provides a delay of about a half microsecond, guaranteeing that the synthesizer has clocked in the data from QH' before it changes

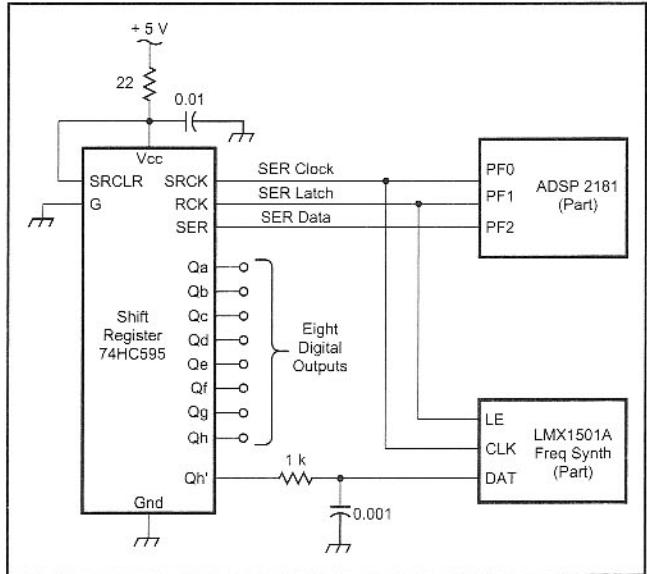


Fig B—Schematic diagram of two cascaded serially programmed devices requiring only three wires from the controller.

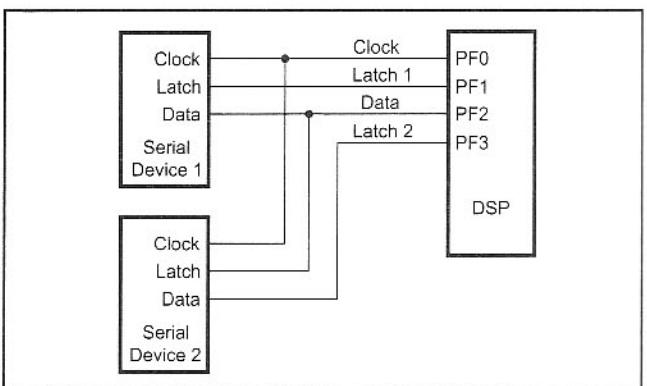


Fig C—Schematic diagram of two serially programmed devices sharing data and clock wires, but having individual latch lines.

due to the clock signal. Some devices may clock fast enough for the network to not be needed, but this must be examined on an individual basis.

Sometimes the time required to program a very long serial stream is excessive, or the serially programmed device may not have an output to support cascading. For these cases, it is possible to share data and clock wires, but to have separate latch wires as is shown in **Fig C**. The data is clocked into both devices at the same time, but only the device receiving a latch signal will act on the data.

The three-wire interface is quite flexible in its usage. In many cases it is the only form for which a particular device may be available. However, in some sense it transfers the simplicity of the interface back to the software that provides the drive. This generally is a satisfactory result since wiring up parallel interfaces with 8, 16 or possibly more wires is very repetitious and not as challenging as software!

The particular encoder used here was a Clarostat 600EN-128 with a resolution of 256 changes per rotation. A variety of encoders are available most of which can be adapted to this application, as well as the possibility of a home-built encoder as described in Reference 1.

Many possibilities exist for connecting the rotary encoder to the processor. **Fig 11.2** illustrates one of the simplest ways to accomplish this. Here the two encoder outputs are connected to *Programmable Flag* inputs, PF0 and PF1. These inputs are part of a set of 8 pins that are dedicated to input and output of digital data (I/O). Within the processor these pins can be defined as either inputs or outputs by writing to a memory-mapped register. Once this is done the pin logic levels can be read from a second memory-mapped register. The only constraint on this implementation is the limited number of pins available.

Expansion of the number of digital I/O lines can be accomplished by connecting flip-flops to what is referred to as *I/O Space*. This allows 16 bits to be read (or written) at a time and requires minimal support hardware. An alternative is to continue using the Programmable Flags, but adding serial-to-parallel conversion hardware (shift registers) as is illustrated in **Fig 11.3**. A major advantage of this scheme is its compatibility with multitudes of serially programmed devices (see sidebar "Three-Wire Serial Interfaces"). Referring to Fig 11.3, there are three lines, *data*, *clock* and *latch*, to transmit the serial data from the processor to the shift register. **Fig 11.4** shows the timing diagram for producing 8 bits of parallel data from the shift register. The data line sets the value of the individual bits. After the data line has achieved a well-defined value, the clock makes a zero-to-one transition that loads the current data value into the shift register. This is repeated a total of 8 times, at which point the entire 8-bit byte has been loaded into the shift register. The order of the shift register is such that the most significant bit (*Qh*) is the first bit in, and the least significant bit (*Qa*) is the last bit into the shift register.

To this point, we have converted serial data from the processor into parallel data lines. If we are to read the logic levels of a multiplicity of external lines, it will easily use up the free programmable flag lines. One simple interface that is particularly suited to occasional reading of lines is the digital multiplexer. Figure 11.3 shows the 8-input multiplexer using a 74HC151 IC. The particular line that is to be read by the processor is selected by the 3-bit address coming from *Qa*, *Qb* and *Qc* of the shift

Fig 11.2—A simple hardware interface for use between a rotary encoder and a DSP device having programmable flag inputs. Only one row of the programmable flags of the DSP are shown here.

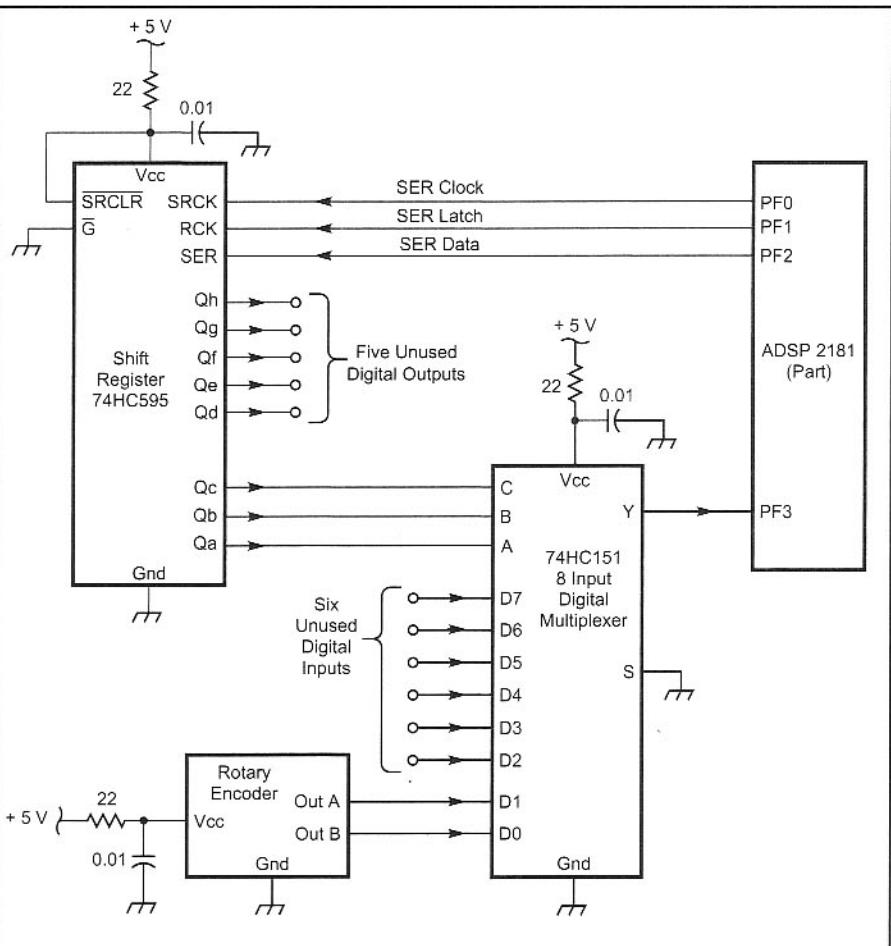
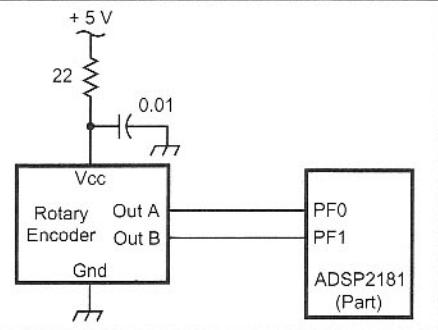


Fig 11.3—An alternative approach to expansion of the number of digital I/O lines is the addition of serial-to-parallel conversion hardware as shown here.

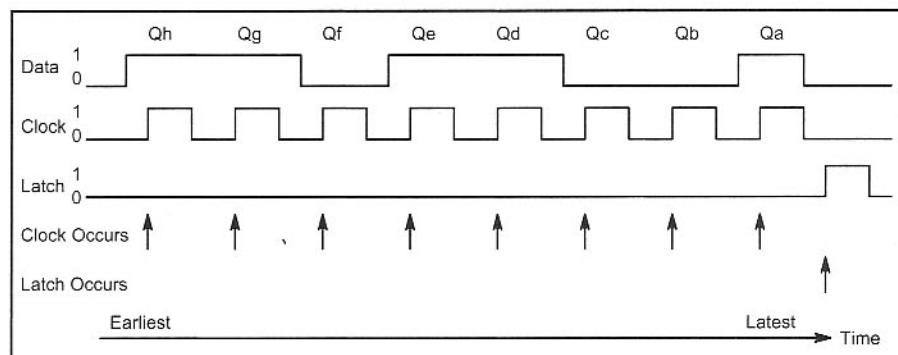


Fig 11.4—Timing diagram for loading the eight-bit 74HC595 shift register with an example binary value of 11011001. Both clocking and latching occur when the signals go from logic 0 to logic 1.

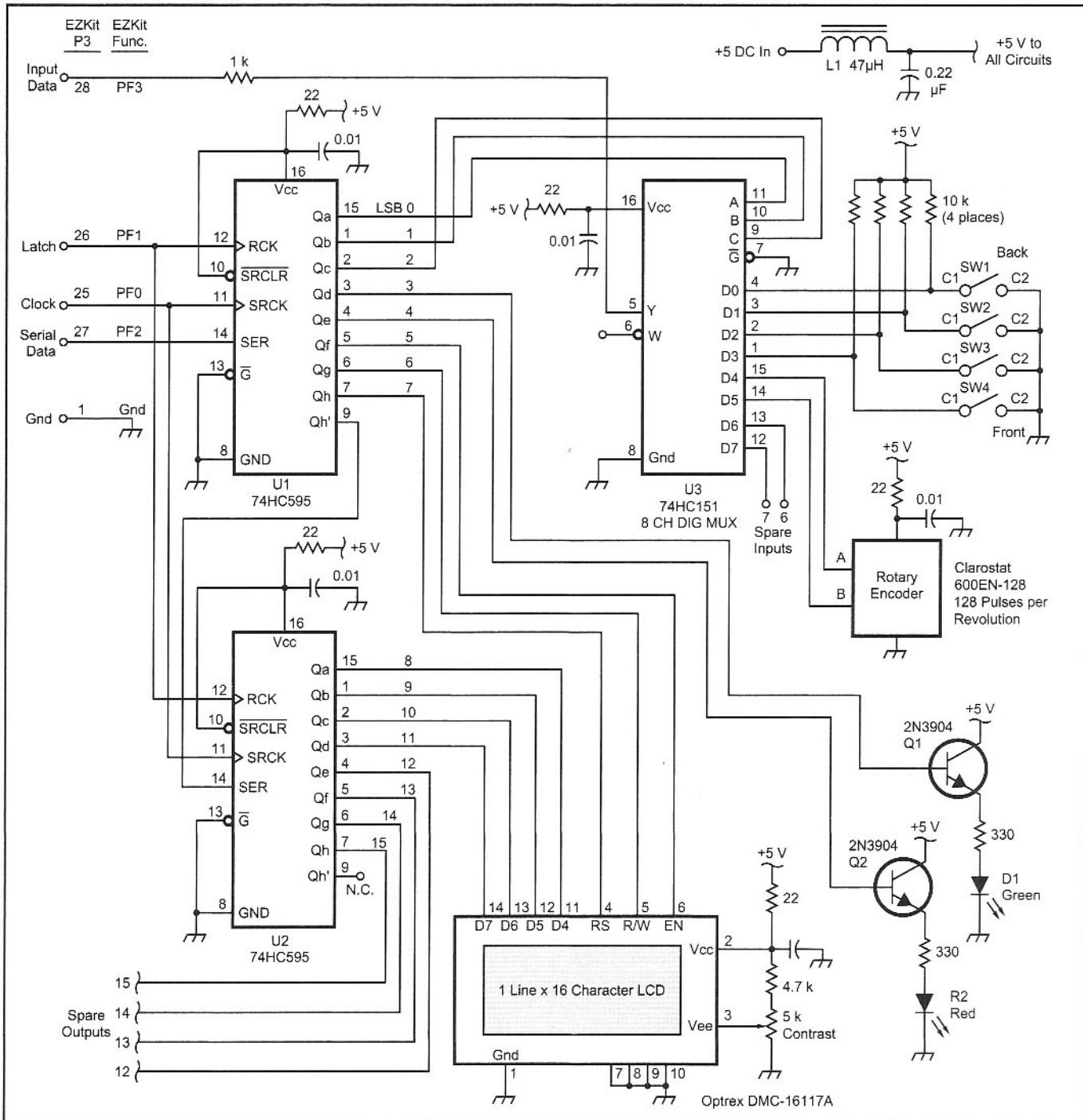


Fig 11.5—Schematic diagram of the hardware interface between a DSP device and multiple control devices, including a rotary knob, four push buttons, two LED indicators and an LCD display.

register. The output of the multiplexer goes to the processor pin PF3. This is programmed to be an input pin during the initialization of the processor.

As a final step in the evolution of control box schematics, **Fig 11.5** shows a complete interface including the rotary encoder for the knob, four push buttons, two LED indicators and a 16-character LCD panel. Four of the parallel inputs are used to read the state of the push buttons. The two LED indicators are driven by simple emitter

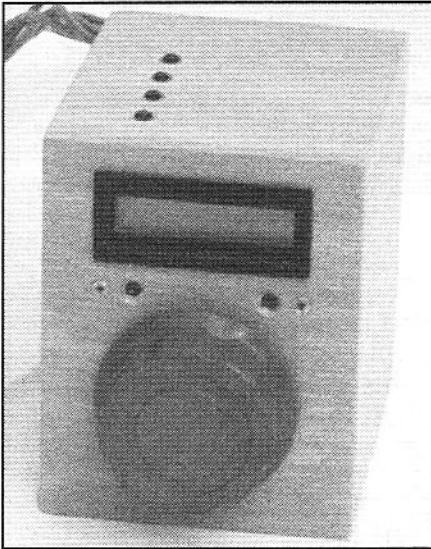
followers, Q1 and Q2, from two of the parallel outputs.

The LCD panel has several options for an interface. Rather simple is the seven-wire arrangement shown in Fig 11.5. Four wires are for data that can be sent a half-byte at a time and the other three wires control the reading of the data by the LCD. All seven wires come from the parallel output interface produced by the shift registers U1 and U2. The control of the LCD panel will be discussed further below when

we look at the methods for using the DSP as a control device.

Programming the Rotary Encoder

A complete example program for the rotary encoder is *C11KNOB.DSP*, included on the book CD. The software is centered on a routine, *knob*. This routine compares the two bits that describe the current knob state with those for the previ-



The knob box was built from thin plywood. An inner box made from scrap circuit board material contains the logic circuitry shown in Fig 11.7. The four push buttons are placed on the top of the box as a convenience in using the box. It is light enough that it wants to move when the buttons are pushed! The LCD display is above the knob. A plastic bezel trims off the display.

ous state and makes one of three choices:

- No Change
- Knob moved counter-clockwise, one count
- Knob moved clockwise, one count

This occurs in the following manner. The inputs come from another routine *inbit* that returns, in register *ay0*, the logic levels of the hardware input lines connected to the 74HC151 digital multiplexer of Fig 11.5. Bits 4 and 5 of *ay0* contain the multiplexer inputs D4 and D5, which are the A and B outputs of the rotary encoder. The previously measured values for these lines are stored in a data memory location *dm(knob_st)*. By comparing the old and the new measurements, it is possible to deduce the knob movement, if any (See sidebar “Using a Table Lookup to Determine Knob Motion”). The implied movement is stored in a 16-member lookup table. This is certainly not the only way to deduce the knob movement, but it has the appeal of being easy to understand. In general, solutions that use a little more memory, but are easy to understand, have much appeal! The entry point to the lookup table is constructed from the old and new knob states by shifting the old state left to bits 2 and 3 and putting the new state in bits 0 and 1. This creates a 4-bit binary number that ranges in value from 0 to 15. All combinations of old and new state are included. The lookup table returns a value of -1, 0 or +1, as shown in Box 1.

Box 1 - DSP routine to determine knob rotation using a lookup table. The output in *ax0* is -1, 0, or 1 for counter-clockwise movement, no movement or clockwise movement.

```

knob:
    ay0 = 4; call inbit;           { LSB of knob state, in ax0 }
    mr1 = 0;                      { In case bit 3 of ax0 = 0 }
    ar = tstbit 3 of ax0;
    if eq jump kn1;
    mr1 = 1;                      { Find out }
    kn1: ay0 = 5; call inbit;     { Yes, it is = 0 }
    ar = tstbit 3 of ax0;
    if eq jump kn2;
    ar = setbit 1 of mr1;
    mr1 = ar;                     { The other case, bit 3 of ax0=1 }

    kn2:                         { Similar stuff for next to LSB }
    ar = dm(knob_st);
    sr = lshift ar by 2 (hi);
    ay0 = sr1;                   { Here with new state in mr1 }
    ar = mr1 or ay0;             { Knob state at last measurement }
    dm(knob_st) = mr1;           { Move left 2 bits }
    ay0 = ^encoder;              { 4 bit state }
    ar = ar+ay0;                 { Current state for next time }
    i4 = ar; m4 = 0; i4 = 0;      { The lookup table address }
    ay0 = pm(i4, m4);            { Get location in the table }
    none=pass ay0;               { The i4 index register gives the }
    rts;                          { easy way to get a table entry }
                                { Set flags, based on table entry }
                                { With -1, 0, or +1 in ay0 }
```

Box 2 - Lookup table for determining knob rotation

```

.var/pm encoder[16];          { Rel Adr=Last state*4+New state }
.init encoder:
    0, H#FFFF00, H#000100, 0,
    H#000100, 0, 0, H#FFFF00,
    H#FFFF00, 0, 0, H#000100,
    0, H#000100, H#FFFF00, 0;
```

Box 3 - Program to modify a program variable, *amult*, using the routine *knob*.

```

call knob;                    { See if knob has moved (in ay0) }
    ar=dm(amult);             { Alter by either 0, -1 or +1 }
    ar=ar+ay0;                 { We add, but ay0 may be + or - 1 }
    dm(amult)=ar;              { For next time & use by others}
```

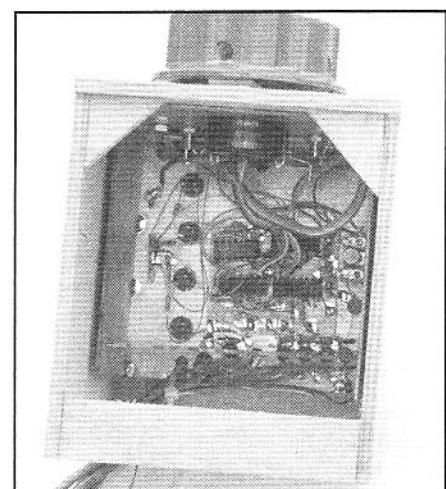
The lookup table is entered into the program as part of program memory as shown in the snippet in **Box 2**. The encoder table is stored as 24-bit data in *pm*, but used as 16-bit data in the DSP. The 00s on the end of the hex values are 8 bits, set to 0, that are never used, but are very necessary to make the bits line up when read as 16 bit values.

It is now possible to alter a value, such as the amplitude multiplier for a signal by calling the *knob* routine. As an illustration, we can modify a memory “gain” value called *amult*, as shown in **Box 3**.

More elaborate programming would allow different changes to be made depending on the knob rotation. This could be used for operations such as changing a filter or a frequency band.

LCD Panel

The *liquid-crystal display* (LCD) is convenient for displaying data from our DSP device. These displays range from the



Inside the knob box is a second box for the digital electronics. Pigtail wires run to the EZ-KIT Lite. For this box, a plug was placed on the pigtail wires to allow the same EZ-KIT Lite to be used for other projects. Any type of plug would be suitable.

simple character display to a large matrix with colors. We will only deal with the least complex of these, but the principles required to extend the complexity will be the same. The display shown here has 16 characters, arranged in a single row. Any of the alphanumeric characters and a variety of symbols can be displayed. The particular display used here is the Optrex DMC-16117A, but a variety of products are available from Optrex and other manufacturers. The programming of many of these displays is similar to that shown here. Check the manufacturer's data sheets for

the particular panel for details.

Programming the LCD panel through the serial-hardware lines is straightforward, but will appear to be somewhat laborious. The panel requires a sequence of commands be sent to initialize the controller. Once this is done, the individual characters of the display can be set by two byte commands. The emphasis here will be on the general nature of using the DSP as a controller, rather than on the specific procedures for this display. The details of this example are included with the programs for the "Knob Box," along with an

application using the box, the two sine wave plus noise generator. Both of these projects are shown later in this chapter.

When a character is sent to the LCD, it is displayed at the left edge, and all existing data on the display are pushed a character to the right. If one wants to write any new character, it is necessary to write all 16 positions in sequential order. For an example, we will display a 16-bit number in decimal form. This will include a leading negative sign if appropriate, or a leading blank if the number is zero or positive. These numbers, in decimal form, can range from -32768 to 32767. Including the minus sign, up to six characters are needed. To simplify the display arrangement, we will always leave room for six characters. We could write a long program routine to convert the number into numeric characters and to load these into the LCD display. Doing this can make a program difficult to follow and prevents reuse of any of the program pieces for other purposes. Writing the program as a collection of subroutines minimizes these problems.

We will now look at some of the details of these five subroutines. For selected portions of the routines, the detailed program instructions are shown. The fully commented source programs are included on the *Experimental Methods in RF Design CD* as part of the program C11KNOB.DSP.



A complete QRP rig for 2-meters, the DSP-10, is built around a minimal amount of hardware and the software running in the laptop PC. Along with the RF hardware in the die-cast box is an Analog Devices EZ-KIT Lite that serves as the last IF and audio portions of the transceiver. See page 11.27 for more information.

Using A Table Lookup To Determine Knob Motion

The table that is stored at the program memory table "encoder" is reconstructed here with the table address offset in binary and the table entries as decimal numbers:

4-Bit Address Offset	Entry
0000	0
0001	-1
0010	1
0011	0
0100	1
0101	0
0110	0
0111	-1
1000	-1
1001	0
1010	0
1011	1
1100	0
1101	1
1110	-1
1111	0

The address offset is shown as a binary number, corresponding to decimal equivalent numbers of 0 to 15. The binary values are the encoder-output logic levels for the last measurement followed by those for the current measurement. All 16 possible combinations are in the table. Relating these to the knob encoder, the binary

numbers are B'A'BA where the primed values refer to the last measurements and B and A are the two logic outputs from the encoder.

Some of the address offsets, such as 0101 or 1111, have the same old and new values and correspond to no motion of the knob. All four of this type can be found in the table to have an entry value of 0 indicating "no change."

Next are address offsets such as 0001. Here the B output has remained logic-level 0, but the A output has changed from 0 to 1. Referring back to the encoder logic of Fig 11.1 it can be seen that only if the knob has counter-clockwise motion is this possible. This results in an entry of -1. In a similar fashion, an offset of 0010 can only occur for clockwise rotation and an entry value of 1 results. If the knob is controlling a value, such as frequency, the new value can result from adding the table entry to the old frequency.

Note that there are four address offsets, such as 0011 or 1001 that should never occur. These correspond to both A and B outputs of the encoder changing at the same time. Fig 11.1 would suggest that this cannot occur. However, if the knob is rotated so fast that a state is skipped over, the 0011 combination may be encountered. This combination tells us that the encoder has changed by two positions, but there is no clue as to the direction. For this reason, the table entry must be zero, meaning that no change will be made.

Converting a Binary Number to Individual ASCII Digits

Fig 11.6 illustrates the programming of the LCD to display a 16-bit signed integer. The subroutine *n2bcd* converts the 16 bit number into six ASCII characters* that are left in a six position array in data memory. Each character is broken into four-bit halves, called nibbles, ready to be sent to the display by the subroutine *outch*. The routine *lcd4* supports *outch* by moving four bits into the shift register using multiple calls of the subroutine *loadl6*. This subroutine handles the pulsing of hardware lines to move data into the shift register. Completing the needed subroutines is *delay*, slowing the DSP process to ensure that the waveforms going to the shift registers have sufficient time to be correctly formed.

Changing the 16-bit number to 6 ASCII

*Most computer users are familiar with the ASCII character code as the language of text files or serial ports, where 128 different symbols are encoded into 7-bit binary numbers. The ARRL Handbook includes the details.

characters was seen to be the function of the subroutine *n2bcd*. This is done by considering each character position in order. If the number is negative, the first position is loaded with an ASCII minus sign. Otherwise it is loaded with a space or “blank” character. The number is then negated if it was negative.

The numeric value to be placed in each character position is determined by repeated subtractions. For instance, for the digit following the sign, we subtract 10,000 (decimal) from it. If this produces a negative result the number must be less than 10,000 and we will put a ‘0’ character in the second table position and move to the 1000s digit. Otherwise we put a one in the second table position and repeat the 10,000 subtraction. This continues through ‘3’, which is the largest value possible for the 10,000s digit, at which point the subtraction must have a negative result. **Fig 11.7** is a flow chart that illustrates this process for the 10,000 digit, and the program fragment in **Box 4** shows these same steps in assembly language.

The second instruction loads the *ay1* register with the ASCII value for the character zero, which is 30 hex or 48 decimal.

This is simpler than counting the number of subtractions and then adding 30 hex to it. Since all of the characters from ‘0’ to ‘9’ are in sequence in ASCII, the results are the same.

The subroutine repeats the same series of subtractions for the 1000s digit, except that here the number of subtractions possible may be as high as nine. This continues through the unit digit, after which all of the six character positions will hold the proper ASCII character. When we humans write a two-digit number in a six-digit space, we leave blanks in the four leading zero spots. These could be converted, but we will keep things simple by leaving these in place since it is not wrong.

This routine demonstrates the complexity occurring when converting a number built on powers of two to one built on powers of 10. For each power of 10, like 10000, 1000, 100,..., subtraction must be used to successively remove the powers of 10. The routine could be shortened by building it out of loops, but generally with the ADSP-2181 program memory is not in short supply. In-line routines, such as used here are often easier to debug and can execute faster than their looped equivalents.

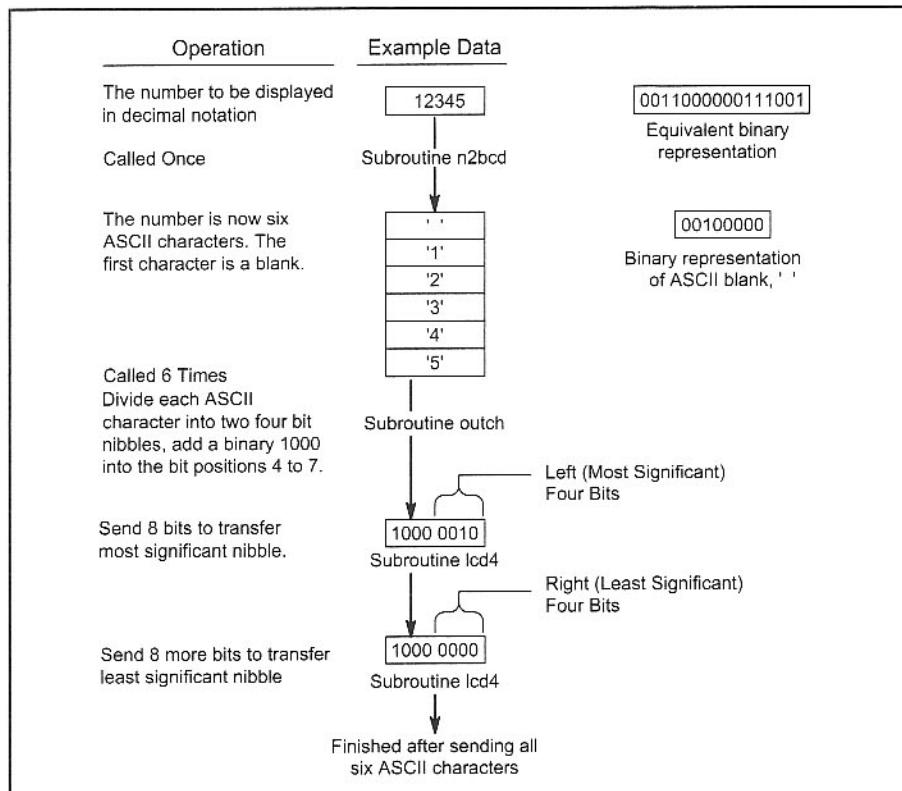


Fig 11.6—Data structures used in converting a 16-bit signed number into a form for sending to the LCD display. Three subroutines are used to break the number into characters, prepare a character for transmission and to send a four-bit nibble as required by the LCD display.

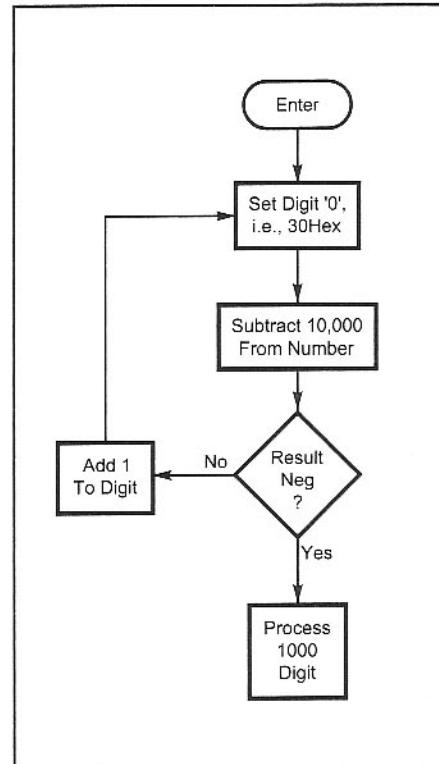


Fig 11.7—Flow diagram of a portion of the *n2bcd* subroutine, showing the extraction of the 10,000's digit. The digit is converted to ASCII by adding the value 30 hex.

Box 4 - DSP program to determine the ASCII value corresponding to the 10,000's digit.

```

{ The number to be converted to BCD is in data memory dm(temp1) }
ay0 = 10000;           { Find the 10,000s digit }
ay1 = h#30;            { '0' to count the subtractions }
n2a: ar = dm(temp1);   { Test the current reduced number }
af = ar - ay0;
if It jump n2b;
ar = ar - ay0;
dm(temp1) = ar;
ar = ay1 + 1;
ay1 = ar;
jump n2a;
n2b: dm(digit + 1) = ay1;

```

{ Done for this digit }
 { Not done, reduce working number }
 { Increase current digit }
 { This is where it is kept }
 { Continue subtractions }
 { store the ASCII value in memory }

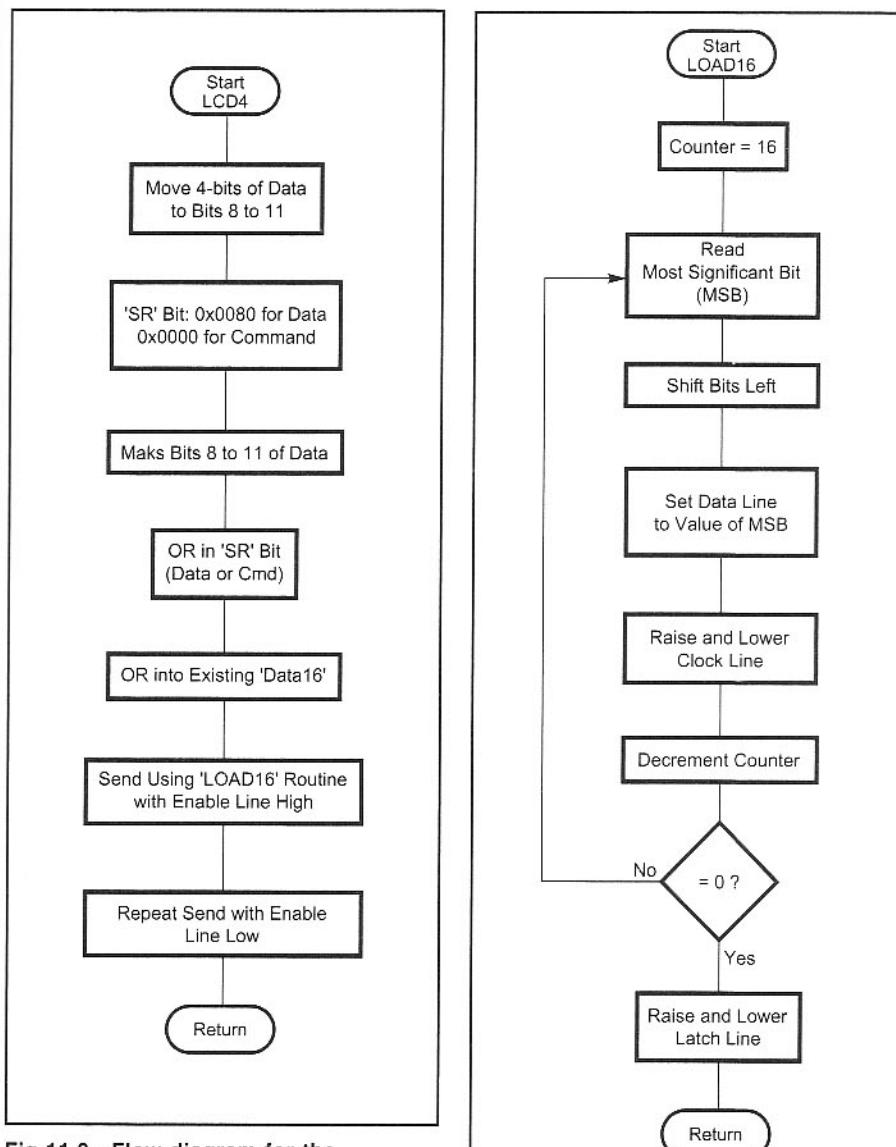


Fig 11.8—Flow diagram for the subroutine *lcd4* that transmits 4 bits of data or command to the LCD panel, while not changing the other outputs of the hardware shift register.

Fig 11.9—Flow diagram of the subroutine *load16*. This transfers 16 bits of data the hardware shift registers.

We now have six characters in a memory array ready to be sent to the display. This is transmitted to the LCD as nibbles, each containing four-bits of the character. To indicate that this information is display data, a binary one is placed in the left-hand position of the eight. All of this is handled by a subroutine, called *out_ch*.

Going back to the schematic of the display in Fig 11.5, of the 16 bits of shift-register output lines, only seven go to the LCD. So, we need to be careful that sending data to the LCD does not change the other outputs. This is accomplished by using a logical OR instruction with a copy of all the outputs kept in data memory as *dm(data16)*. Other data manipulation steps are needed to be consistent with the requirements of the LCD hardware. The subroutine *lcd4* performs these operations for both nibbles. **Fig 11.8** shows the flow of this subroutine.

The only missing operation now is a method to load the 74HC595 shift registers with serial data (see the sidebar on page 11.2, “Three-Wire Serial Interfaces”). This is accomplished by use of a subroutine *load16*, outlined in **Fig 11.9**. One advantage of this modular subroutine structure is the ability to use this same routine for any operation that requires altering the outputs of the shift registers. The figure and the commented listing on the *Experimental Methods in Radio Frequency Design* CD-ROM can be examined to see the detailed operation. However, one recurring element is to send a pulse on a hardware line. In assembly language sending a positive going pulse typically looks like **Box 5**.

The routine “delay3” does nothing for 3 microseconds. This allows plenty of time for the feed-through filters coming from the PF leads to achieve their full rise. The delay routine could have been written as a loop, such as

```

delay3:
  cntr=97;
  do dly3a until ce;
  dly3a:      nop;
  rts;

```

but this has a drawback. There are only four places on the counter stack. Every time a new value is loaded into the “cntr” register, the current value is placed on the counter stack. There is only room for four values on this stack and a fifth attempt will result in counter data being lost. To leave room for other routines, the delay routine uses extra space in program memory to save space on the counter stack. It looks like:

Box 5 - DSP assembly language to create a 3 microsecond pulse on the hardware line, PF1.

```
{ Latch the data with a pulse on bit 1 }
ax0 = dm(PFDATA);           { Get the current PF data }
ar = setbit 1 of ax0;        { Make bit 1 a 1, it was 0 }
dm(PFDATA) = ar;            { Send to hardware, via dm }
call delay3;                { Pulse is 1, Wait 3 microseconds }
ax0 = dm(PFDATA);           { Get the PF data again}
ar = clrbit 1 of ax0;        { Bring hardware line to 0
dm(PFDATA) = ar;            { Again send to hardware, via dm }
```

delay3:

```
nop; nop; nop; nop; nop;
nop; nop; nop; nop; nop;
{ ... And 8 more lines of
NOPs here ... }

nop; nop; nop; nop; nop;
nop; nop; nop; nop; nop;
rts;
```

Either routine performs no function during its execution. If an interrupt occurs during the delay routine, it will only increase the delay time, which will not be harmful.

Returning to the *load16* routine, the memory location `dm(PFDATA)` is one of a number of dedicated memory locations that are treated as registers.² The lower 8 bits of PFDATA correspond to the 8 pins

of *Programmable Flag* called *PF0* to *PF7* in hardware terms. These pins can be programmed to be either inputs or outputs. If they are outputs, as we need for the shift register data, clock and strobe, writing to the location `dm(PFDATA)` will change the pins to the new value. Reading from `dm(PFDATA)` tells the program the current setting of all pins while writing will set the levels.

The *load16* routine proceeds through all 16 bits by finding from `dm(data16)` the desired bit value, putting this onto bit 2, and then moving the clock line, bit 0, from 0 to 1 and back. Delays are inserted at each point to make sure that the data arrives before the clock pulse and that all pulses are long enough to reach their full extreme values. Finally the strobe line, bit 1, is moved from 0 to 1 and back, latching the 74HC595 shift-register data by moving it to the output pins.

11.3 AN AUDIO GENERATOR TEST BOX

A device using the capabilities of the Knob Box is the Audio Generator. This provides an output signal from the EZ-Kit consisting of two sine waves and a random noise. This is useful for transmitter testing using either one or two tones. The noise signal can be useful for transmitter testing or for simulating the reception of signals in noise. Each sine wave can have its frequency set to any value from 1 Hz to 20 kHz, and the RMS amplitude can be varied in 0.1-mV (100-microvolt) steps. The noise is always Gaussian and flat with frequency. The noise RMS amplitude can also be varied in 0.1-mV steps.

This audio generator also illustrates the building block assemblage that we are using. The sine wave and noise generators come from Chapter 10 routines, and the knob and LCD hardware and software are those that have just been discussed. In the following section, we will tie these together into a handy test box.

All signals from the generator have great relative-amplitude accuracy. The absolute accuracy of the D/A converter output is only about 10%. This is a scaling error only and can be removed by calibration of the particular converter. Even without an absolute calibration, the signal-to-noise ratio or the ratio of two signal voltages can be set very accurately, typically better than 0.1 dB.

The distortion in the generator output is very low at about 0.025 per cent. Distortion is a much more important parameter for this type of application.

The four button switches on the knob box control the various functions. Button 1 scrolls through display controlling which of the three waveforms is being controlled:

Sine wave 1

Sine wave 2

Noise

Button 2 selects the knob function:

Amplitude

Frequency

Button 3 is left unused to allow for future additions, and Button 4 toggles all outputs between on and off. The red LED indicates the on/off state.

The display has 16 characters, adequate to indicate the generator state. For instance, if Button 1 selects the first sine-wave generator, the display would be

"1 fffffHz vvv.vmV"

where the first 1 means that the data applies to generator 1, fffff is the frequency in Hz and vvv.v is the RMS output level in millivolts.

Fig 11.10 is a block diagram of the soft-

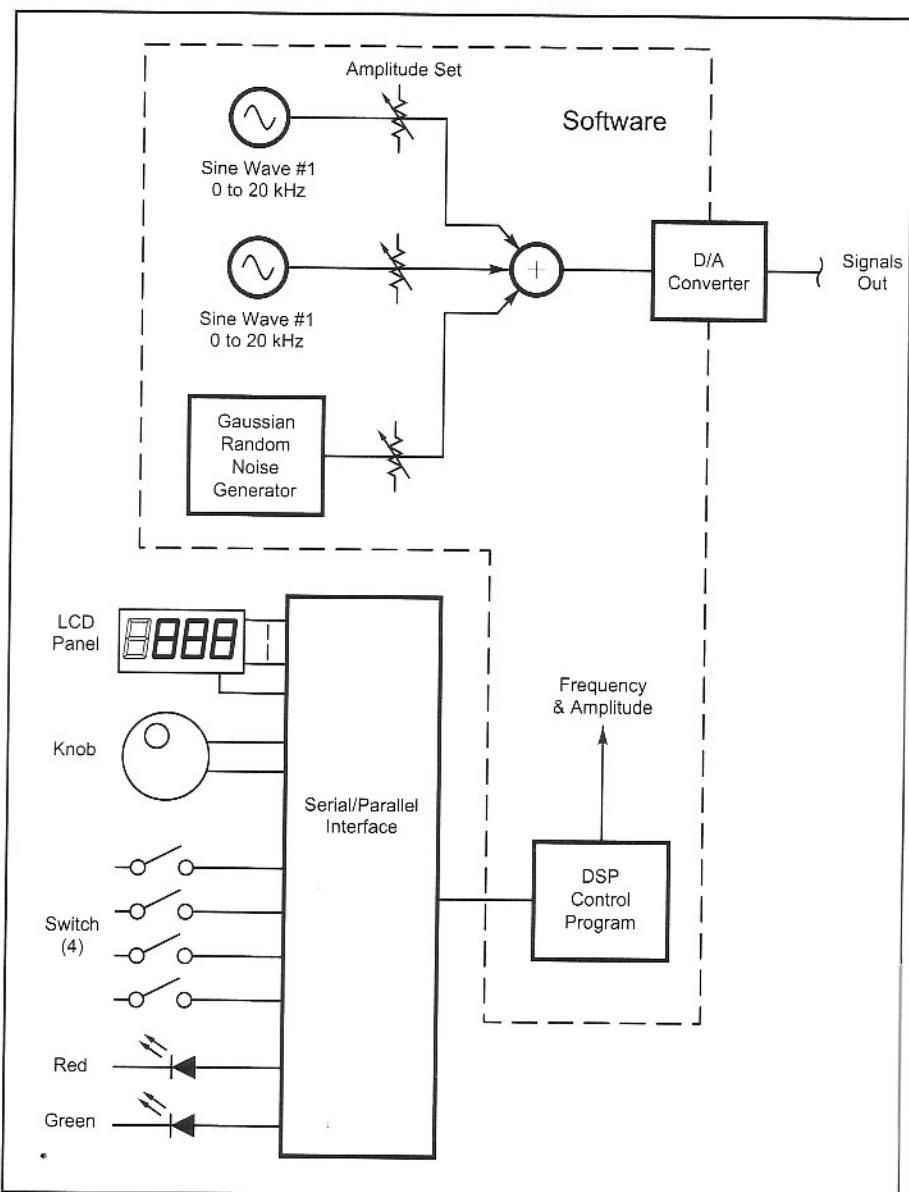


Fig 11.10—Overall block diagram of the tone and noise generator. The knob controls both the frequency of the sine-wave generators and the amplitudes of the three signals. The function of the knob is determined by the push buttons. The 16-character display is also driven by the interface circuitry controlled by the DSP software.

Box 6 - DSP routine to set phase increment for sine-wave generator.

```
{
  Frequency in Hz in the ar register. To convert to a phase increment
  we need to multiply by 65536/48000. But in the 1.15 arithmetic, the
  biggest value is 1.0. So, we multiply by FR2PH=0.5*65536/48000=0.6827 and
  then shift left 1 bit, the same as multiplying by 2. }

  .const    FR2PH=0X5762; { Hex for 0.6827 in 1.15 format }
  { And the code in the main body of the program: }
  my0=FR2PH;
  mr=ar*my0 (ss);           { The fractional multiply, and }
  sr=ashift mr1 by 1 (hi); { the multiply by 2, which is}
  sr=sr or lshift mr0 by 1 (lo); { in two parts to get LS bit }
```

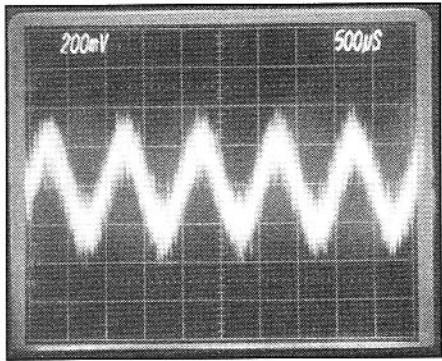


Fig 11.11—Oscilloscope trace of the Audio Generator output. One sine wave is set to 150-mV RMS and the other to zero. The noise level is 50-mV RMS making the S/N 9.5 dB ($20 \log(3)$). The sine-wave frequency is 1000 Hz.

ware and hardware functions involved. The individual functions, such as sine-wave generation, knob control and LCD display have all been covered earlier and will not be repeated here. The details of the integration of these program components

can be seen in the full listing that is available in the program *c11tbox.dsp* on the CD-ROM that accompanies this book. The more interesting areas are the details that must be handled to make the signal generator operate properly.

For instance, the display for frequency is in integer Hz, from 1 to 20,000. The sine-wave generator has a resolution of about 0.73 Hz. The knob could be used to change frequency in either in steps of 1 Hz or 0.73 Hz. Either way, a conversion must be made to the other resolution step. The method used was to always change the desired frequency by 1 Hz, and then to convert this to a phase increment corresponding to the 0.73 Hz step. This results in the knob always producing a visible frequency change on the display, but about 1/3 of the possible generator frequencies are not used. The conversion from a frequency in the AR register to a phase increment in the SR1 register is as follows in **Box 6**.

Figs 11.11 and 11.12 are example waveform outputs from the Audio Generator. Output levels and frequencies are shown in the captions.

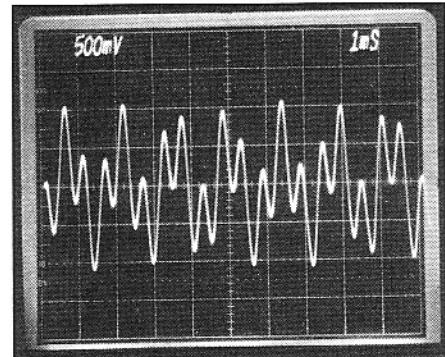


Fig 11.12—Oscilloscope trace of the Audio Generator output. The sine-waves are of equal amplitude and the frequencies are 700 and 1900 Hz. The noise is set to zero.

If the D/A converter is operated below its overload point the distortion, including intermodulation, can be expected to be very small. The principle drawback to this approach is the limited frequency range. For the hardware used here it is not practical to operate much above 20 kHz.

11.4 AN 18-MHZ TRANSCEIVER

This CW/SSB transceiver operates in the 17-meter amateur band from 18.068 to 18.168 MHz. Direct conversion, as discussed in Chapters 8 and 9, is used for both the receiver and transmitter. All RF functions are built with conventional hardware, but the audio functions are DSP based. In addition, control functions were delegated to the DSP, to the extent possible.

The general arrangement of the transceiver is shown in the block diagram, **Fig 11.13**. The receiver begins with a single tuned circuit and an RF amplifier. The considerations for signal-to-noise ratio, dynamic range and LO radiation were discussed in Chapter 8 and apply here. In



The 18-MHz Transceiver.

order to use the same filters and mixers on both receive and transmit, there is a PIN diode switch following the RF amplifier. For reception, this switch also provides a simple method for manually controlling the RF gain, as the PIN diode can also be used as an adjustable resistor.

Two mixers are connected to the RF circuits through a power divider. A 90-degree power divider supplies the conversion oscillator for the two mixers. In reception, this creates the 'In-phase' and 'Quadrature' or I and Q signals at audio. After low-pass filtering, an A/D converter that is part of the DSP board, digitizes the two signals.

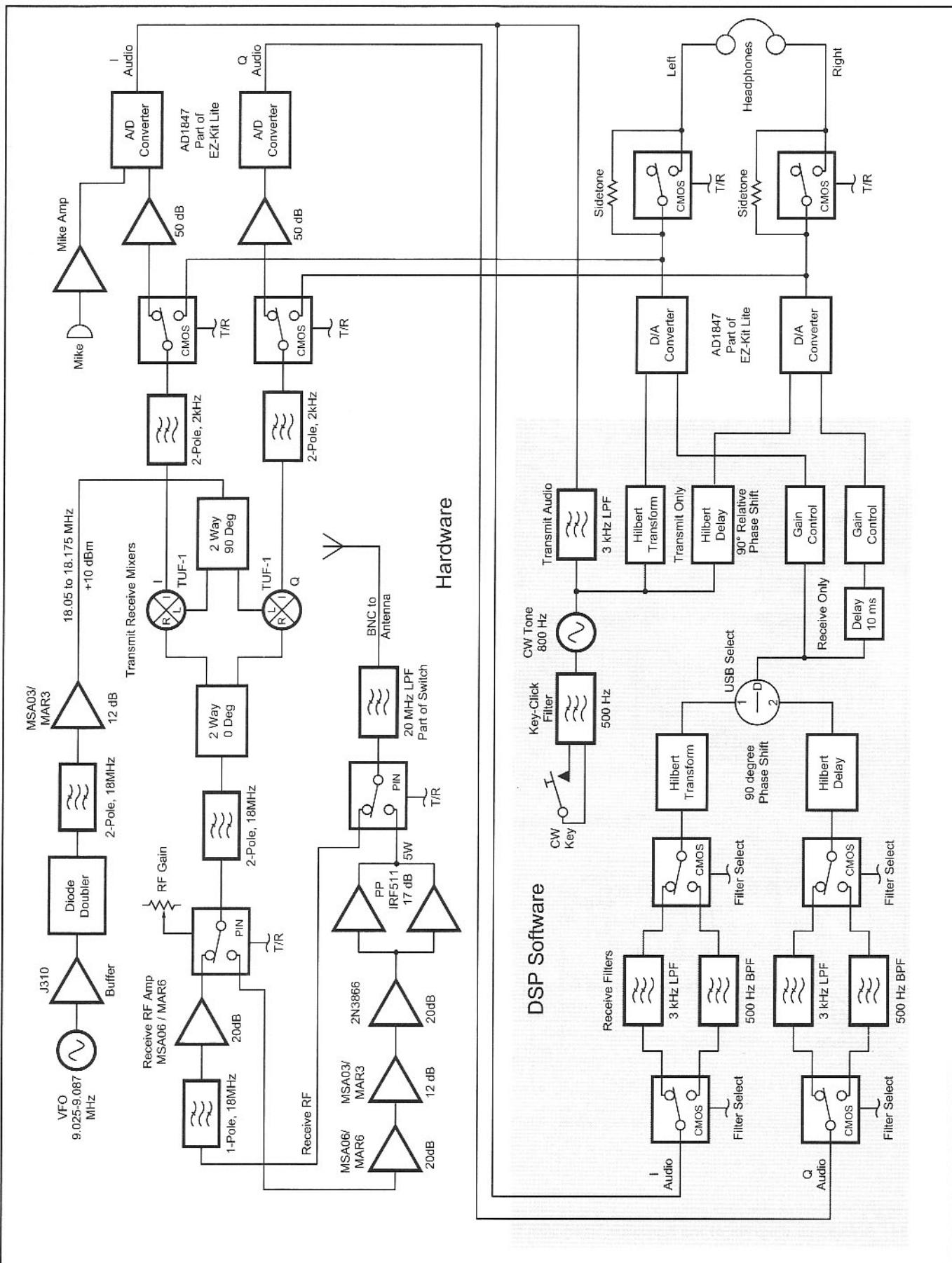


Fig 11.13—Block diagram of the 18-MHz transceiver showing the division of the functions between conventional hardware and DSP software.

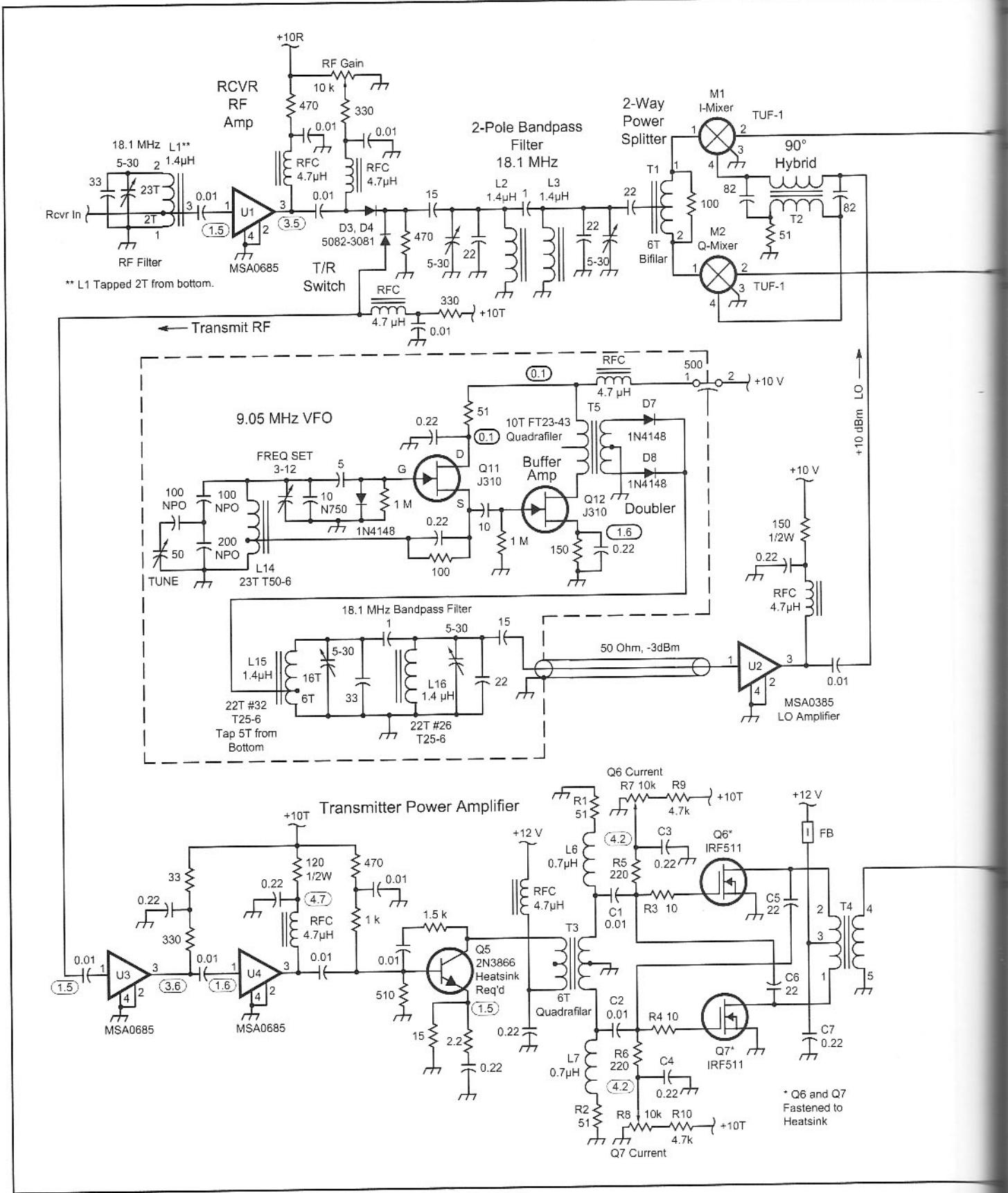
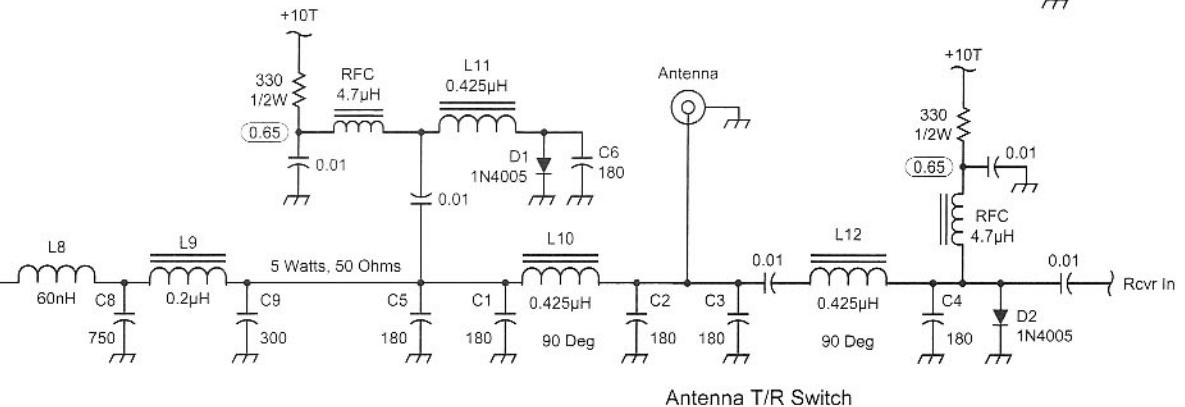
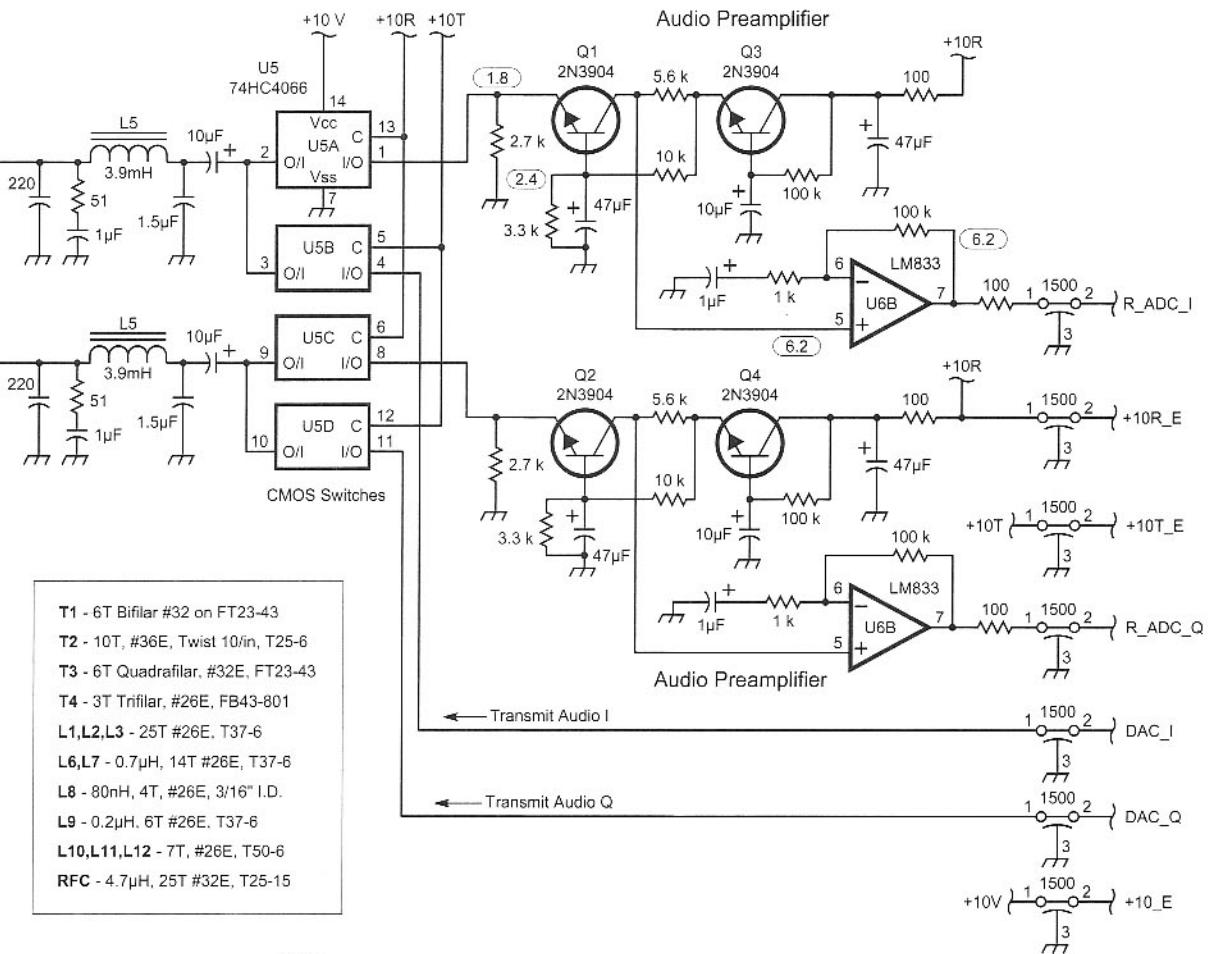


Fig 11.14—Schematic diagram of the hardware used with the 18-MHz transceiver (continued on next two pages).



Note: The circuitry on these two pages (11.14 and 11.15) should be contained in a shielded enclosure. The 1500 pF feedthrough capacitors filter the leads coming into the enclosure.

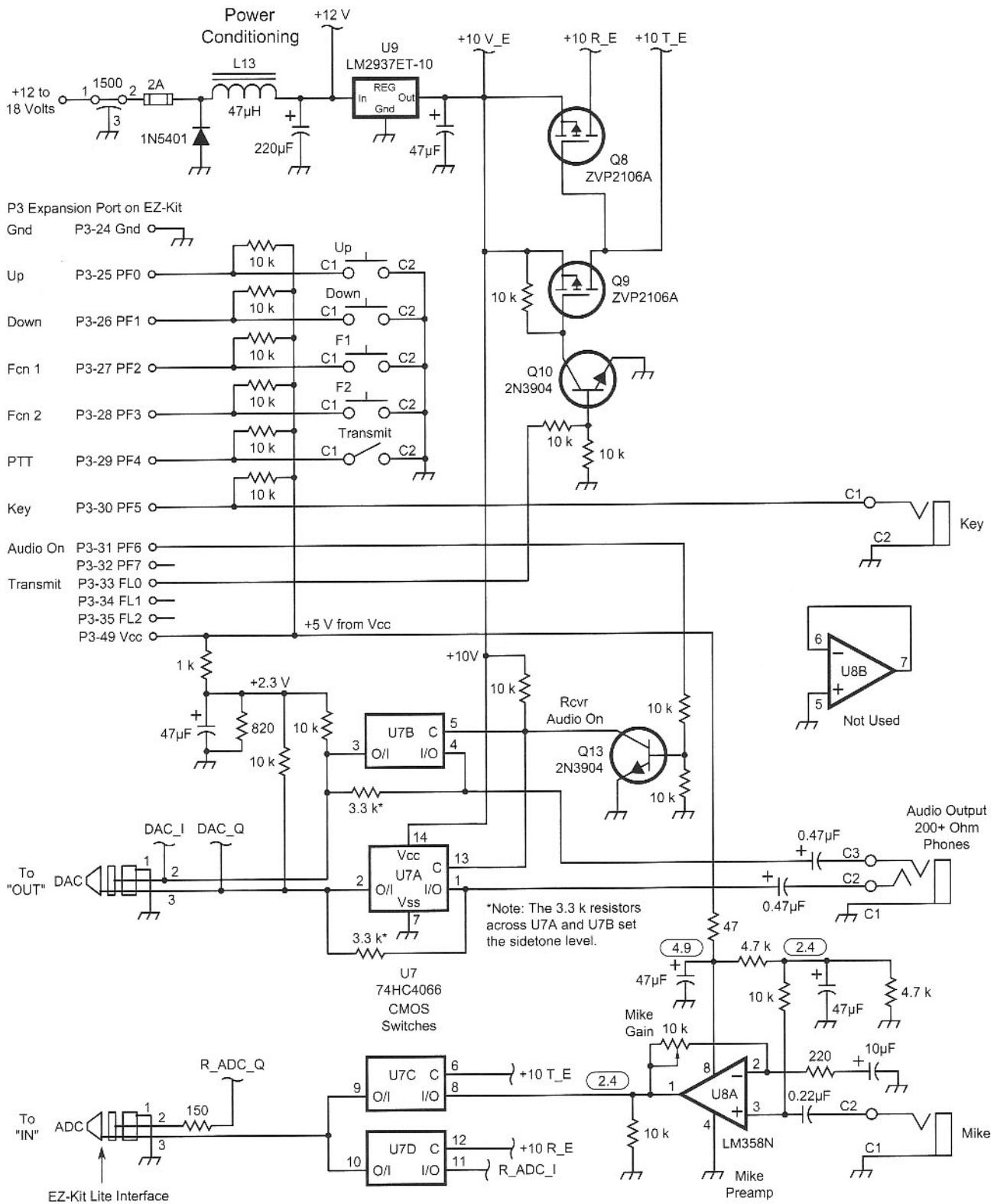


Fig 11.14 continued.

The I and Q audio signals are put through individual audio filters in the DSP. Two filter bandwidths are provided, a 3-kHz low pass filter and a 500-Hz filter, suitable only for CW. Due to the DSP implementation, the I and Q filters are identical in their response. In order to have single-sideband reception, a broadband 90-degree phase difference must be applied to the two audio signals. This is done with a DSP filtering technique called the Hilbert transform. The received upper-sideband signal can then be formed with a simple subtraction of the audio signals. Dividing the audio signal into left and right channels and applying a delay to one of these provide binaural reception. A D/A converter then converts the audio back to analog form, ready to go to headphones.

Transmission reverses most of the signal paths from those of reception. For SSB, a microphone preamp provides some voltage gain ahead of the A/D converter. Low-pass DSP audio filtering restricts the transmitted bandwidth, remembering that we have no I-F filtering to do this. Hilbert transforms produce the 90-degree phase difference needed for the suppression of the lower sideband. The transmitter signal is converted to analog form in the same D/A converter that was used in the audio output of the receiver. After going back through the I-Q mixers, the RF signal is quite low in amplitude. Four stages of amplification raise this to about 5-W SSB PEP or CW amplitude.

For CW transmission, the on-off key signal goes through a 500-Hz LPF to restrict key-clicks. The filtered signal amplitude modulates a pair of 800-Hz tones. These tones are generated in the DSP to differ in phase by 90 degrees, again ready to be converted to analog signals for the I-Q mixers. We again used a method that works well because of the accuracy of DSP, but is considered poor practice in hardware form.

The VFO is quite conventional. A frequency doubler increases the isolation between the 9-MHz VFO and the 18-MHz RF signals.

RF Hardware Details

To simplify the hardware, a number of silicon MMICs are used as amplifiers. As shown in the RF schematic, Fig 11.14, the receiver RF amplifier, U1, is a broadband device with a gain of about 20 dB. This is an Agilent (HP) MSA0685, or equivalently, the Mini-Circuits MAR-6. These devices have input and output impedances that are close to $50\ \Omega$, broadband gain and reasonable output powers and inter-

modulation levels. These devices are available in a number of different gain and power levels. They require external blocking capacitors, dc power feed RFCs and current limiting resistors. Probably the biggest drawback to the use of these devices is their power consumption. Their efficiency is about half of that achievable with a well designed transistor amplifier, due mainly to the power lost in the current limiting resistor.

Preceding the RF amplifier is a single tuned circuit built around the inductor L1. This restricts the signals that are seen by U1. It is particularly important to reduce the level of inputs at half frequency, or about 9 MHz. Otherwise, these signals are prone to being doubled in the amplifier, making the 17-meter band come to life at times it is not! Two more tuned circuits, built around L2 and L3 provide most of the RF selectivity. This filter uses a configuration of S. B. Cohn^{3,4} using capacitive coupling on the ends to match impedance levels. The 15 pF on the input matches to $50\ \Omega$ while the 22 pF on the output side matches to $25\ \Omega$, suitable for connecting to the two $50\ \Omega$ mixers.

Between the RF amplifier and the filter is a PIN diode switch controlled by the transmit receive (T/R) voltages. For transmit, this connects the filter to the transmit RF amplifier. In the receive case, it serves this same switching function but, also the current through the diode can be varied by the RF gain control. This allows about 40 dB of control range, and is of considerable value when working strong local stations.

A two-way isolated power splitter, T1, applies the received signal to the two mixers. Usually these splitters include a transformer to change the impedance level from 50 to $25\ \Omega$. As was discussed above, this impedance transformation is part of the RF filter.

The mixers are double-balanced TUF-1 types from Mini-Circuits. These provide excellent isolation between the LO and RF

ports; this is the transmit carrier rejection. The LO drive differs in phase by about 90 degrees for the two mixers providing one of the necessary elements for the "phasing method" of SSB detection and generation.

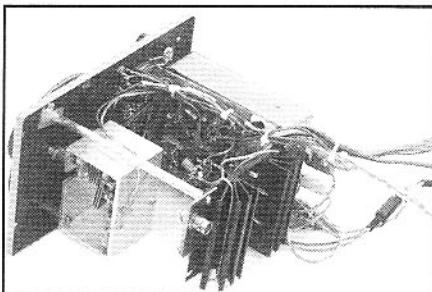
The RF phase-shift network (see the discussion in Chapter 9) consisting of a tightly coupled inductor, T2, the two 82-pF capacitors and the $51\ \Omega$ terminating resistor. This network has rather sophisticated operation, considering its simplicity. The LO signal is divided into two equal mixer drive signals with the 90-degree phase difference. In addition, there is isolation between the two outputs that go to the mixers. Ideally, no power is transferred to the $51\ \Omega$ resistor. It serves to provide isolation when one a signal is applied at just one of the mixers.

The drawback of this phase-shift network is that it only works over a narrow band of frequencies. The power division is equal only at the center frequency, and the isolation deteriorates out-of-band as well. This causes the harmonic energy generated in the mixer diodes, due to the LO drive, to redistribute itself in strange ways, as can be observed on an oscilloscope. However, the important equal power and 90-degree relationship is preserved at the fundamental frequency. Because of this, the circuit generates outputs of the correct amplitudes and phase.

AF Circuitry

The receive path signals are generally too weak for the A/D converter without amplification. Full scale for the A/D converter is about ± 2 V or a 4 V swing. About 14 bits are above the A/D noise level within an audio bandwidth. This sets the minimum input-signal requirements at about $4/2^{14}=4/16384=244$ microvolts. Bringing a 0.1-microvolt signal up to this level requires about 67 dB of audio gain. This is provided by grounded-base transistor Q1 (or Q2) and a low-noise op-amp, U6A (or U6B). Further details of this circuit can be found in Chapter 8.

The receive audio path to the A/D converter has switches, U7C and U7D, allowing the microphone audio to be connected to the A/D converter during transmit. These are 74HC4066 CMOS types, which show an "On" resistance of $35\ \Omega$, typically. For reception this can have an effect on the noise figure. One simple method of minimizing this affect is to parallel two or more switches by mechanically stacking them and soldering the pins together. Alternatively, four MOSFET devices, such as the 2N7000, could be substituted for the CMOS switches.



General inside view of the 18-MHz transceiver.

VFO

FET Q11 is a conventional Hartley VFO shown in Fig 11.14, operating at half of the output frequency. The tuning capacitor was capacitively tapped down on the tuned circuit to make the tuning range just over 100 kHz. Q12 buffers the output of the VFO. Diodes D7 and D8 are a balanced doubler that is reasonably efficient at producing even harmonics and suppresses the fundamental frequency and odd harmonics. This reduces the filtering needs on the output of the doubler; the double-tuned circuit built around L15 and L16 produces a clean spectrum, as was illustrated in Chapter 5.

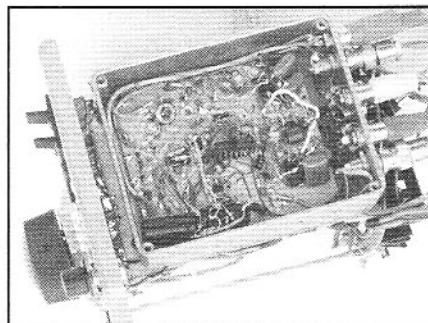
In the interest of good mechanical stability, the VFO was built in a surplus aluminum box with relatively thick walls. The coils were all fastened in place with dabs of silicone sealant. Multiple aluminum spacers hold the VFO to the steel front panel. Almost no microphonics can be sensed when the case is tapped with a hard object. This is often a problem with VFOs built for higher frequencies.

Considerable experimentation was done to make the VFO temperature stable. The procedure was straight from Hayward.⁵ After about 7 or 8 tries, a simple compensation consisting of a 10-pF N750 parallel capacitor was found to make the temperature drift of the 18-MHz frequency only 25-Hz per degree C. There is probably good fortune involved in getting the compensation that good, as an apparently identical 10 pF produced a drift of about 50-Hz per degree. Either way, it is worth the effort to do the experiments and compensate the VFO, since the uncompensated stability was measured at -470-Hz per degree C.

Power Amplifier

A single low cost IRF511 MOSFET was tried as an output amplifier. It produced about 3 W of power at 13.6 V. Higher supply voltages produced much more output, but battery operation was one of the goals for this rig. To produce a 5-W output, two of the MOSFETs were placed in the push-pull configuration shown in the schematic. Ferrite cores were used in the input and output transformers.

As is usually the case for these devices (see Chapter 2), HF stability required some extra components. The major culprit in degrading the stability is the 30-pF feedback capacity from the drain to the gate. Good stability and gain at 18 MHz could be achieved by applying some cross neutralization from the two 22-pF capacitors. It was found, however, that there was a tendency toward oscillation in the 2 to 4-MHz region. This is associated with the cut-off phase-shift of the input and output



18-MHz transceiver shielded box circuit detail showing extensive use of the "ugly" construction method.

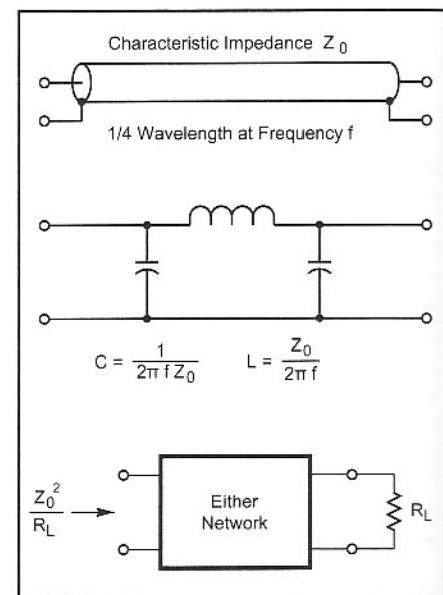


Fig 11.15—Schematics and design equations for impedance inverters built from transmission lines and lumped capacitors and inductors. At the single frequency, f , the two circuits have identical behavior.

transformers. Two steps were taken to keep this from being a problem. First, the amount of neutralization was limited to the 22-pF value instead of using the full 30-pF value. Second, a low-frequency input-loading network was added to each device, consisting of L6 and L7, along with the associated 51-Ω resistors. The resulting amplifier is measured to be unconditionally stable for all input and output impedances, throughout the HF spectrum.

A low-pass filter/matching network was placed on the amplifier output. L8 and L9 and the associated capacitors limit the harmonics and also step the 7-Ω output impedance up to 50 Ω. This network limits the frequencies for which this amplifier can be used. Other portions of the amplifier are useful from 1.8 to 30 MHz.

Antenna Switching

Low cost rectifier diodes (see Chapter 6) switch the antenna between the transmitter power amplifier output and the receiver input. A simpler, series-tuned approach, as was also used in Chapters 6 and 12, would probably have worked at this power level. However, this is an example of a solid-state RF switch that can be applied at quite high power levels. The use of impedance inverters for fast antenna switching has roots at least as far back as the early days of radar where it was implemented in waveguide.⁶ The following discussion shows how these concepts were applied to this transceiver.

Pi-networks, consisting of L10, L11 and L12 along with their associated 180-pF shunt capacitors, act as 90 degree phase shifters at 18 MHz. Just like their counterparts, the "quarter-wave transformer," these networks serve as impedance inverters. This means that if one end has a low impedance placed across it, the impedance seen looking into the other end will be high. The opposite is true as well; if a high impedance is placed across one end, the other end will show a very low impedance.

Fig 11.15 shows the design for this network. Both the capacitors and the inductor are chosen to have the same reactance at the center frequency. This reactance has the same role as the characteristic impedance of the quarter-wave transformer.

In the antenna T/R switch of Fig 11.14, the inverting network consisting of L12, C3 and C4 acts as low-pass filters during receive, with the signal passing without attenuation. In transmit, diode D2 is conducting and its low impedance shorts out the receiver input. The inverting network uses this low impedance to cause a very high impedance to appear across C3.

The same effect occurs at the transmitter output, due to diode D1 and the inverting network consisting of L11, C5 and C6. During transmit, when D1 is conducting, the impedance seen at the transmitter output, across C5, is very high. Here we also exploit the reverse effect. During receive D1 is not conducting and therefore presents a high impedance, primarily the diode capacity of a few pF. This is transformed through the inverting network to produce a low impedance at the transmitter output, disconnecting any effects of the MOSFET amplifier. The next inverting network, L10, C1 and C2 transform this back to a very high impedance at the antenna connection point.

A single value of capacity, 180 pF, was used for all the networks, for convenience. If they are available, the parallel 180-pF capacitors can be replaced with a single 360 pF.

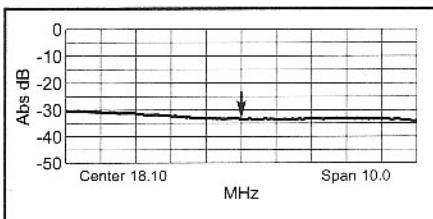


Fig 11.16—Measured isolation of the antenna T/R switch between the transmitter and the receiver.

The inverting networks are relatively non-critical. Any tuning that might be needed can come from squeezing or spreading the turns on the coils.

The Antenna T/R switch was tested as a component by breaking the leads going to the transmitter output and the receiver input. The 18-MHz insertion loss from the antenna connector was 0.33 dB to the transmitter (in transmit) and 0.25 dB to the receiver (in receive). Receiver isolation is a measure of the amount of power going from the transmitter to the receiver input, when the switch is in transmit. As can be seen in Fig 11.16 this was measured to be about 33 dB at 18 MHz. For a 5-W transmitter this keeps the power at the receiver input below 4 dBm, well below the maximum safe input level for the RF amplifier.

DSP Circuits

For this rig we have chosen to move much of the circuitry into DSP. This is an alternative to conventional analog circuits. In some cases we can improve upon the performance that could be expected from the analog equivalent, but in most cases it comes down to what is easiest. The DSP is again done with a demo board. In some

sense, the demo board is a component that is generally easier to install than the parts that it replaces.

One might argue that it takes more time to write the DSP software than building hardware. This is almost certainly true for the first time with a circuit block. However, seldom do we need to write software the “first time.” In many cases, we can borrow from previous work or find suitable beginnings in reference books. The material presented here falls in this category. However, this is not to discourage anyone from taking the code apart and trying their own ideas and algorithms. There can be great fascination with writing a program and seeing it produce useful results, such as a DX QSO!

The DSP program for the 18-MHz transceiver not only processes the audio signals for the transmitter and receiver, but controls the simple functions such as transmit and receive switching, reading the panel button switches and lighting the transmit LED. Instead of laboriously describing all of the DSP programs, the following will describe the most important elements of the program. Much of what will be left out is repetitious or is obvious, once one understands the basics of the program writing.

The full DSP program listing for transceiver is available on the book CD-ROM as *TR18.DSP*.

Reception

The basic reception scheme, shown in Fig 11.17, is the direct-conversion I-Q (phasing) method. The basic principles have been around for a long time and have been implemented in analog circuits, as was shown in Chapter 9, and DSP as was done by Rob Frohne, KL7NA.⁷ The logi-

cal juncture between the RF circuits and the DSP is at the outputs of the mixers. The first of the low-pass filtering is done in hardware. This limits the level of out-of-band signals levels that are seen by the A/D converter.

Almost all of the band-pass shaping is done in the DSP. Two identical filters are used, one in the I channel and another one in the Q channel. If the signal that we are receiving is of a single frequency, such as a CW signal, the I and Q channels will be a single-frequency audio signal. The frequency will be the difference between the 18.1-MHz LO and the incoming signal. Ideally the amplitudes will be identical and they will be 90 degrees out-of-phase. The actual phase difference will track that of the LOs applied to the mixers.

Applying a 90-degree phase-shift across the audio spectrum and either adding or subtracting the resulting two signals accomplishes SSB reception. The 90-degree shift will bring the two audio signals so that they are either in-phase, or 180 degrees out-of-phase. Addition, or subtraction, then makes the two signals either add to double amplitude, or to cancel to zero. The choice of sign determines whether upper or lower sideband reception is being used.

Regardless of how it is implemented this “phasing method” has a two standard problems. First, producing a constant amplitude, constant 90-degree phase shift over a wide band of frequencies is always an approximation. Second, the mixers, LOs and analog filters all introduce small phase and amplitude errors. Both of these factors, explored in some detail in Chapter 9, serve to limit the ability to eliminate the undesired sideband, referred to as opposite side-band rejection. A DSP

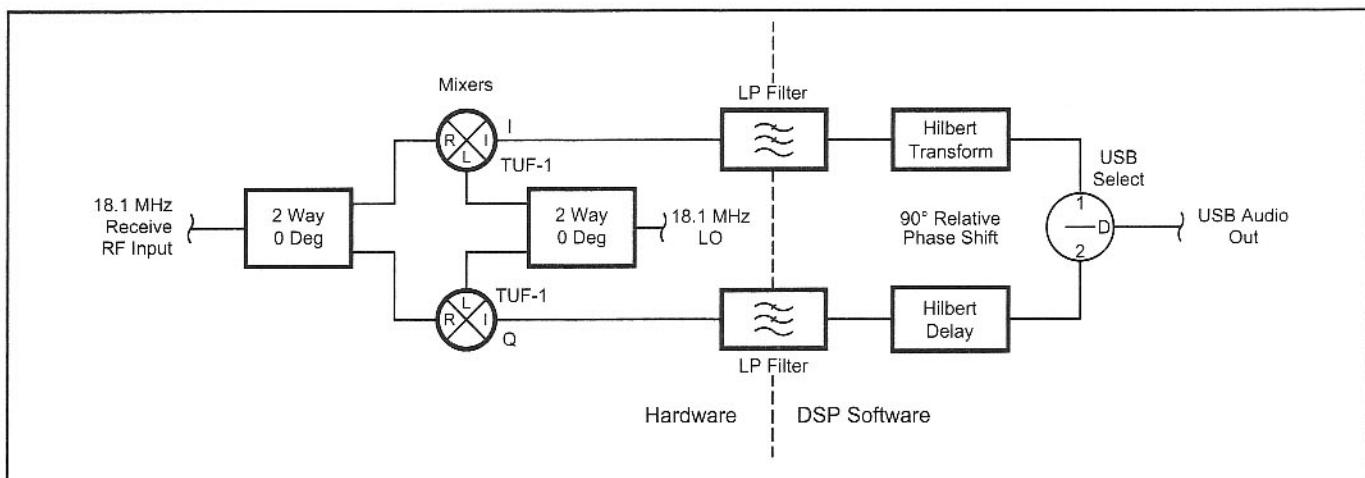


Fig 11.17—Simplified block diagram showing the phasing method of reception used in the 18-MHz transceiver. The circle at the right with a minus sign subtracts input signal 2 from input signal 1.

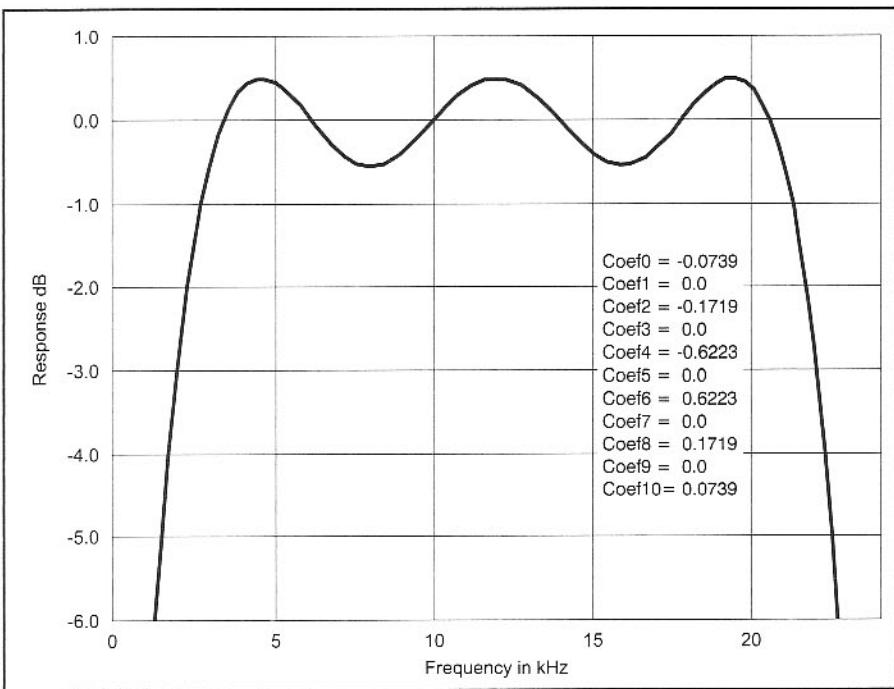


Fig 11.18—Coefficients and amplitude response for a very simple 11-tap Hilbert transform. This is shown to illustrate the method, as one would never use a transform with only 11 taps for SSB generation.

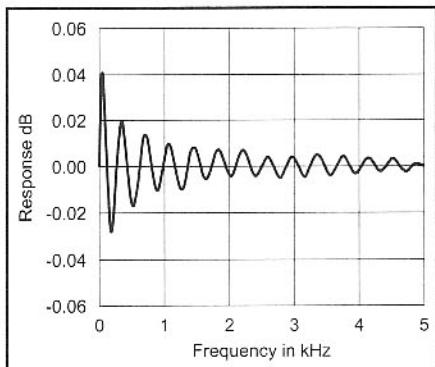


Fig 11.19—The amplitude response of a Hilbert transform using 247 taps and a sample rate of 48 kHz.

implementation of the phasing method does not inherently provide a higher level of unwanted-sideband rejection relative to analog methods. Rather, it should be looked at as an alternative implementation that is potentially easier to implement. This is particularly true if the DSP hardware is being used for other purposes anyway and the only addition is in the software area.

In Chapter 9, the reasons for needing a wideband audio 90-degree (relative) phase shift network were explored. An analog method was used in that chapter to achieve that response, typically using 6 op-amps and precision RC networks. In DSP implementations, the same function is accom-

plished by a “Hilbert transform.” The implementation of this transform has a structure identical to the FIR filter that was discussed earlier. The distinguishing characteristic is the particular choice of FIR coefficients. The coefficients and frequency response for a simple 11-tap Hilbert transform are shown in **Fig 11.18**. The response of this transform is exceedingly far from flat. It cuts off below about 3 kHz and has about a half dB ripple above this frequency. However, it does allow us to examine several important characteristics of this transform:

- Every other coefficient is zero
- The second half of the coefficients is the negative of the first half
- The amplitude response varies across the passband
- The phase shift is not shown, as it is 90 degrees, plus a constant delay, at all frequencies. If the number of taps is an odd number, the constant delay is an integral number of sample periods, and easily compensated for. The difference between the Hilbert transform output and a constant delay leaves a very accurate 90-degree differential phase shift.

The amplitude response of the Hilbert transform is never completely flat with frequency. As we saw, with only 11 taps, performance is so poor that one would not consider it in a transceiver. As the number of taps is increased, it is possible to not only cover a wider frequency range, but to also diminish the ripple in the pass-band.

Further, our 48-kHz sample frequency is high, as is discussed below. The frequency response of the FIR filters scales with sample frequency. For the 18-MHz transceiver, we can allow the 48 kHz to remain, if the number of taps is raised. A value of 247 was selected. The computational load is only about half of what it seems, since every other coefficient is zero and does not need to be computed. **Fig 11.19** shows the resulting response, which is typically flat within about 0.01 dB and always within 0.04 dB. Going back to the phasing analysis of Chapter 9, this contributes a typical opposite sideband response of $20 \log e/2$ which for the 0.01 dB error (voltage error $e=.00115$), results in an opposite sideband suppression of $-20 \log(0.00115/2)$ or about 65 dB. Repeating this calculation for the worst case 0.04-dB error, the opposite sideband is -53 dB.

The DSP program snippet in **Box 7** is the Hilbert transform and compensating delay. The structure is so similar to the conventional FIR filter described in Chapter 10, that only the Hilbert transform specific portions will be discussed.

The zero coefficient values are not entered at all in the table `hilbert_coeff`, cutting the table size almost in half. To see how zero multiplies occur, it is useful to remember that the data are arranged in a circular buffer. The second time the instruction, `dm(i0, m1)=mr1` occurs, the new data are placed at the location in the buffer pointed to by `i0` and the pointer is increased by `m1`, which has a value of one. Within the FIR multiply-and-accumulate loop, `mx0` is loaded with data from `mx0=dm(i0, m0)` where `m0` has a value of two. This causes the pointer, `i0`, to be incremented by the value two after the data are fetched from memory, skipping every other data point. When the counter reaches zero, the loop is broken and after the last computation, `i0` is left pointing to the oldest point in the buffer. The next time through the `do_hilbert` routine, placing data into the buffer causes an increment of one and the FIR computation moves up by one. This brings us to the first of the data points that were passed over in the last FIR computation cycle. And the process continues, moving up one point in the buffer each cycle.

The block diagram of **Fig 11.20** illustrates this same Hilbert transform operation. The top ‘I’ path is a simple delay to compensate for the flat delay of the transform. The bottom ‘Q’ path is a FIR filter in structure, but only the even numbered coefficients are used since the multiplications for the coefficients of zero value are omitted.

As is normally the case with broadband

Box 7 - DSP program for computing a 90° differential phase shift using the Hilbert transform.

{The following are constant and memory declarations placed at the top of the overall program:}

```
.const H3=247;           { Num taps in Hilbert
                           FIR filt }
.const H3P1ON2=124;     { This is (H3+1)/2 }
.const H3M1ON2=123;     { ...and (H3-1)/2 }
.const H3M3ON2=122;     { ...and (H3-3)/2 }

{The Hilbert coefficients are stored in program memory(pm) so they can be fetched at the same time as data is brought in from data memory (dm). The values are read from a file hil_3_48.dat where the values are given as 24-bit hex numbers. The values are left justified 16-bit numbers and padded on the right with two hex zeros. A sample of coefficients would look like:}
021E00
01F500
01D000
01AF00
.var/pm/circ hilbert3_coeff[H3P1ON2];
.init             hilbert3_coeff: <hil_3_48.dat>

{ Each data memory location for the Hilbert transform is declared as follows: }
.var/dm/circ h3delay[H3M1ON2]; { Delay line }
.var/dm/circ h3data[H3];       { Buffer for data }
.var/dm      m1_sav;           { Allows reuse of m1 }
.var/dm      h3delay_i0_sav;    { Allows reuse of i0 }
.var/dm      h3data_i0_sav;    { Allows reuse of i0 }

{ Initialization of the Hilbert transform takes place once at the beginning of the program operation. Zeroing of arrays is useful for simulation, but is not needed for transceiver operation, and is not done here. }
i0=^h3delay;           { Address of delay line
                         memory }
dm(h3delay_i0_sav)=i0;
i0=^h3data;
dm(h3data_i0_sav)=i0;
```

{ This is the Hilbert transform subroutine. It is called during the 48-kHz rate interrupt to generate a 90-degree phase shift between the I and Q channels. Hilbert has independent inputs and outputs for delayed and phase shifted paths. Uses HIL_3_48.DAT running at 48 KHz in order to get response down to 300 Hz. }

```
Delayed path: ar in, ax1 out.
90 deg path: mr1 in, mr1 out.}
do hilbert:          { 48 KHz Hilbert for receiving }
dm(m1_sav) = m1;
m1 = 1;
```

{ First the delayed path to compensate for the Hilbert delay }

```
i0 = dm(h3delay_i0_sav); m0=0; i0=%h3delay;
ax1 = dm(i0, m0);           { get ax1, the delayed output }
dm(i0, m1) = ar;            { Put new data in, update ptr }
dm(h3delay_i0_sav) = i0;   { Save pointer }
```

{ Next the actual Hilbert transform: }

```
i0=dm(h3data_i0_sav); m0=2; i0=%h3data; { i0
points to data }
i4=^hilbert3_coeff; m4=1; i4=%hilbert3_coeff;
dm(i0, m1)=mr1;           { Enter new data and bump ptr 1 }
```

```
} mr0, mx0=dm(i0, m0), my0=pm(i4, m4);
{ FIR multiply and Accumulate loop: }
cntr=H3M3ON2;
do hil_loop until ce;
hil_loop: mr=mr+mx0*my0(SS), mx0=dm(i0, m0),
my0=pm(i4, m4);
{ Process the last point: }
mr=mr+mx0*my0(SS), mx0=dm(i0, m1), my0=pm(i4, m4);
mr=mr+mx0*my0(RND); { mr1 = phase shifted
output }

if mv sat mr;
dm(h3data_i0_sav)=i0;
m1 = dm(m1_sav);
rts;
```

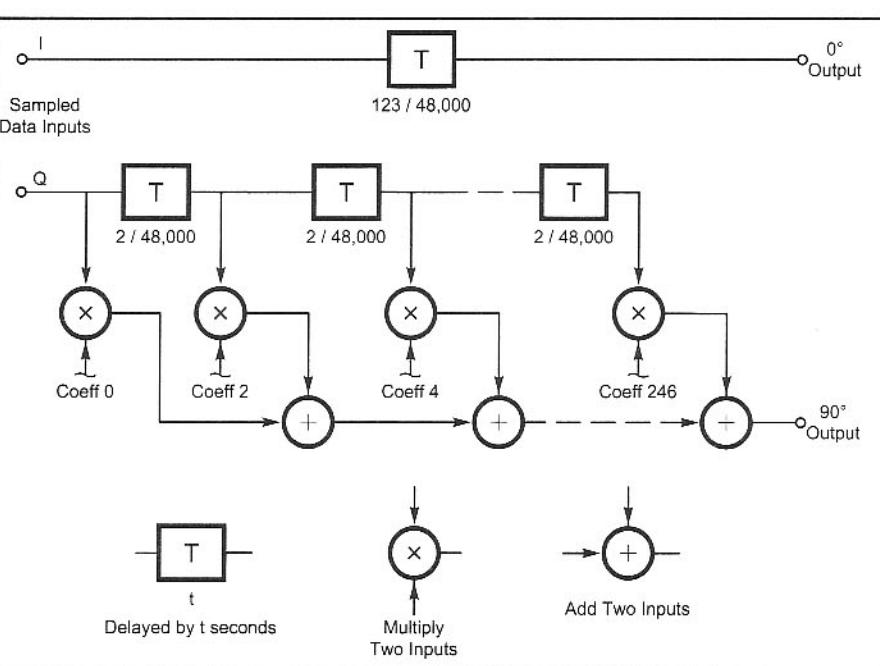


Fig 11.20—Block diagram of the Hilbert transform with 247 taps. The blocks marked 'T' are delays of multiples of sample periods, as indicated on the diagram. Each sample period is 1/48,000 second.

phase shift networks, there is a fixed delay that is much greater than the delay associated with the 90-degree phase shift. For the 247-tap Hilbert transform, and our 48-kHz sample rate, this delay is $0.5 \times (247-1)/48,000$ or 0.0025625 seconds (about 2.6 ms). Other than the need to compensate for this delay, there are no operational problems for a SSB or CW radio.

The second problem in our phasing method of SSB reception was phase and amplitude errors between the two channels. These errors are associated with the mixers and LO hardware and will most likely stay relatively constant over time. If we knew what the errors were we could add in an "anti-error" and have perfect opposite side-band rejection. The degree to which this can be accomplished in practice results in typically 20 dB in improved side-band rejection. Temperature extremes will not allow this to be kept with a simple correction, but the results can be surprisingly good. The problem of knowing what the error is can be solved by merely adjusting the correction until the

opposite sideband disappears.

To understand this process one should think of the error between the desired I (or Q) signal as both an amplitude and a phase shift. This is referred to as an “error vector” and is illustrated in **Fig 11.21**. In the example, not only is the actual signal longer (bigger amplitude) than the desired signal, but there is a phase shift between the two. To correct the signal, we must subtract the error vector from the actual signal. To do this, we

take advantage of the fact that the actual I and Q signals are roughly 90-degrees apart in phase shift. By taking a fraction of the I signal and adding it to a fraction of the Q signal, it is possible to create the negative of the error signal—just what we need to suppress the opposite sideband. **Fig 11.22** shows an implementation for our correction of the sideband suppression. The constants, I_Gain, Q_Gain and QI_Cross_Gain are all numbers between -1 and 1. Both I_Gain and

Q_Gain would not be needed if we allowed gains greater than 1. But it is a convenience to not do this and it is relatively easy to provide the two gain values. Therefore, one of those gains will be set to 1.0, which, in fractional integer arithmetic, is the fraction 32767/32768, entered as a hex value of H#7FFF (see the discussion of fixed-point arithmetic in Chapter 10).

The other gain of the I_Gain/Q_Gain pair can then be set to a value close to 1.0, as determined experimentally. The cross-gain value should be small, but it can be either plus or minus. A value such as +0.05 might be typical and is represented as the fraction 0.05*32768/32768 or 1638/32768 and entered into the program as 1638.

Listing TR18D shows the USB reception routines, including the vector correction. The usual declarations of constants and memory, by name, are at the top of the program.

The three constants that are needed to

Listing TR18D

Phasing method receiver including error correction. The inputs are I and Q signals that have been low-pass filtered.

{The following are constant declarations, placed at the top of the overall program:}

```
.const RGAIN_I=32400; { Adjust value to suit }
.const RGAIN_Q=32767; { Adjust value to suit }
.const RGAIN_IQ=2060; { Adjust value to suit }
```

```
{-----}
```

{The I data is at memory location 'save_i' and the Q data is in sr0}

```
ar = dm(save_i);
my1 = RGAIN_I;
mr = ar * my1 (SS);
dm(save_i) = mr1;
my1 = RGAIN_IQ;
mr = ar * my1 (SS);
ay0 = mr1;
my1 = RGAIN_Q;
mr = sr0 * my1 (SS);
ar = mr1 + ay0;

mr1=dm(save_i);
call do_hilbert;
ay1 = mr1;
ar = ax1 - ay1;

{ Move the I signal data to ar }
{ I Gain correction factor }
{ I signal * correction }
{ Temporary storage }
{ Generate the IQ cross }
{ correction factor }
{ Save cross-correction factor }
{ Q chan gain correction }
{ Q signal * correction }
{ Add in cross-correction }

{ For hilbert }
{ 90 deg; ar, mr1 in; ax1, mr1 out }
{ Get ready to subtract Q out }
{ - = usb }
{ USB audio output is now in register ar }
```

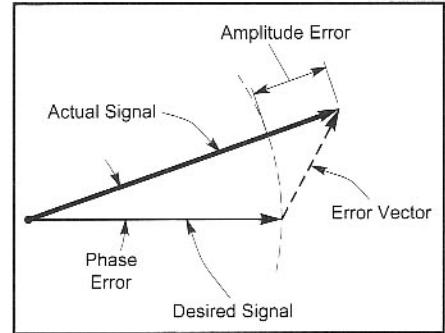


Fig 11.21—Phase and amplitude errors in the phasing method shown as vectors.

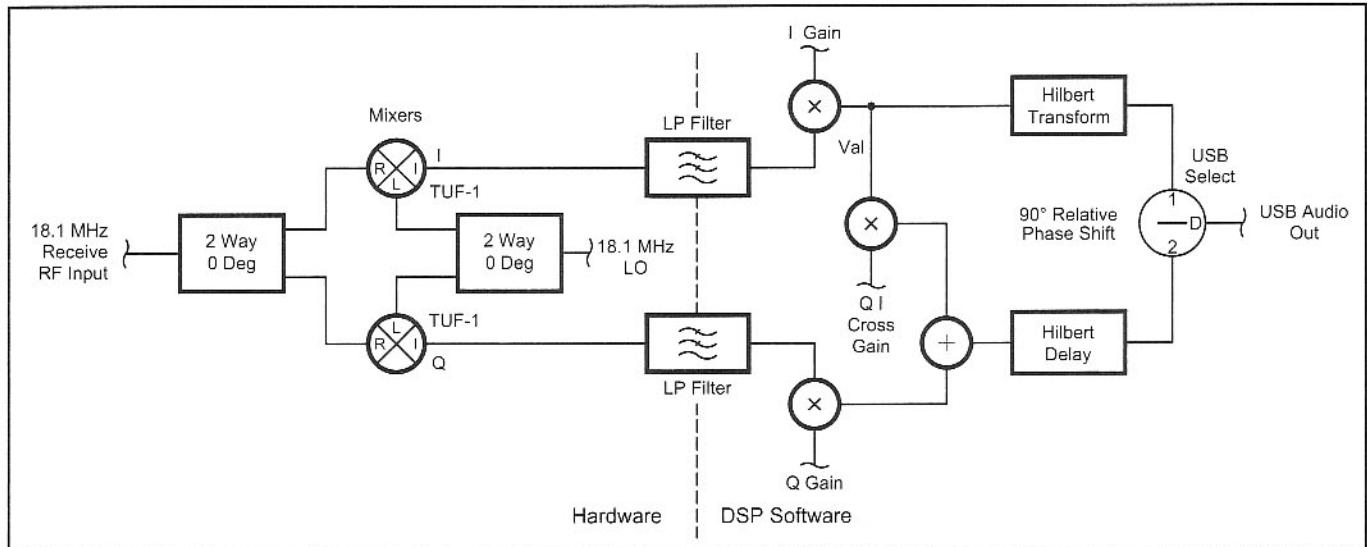


Fig 11.22—Block diagram of a phasing method receiver with DSP software error correction. The cross gain is shown going from the I channel to the Q channel. It will work equally well going in the reverse direction, but both directions are never needed.

suppress the opposite sideband are entered as constants. This is a very simple system, but requires re-assembly of the program to null the sideband. Experience has shown this a reasonable approach, since the settings do not normally need to be changed often. Multiplication by both RGAIN_I and RGAIN_Q occurs each time through the routine, even though one of these constants will have the value of 1.0. This simplifies the adjustment of the constants since we don't know which will have the 1.0 value.

The Hilbert transform, discussed above, is a subroutine invoked by 'call do_hilbert.' This applies the differential phase shift so that the USB can be formed with simple subtraction 'ar=ax1-ay1.'

Also shown in the listing is the audio gain control. One of the conveniences of a DSP implementation is having gain control steps in constant dB amounts. For analog gain controls, this is approximated with what are called "log" potentiometers. Our DSP implementation starts with the binary shifter as a basic component. If the signal word is shifted left by one bit, the result is an increase in level of 6.0 dB. Shifts to the right decrease the audio level by the same amount. This has the desired equal dB amounts per step, as well as great simplicity. The drawback is that the steps are too big. Experience suggests that 1-dB steps seem too small, but 1.5 to 2-dB steps allow one to choose a comfortable audio level with a reasonable number of button pushes.

We implement 1.5-dB steps by having a table of four entries corresponding gains of 0, -1.5, -3.0, and -4.5 dB. This table, stored in program memory, is called 'aud_gain' and provides multipliers that can be used between the 6.0-dB steps. As an example, a gain of -1.5 dB is a voltage ratio of $10^{(-1.5/20)}=0.8414$. In fractional arithmetic this is a value of $0.8414*32768=27571$, which in hexadecimal form is H#6BB3. The program memory words are 24-bits wide, but only 16 bits of this are available when used as data. The bits will be properly aligned if the hex values are padded on the right with '00.' Thus, the -1.5-dB entry in hexadecimal is H#6BB300.

The button control parts of the program have setup two values for the audio gain control, 'af_gain' which contains one of the 1.5-dB step multipliers, and 'af_shift', which is the number of 6-dB steps. These shifts can be either plus or minus.

Audio Filtering

The general nature of FIR filters has already been covered. Here we apply these principles with two receive filters, a 3-kHz

low-pass filter suitable for either all modes, and a 500-Hz wide band-pass filter for CW use.

The index register pointer, i0, of the DSP is used to find the data points for the FIR filter. Initialization of this register is critical. Omitting this can cause hours of grief in getting the DSP program to operate. The program may function at times and fail at others, depending on the random initialization. The program instructions for this initialization are:

```
i0=^idata;
dm(fir1i_i0_sav)=i0;
```

When the FIR filter is called, the pointer i0 is loaded by the instruction

```
i0=dm(fir1i_i0_sav);
```

all of which allows i0 to be reused in many routines.

Binaural Delay

This feature is always in operation for the transceiver. The addition of a delay of about 10 milliseconds in the sound heard by one ear, relative to the other has interesting effects, very closely related to the I-Q binaural effects used in Chapter 9. The noise heard by the two ears loses correlation and allows the mind to better distinguish between a CW tone and the noise.

On CW, the tone takes on the effect of having a spatial position that depends on the tone frequency. The noise position is, in effect, always moving around "inside your head."

As a signal is tuned, the phase relationships between the tones heard by the ears changes for the delay system. For the I-Q binaural, it is a constant 90 degrees while the phase shift for the delay binaural increases with frequency. For the 10 millisecond delay the phase shift is 90 degrees at $1/(4*0.01)=25$ Hz and changes quite rapidly with tuning. Thus, the two systems do not have the same sound when tuned. In either system the noise is uncorrelated and the sound is similar, not unlike an FM stereo radio without an antenna. Probably the biggest difference is that the I-Q binaural system receives both sidebands, whereas the delay binaural is compatible with SSB. The delay binaural is in the final audio path and is compatible with any mode.

Implementation of a binaural delay requires some memory for storing the signal, but very little computation is needed. Listing TR18E is the portion of the DSP program required.

Operation of this delay line is closely related to the address generators used by the ADSP-2181 DSP.

A segment of memory, such as our 'delay [DELAY_SIZE]' can be designated as circular by the key word 'circ.'

DELAY_SIZE is the same as the constant 512 and so this many words of data memory are set aside. Each word is 16 bits,

guish between a CW tone and the noise. On CW, the tone takes on the effect of having a spatial position that depends on the tone frequency. The noise position is, in effect, always moving around "inside your head."

As a signal is tuned, the phase relationships between the tones heard by the ears changes for the delay system. For the I-Q binaural, it is a constant 90 degrees while the phase shift for the delay binaural increases with frequency. For the 10 millisecond delay the phase shift is 90 degrees at $1/(4*0.01)=25$ Hz and changes quite rapidly with tuning. Thus, the two systems do not have the same sound when tuned. In either system the noise is uncorrelated and the sound is similar, not unlike an FM stereo radio without an antenna. Probably the biggest difference is that the I-Q binaural system receives both sidebands, whereas the delay binaural is compatible with SSB. The delay binaural is in the final audio path and is compatible with any mode.

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A segment of memory, such as our 'delay [DELAY_SIZE]' can be designated as circular by the key word 'circ.' DELAY_SIZE is the same as the constant 512 and so this many words of data memory are set aside. Each word is 16 bits,

Listing TR18E

DSP program snippets for delay binaural sound.

{The following are constant and memory declarations, placed at the top of the overall program:}

```
.const      DELAY_SIZE=512;
.var/dm/circ  delay[DELAY_SIZE]; { The delay line, binaural }
.var/dm      del_i0_sav;          { Storage when not in interrupt }
```

```
{-----}
```

```
{ This part of the program is executed at startup to initialize the
pointer to the delay line, delay[]. }
ax0 = ^delay;           { Get the address of delay line }
dm(del_i0_sav) = ax0;  { The pointer is saved here }
```

```
{-----}
```

```
{ This program snippet is executed at each 48 kHz interrupt to put the
left channel data into the delay line, and to take the delayed data
out for the right channel. Left data is in register sr1:
i0=dm(del_i0_sav);    { Load i0 pointer }
m0=0;                  { Do not adjust the pointer, now }
l0=DELAY_SIZE;          { The length of the circular line }
mr1=dm(i0, m0);        { Remove the delayed signal }
m0=1;                  { Now increment pointer on write }
dm(i0, m0)=sr1;         { Put the new signal in the line}
dm(del_i0_sav)=i0;      { Save the pointer for next time }
dm(tx_buf+2) = mr1;     { Send audio data to right D/A }
```

adequate to store one sample of the audio waveform. This is illustrated in Fig 11.23. There are 8 address generators, and the binaural delay uses only one of these, generator zero. Three parameters control the generator, $i0$, $m0$ and $l0$. $i0$ is a pointer, meaning that it is an address in memory. $m0$ is an increment amount that tells the generator to add the value of $m0$ to $i0$ after doing either a read or write operation. $i0$ applies if the buffer is circular, and tells the address generator to not point to memory locations past the base location plus $i0$, but instead to wrap around to the beginning. Note that $m0$ can be zero or negative. Negative values mean that the progress through the circular buffer is in the reverse direction.

Returning to the listing, the value of the pointer is restored to $i0$ with ' $i0=dm(del_i0_sav)$ ' and $m0$ is set to zero, meaning that no change will occur to $i0$ when the delay line is accessed. $l0$ is set

to the length of the circular buffer, $DELAY_SIZE$. The right audio channel signal sample is next removed from the line with ' $mr1=dm(i0, m0)$ ' and left temporarily in register $mr1$. The increment register, $m0$, is now changed to one. When we put the new audio data into the delay line with $dm(i0, m0)=sr1$, the pointer, $i0$, will now have one added to it following the memory write. What this does is to move $i0$ to the location of the now oldest data point. After 512 applications of this routine, the pointer will be again pointing to the data point that was just entered. This delays the data by $512/48,000$ of a second, or about 10.7 milliseconds.

stants are needed, as there are differences in the audio paths, due primarily to the differences introduced by T/R switching.

CW Transmission

This mode requires that the frequency of the transmitted signal and the received "zero-beat" signal be offset by a tone frequency, such as 800 Hz. Some sort of TR activated switching device can be used in the VFO to provide the offset as was seen in Chapter 6. Alternatively, an audio tone can be generated and passed through the SSB generator. The VFO never changes frequency and the offset can be precise. Unfortunately, there often are two undesired signals accompanying the CW signal. The VFO output must be suppressed by the quality of the mixer balance. Mixers, such as the Mini-Circuit TUF-1 can have 50 to 60 dB of inherent L-R balance. It is often possible to increase this by 10 dB or more by adding a very small gimmick capacitor between the LO signals and the mixer output. Fig 11.25 illustrates a general approach for increasing the mixer balance in this way.

The second undesired signal is the opposite side-band. This, however, is the same problem that was solved for SSB with the I-Q vector correction. This suggests a method for adjustment of the correction constants. If we transmit a CW tone and receive the unwanted side-band on a local communications receiver, the S-meter can be used to find a null. The correction constants are those that make the signal disappear.

Fig 11.26 shows the screen of a spectrum analyzer attached to the output of the 18-MHz transceiver with the key down. The VFO is in the center of the screen at 18.100 MHz. Each division is 500 Hz and the tone frequency is 850 Hz. With USB being used, the transmitted signal is above the carrier frequency. Suppression of the carrier is 48 dB and the opposite side-band, 850 Hz below the center, is 63 dB below the transmitted signal. An additional signal can be seen 1700 Hz above the VFO frequency. This is due to the modulation of the second harmonic of the 850-Hz tone. This undesired output is suppressed 50 dB. One would always want all spurious signals to be undetectable, but in the real-world way of such things, these levels are acceptable. This level of spurious signal will, in general, be covered by the key-clicks in almost any CW transmitter.

Key-click suppression is normally dealt with by limiting the rise-time of the keying waveform. It can be shown that this will cause the key-click spectrum to fall off much faster as one tunes off the CW signal. It is possible to increase the rate even

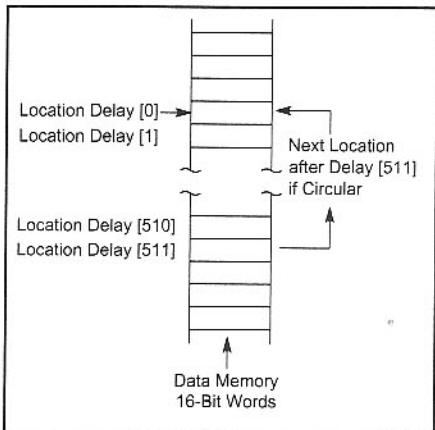


Fig 11.23—Circular data buffer used to implement a 512 point delay line as is used for delay binaural operation.

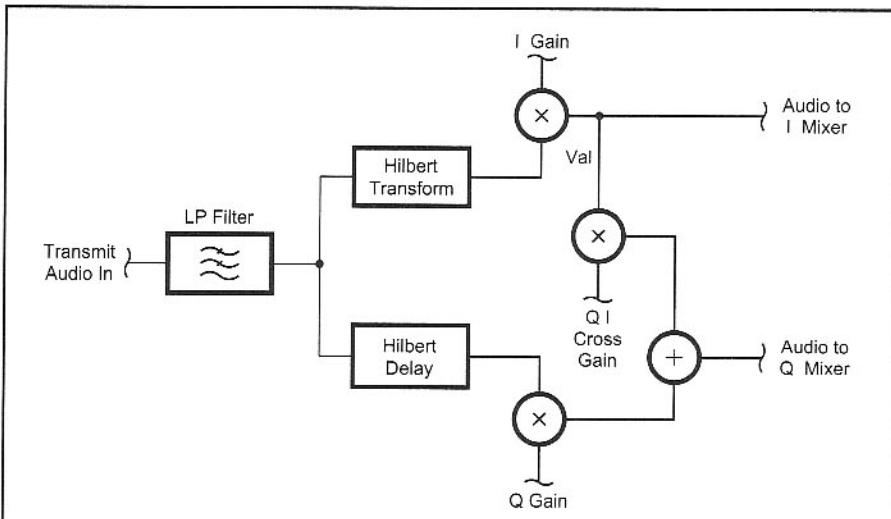


Fig 11.24—Simplified block diagram showing the I and Q corrections to improve the unwanted sideband rejection for transmit.

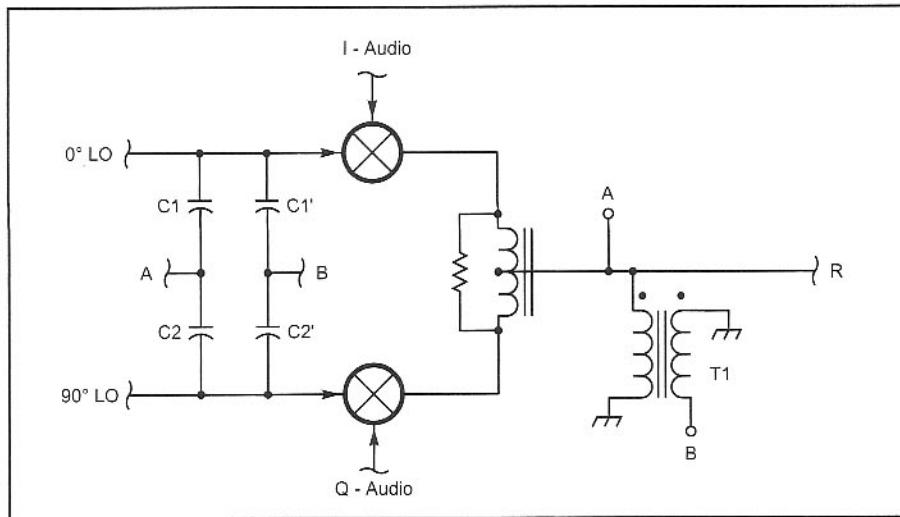


Fig 11.25—Schematic diagram a circuit for increasing L-R isolation of a balanced mixer. In order to minimize the capacitance values, one should never use both C1 and C1' or C2 and C2', as this would only increase the size of both capacitors. All capacitors are a fraction of a pF, made from gimmick wires, which are merely two enamel covered wires twisted together. The transformer, T1, is 5 turns of #26 bifilar wire on a small ferrite core, such as Amidon FT-23-43.

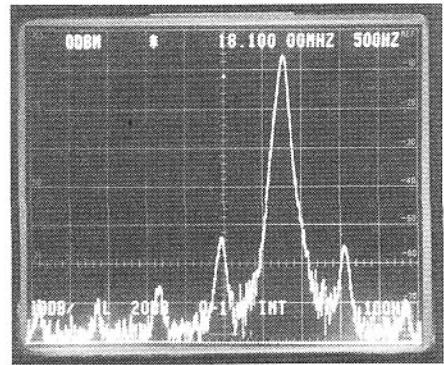


Fig 11.26—Output spectrum of 18-MHz transceiver in CW mode. The carrier is at the center of the screen. The transmitted signal is the large response 1.7 divisions to the right. The small response the same distance to the right is the unwanted sideband. Measurements were done with a Tektronix 494 analyzer.

more if, not only the rise-time is limited, but the keying waveform is made to have rounded corners at turn-on and turn-off. A direct way to insure that this happens is to pass the keying waveform through a low-pass filter and then use the resulting waveform to amplitude modulate the RF signal. In our case, the modulation can be applied to the 800-Hz tone, before it goes to the Hilbert transform and then to the mixers. As an added benefit, the 800 Hz is available for use as a transmitter side tone, ensuring that a station is tuned in correctly when the received tone is the same as the side tone.

The filter used here is a 500-Hz LPF. The 48-kHz sampling rate requires about 200 taps on the FIR filter, but the DSP is not busy during CW transmission, so this is not a problem. As shown in **Listing TR18F**, amplitude modulation in the DSP is accomplished by generating a sine-wave at the CW offset (800 Hz) and multiplying this by the output of the key-click LPF. This is repeated for a 90-degree phase shifted Q signal by generating a cosine wave and repeating the modulation. The output of the key-click low-pass filter has overshoot that is slightly greater than the input. This is a necessary part of limiting the transmit spectrum. To ensure that this is not saturated by the low-pass FIR filter, the input to the filter is reduced in amplitude by a factor of 0.91, as shown.

The I and Q corrections for improving the side-band suppression uses the constant values GAIN_I, GAIN_Q and

Listing TR18F

DSP routines used to generate a CW transmit signal

```

xi_cw:
filt.

ax0 = dm(key);
none = pass ax0;
ar = 0;
if ne jump xi_cw1;
ar = 29491;
xi_cw1: call fir_xmt_cw;
my0 = mr1;
ax0 = dm(cw_dphase);
ay0 = dm(cw_phase);
ar = ax0 + ay0;
dm(cw_phase) = ar;
{ If key is down, put a .9 (29491) into CW fir
Modulate fir output onto carrier. This scheme
allows top space for overshoot in the fir. }
{ Get hardware CW key data }

{ CW off }
{ CW key is up }
{ 0.9 to key click filter }
{ Input in ar, output in mr1 }

{ Phase increment for lo }
{ Last phase }
{ New phase }
{ For next time }

ax0 = dm(cw_phase);
call sin;
mr=ar*my0(SS);
ar = -mr1;
{ ax0=Phase, Sin returned in AR }
{ CW Gate }
{ Make USB}

my1 = GAIN_I;
mr = ar * my1 (SS);
ar = mr1;
{ Gain correction factor }
{ Keyed sine wave * correction }
{ Corrected I signal }

my1 = GAIN_IQ;
mr = ar * my1 (SS);
dm(t1) = mr1;
dm(tx_buf + 1) = ar;
{ Cross-correction for Q }
{ In-phase transmit i-f sig out }

ax0 = dm(cw_phase);
ay0 = 16384;
ar = ax0 + ay0;
ax0 = ar;
call sin;
mr = ar * my0(SS);
my1 = GAIN_Q;
mr = mr1 * my1 (SS);
ay0 = dm(t1);
ar = mr1 + ay0;
{ That takes care of I, now Q: }
{ The phase used for I chan }
{ 90 degrees for quadrature lo }
{ Q chan phase }

{ Cos lo sig, sin() preserves my0 }
{ CW Gate for Q signal }
{ Q chan gain correction }

dm(tx_buf + 2) = ar;
{ Now add in cross-correction }

{ Quadrature transmit sig out }

```

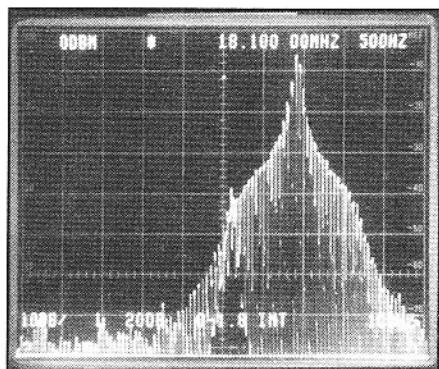


Fig 11.27—Measured spectrum of the transceiver in CW, when being keyed on and off at 10 dots/sec. The horizontal scale is 500 Hz/div and the vertical scale is 10 dB/div.

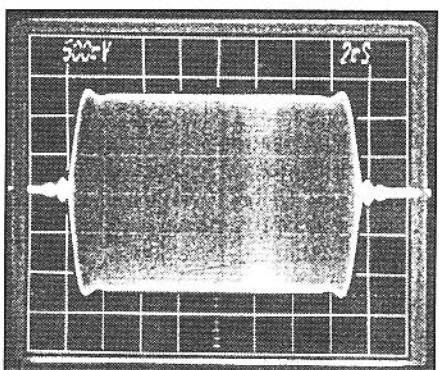


Fig 11.28—RF waveform that results from the keying low-pass filter. The small ripples at the ends of the waveform are a result of the key-click reduction. This waveform was measured on the DSP-10 transceiver, outlined later in this chapter, that uses the same keying system as the 18-MHz transceiver.

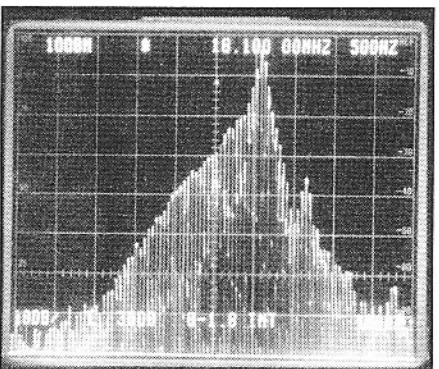


Fig 11.29—Measured spectrum of a commercial transceiver in CW operation, when being keyed on and off at 10 dots/sec. The horizontal scale is 500 Hz/div and the vertical scale is 10 dB/div. This spectrum is typical of signals on the air with their key-click spectrums limited by rise and fall times. It is shown here for comparison with the DSP derived spectrum of Fig 11.27.

GAIN_IQ. As was the case for reception, either GAIN_I or GAIN_Q should be kept at a value of +1 (32767 integer.)

The resulting key-click spectrum (see Fig 11.27) is cleaner than many commercial transmitters and sounds very good on the air. The spectrum is down about 30 dB at an offset of 500 Hz. Fig 11.28 is the keying waveform at the output of the key-click low-pass FIR filter. The small ripples that both precede and follows the main keying transitions are characteristic of a frequency constrained waveform. These ripples are not heard by the ear when receiving the signal. If they were not present, the ear would hear the well known key-click sound. For comparison, Fig 11.29 is representative of the key click spectrum for transmitters that shape the keying by limiting the rise and fall times. This was measured on a commercial transmitter of 1990 vintage. The far-out spectrum tends to fall off more slowly than the DSP shaped system produces.

Control Functions

Four push-button switches are used to communicate data into the DSP for the 18 MHz transceiver:

Button 1 - Turn the audio gain up 1.5 dB.
Button 2 - Turn the audio gain down 1.5 dB.

Button 3 - Alternate between Upper Sideband and CW modes.

Button 4 - Alternate between a wide-band SSB filter and a narrow-band CW filter.

Operation of all four push-buttons is the same.

Push-button switches are prone to having multiple on/off states when they are first pushed, referred to as "contact bounce." The effects of this can be eliminated with hardware de-bounce circuits, or in our case this can be done in the DSP. A software counter, bcounti is used to measure how long the ith switch has been depressed. The counter is initially set for a value of 100, meaning that the switch has not been pushed. The interrupts occur every 1/48,000 second at which time the switch state is read. If the switch has been pushed, the counter is diminished by one, but not allowed to go less than zero. If the switch has not been pushed, the counter is increased by one, but not allowed to go above 100.

In the background portions of the program, the counters are examined. If any of them are at zero, they are considered to have been pushed, that is, the button has been down at least $100/48,000 = 2.083$ milliseconds and is now "de-bounced." So, the appropriate action for the switch, such as turning up the audio gain is performed. Next, a flag is set so that the further indi-

cations of the switch having been pushed will be ignored until the counter has returned to 100. This is saying that each push of the button must be followed by a release. There are no extra repeated actions for holding the buttons down.

The details of this de-bouncing and button interpretation are covered with comments in the program *TR18A.DSP* on the book CD for those wanting to see an example.

Sampling Rates For The 18-MHz Transceiver

The A/D and D/A converters for the transceiver operate at a 48-kHz rate. This provides an audio response to at least 20 kHz. In the case of the transmitter, it is totally inappropriate to transmit signals with such bandwidths, and low pass filtering is provided to prevent this. In the case of the receiver, it is interesting to be able to have wider bandwidths than the conventional SSB filters give. Typically, in the interest of QRM rejection, these filters cut-off in the 2.5 to 3.0 kHz region. Some people find the narrower filters creates a muffled sound to the audio. A high sampling frequency gives ample opportunity to experiment with this.

Another example of an algorithm that benefits from a high sampling rate is a noise-blanker. Signals are easily stored in a delay line while decisions to blank are made. As discussed in Chapter 10, if sufficient bandwidth is available, the presence of noise could be determined by the nature of the wide-band signal relative to the desired signal being received.

It is challenging to maintain high opposite side-band rejection with an analog I-Q phase-shift network. In the case of the Hilbert transform approach in DSP, the only difficult part is keeping good amplitude response at low frequencies (around 300 Hz.) The high frequency side of the Hilbert response continues up to within a few hundred Hz of half the sampling frequency. Thus the opposite sideband rejection bandwidth can be very wide.

One of the interesting effects from using a wide bandwidth for SSB reception is a new view of transmitter splatter. One hears the transmitter splatter, not as off-frequency hash, but rather as a distortion to the voice. It is possible to make judgments of transmitter cleanliness by tuning the signal in and listening for the distortion. The excellent linearity of the A/D converters makes the receiver an insignificant contributor to the distortion being heard.

As usual, there are some negative features of using a high sampling frequency. The most obvious is the increased load on

the processor. With a sampling frequency of 48 kHz, there is a maximum time of $1/48000=20.833$ microseconds to process the interrupt. The ADSP-2181 processor completes 33 instructions per microsecond and so there are a maximum of $20.833 \times 33 = 687$ instructions per interrupt. During reception these are allocated roughly as:

FIR Filter I	143
FIR Filter Q	143
Hilbert Transform	148
I-Q vector correct	10
Audio gain control	4
Binaural delay	7
Other receiver jobs	62
Buttons	<u>56</u>
Total	573

This uses about 84% of the available time, but leaves adequate time for the background processing. Background tasks are chosen because they have neither deadlines, nor rates of occurrence that they must achieve.

A second drawback to a high sampling rate is the response of FIR filters. These can have fast rates of cut-off outside of the pass-band, but the filter shape still scales with sampling frequency. We get satisfactory response for the 18-MHz transceiver using a 48-kHz sampling rate. But if we needed greater selectivity, there would be two approaches possible. We could run a lower sampling rate. A rate of 10 to 15 kHz would still support excellent audio response for communications.

A second way that allows the FIR filters to have a low sampling rate and also have a wide-band system available is to use multiple rates. This approach, called decimation is illustrated in **Fig 11.30**. The

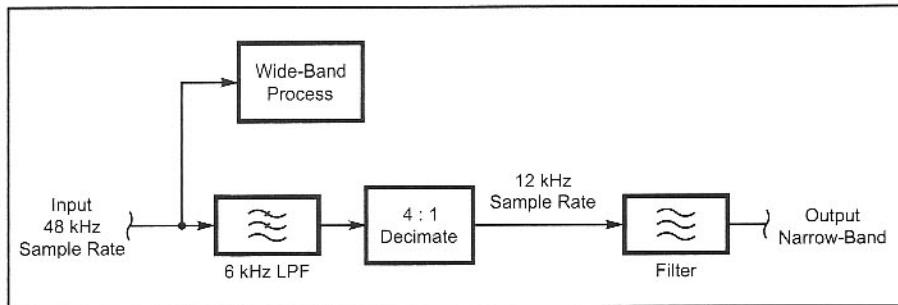


Fig 11.30—Use of decimation to improve filter response and to reduce computational load. The process of decimation first low-pass filters the data and then discards a fraction of it that is no longer needed to satisfy the Nyquist sampling criteria.

basic process is to limit the bandwidth to a fraction of the total bandwidth using a low-pass filter. In this example, the filter cuts off all significant signals above 6 kHz. Next 3 out of every 4 samples are discarded. The Nyquist sampling criteria is met since the new sampling rate of 12 kHz is at least twice the frequency of any signal that we are processing. The selectivity of all filters, low-pass, band-pass or any other, will be improved by a factor of four. Alternatively, the selectivity can be maintained, but the numbers of taps in the FIR filters can be reduced.

The gains of decimation are great. Not only can the number of FIR taps be reduced, but the processing load is also reduced because the sampling rate is down.

Analog vs Digital

One may already have noticed some strong resemblances between the R2 receiver and the mixer/I-F circuits of this 18-MHz rig. It is interesting to compare the two circuits to see where the use of

DSP has changed the implementation.

The I-F filter/diplexer, built around L4 and L5 is identical. Switches, U5A-U5D are added to allow T/R switching and so are needed with either implementation. The R2 uses audio filtering that is in the DSP for this rig. Audio amplification is needed for both implementations since the signal levels coming from the mixers can be of sub-microvolt levels. For the DSP implementation, RF filtering, consisting of 1500-pF feed-through filters, is needed to keep noise from the DSP processor from getting back into the RF circuits. And, of course, the biggest difference is that the DSP implementation requires A/D and D/A converters plus the processor.

The overall complexity and power consumption of the DSP implementation are both greater than that of their analog counterparts. The compensating feature is the performance of functions such as filtering and sideband suppression, along with the ability to make changes and add features without hardware changes.

11.5 DSP-10 2-METER TRANSCEIVER

As the complexity of an electronic project grows, the amount of time and technical skill required for successfully completion easily exceeds the allowable bounds for "weekend experimenters." Much of the material in this book emphasizes ways to have success with a project by using simple approaches and limiting the features. QRP amateur construction and operation has thrived on this approach. This view can be modified somewhat when the project has significant portions implemented in software. An example is the DSP-10 all-mode 2-meter transceiver using a DSP-based last I-F and audio sections with a computerized front panel.

The details for the DSP-10, including the *QST* article and all of the computer programs, are included on the *Experimental Methods in RF Design* CD. The following material is an overview of the project that shows the overall scope and content. Most of the DSP programs involve routines that have been discussed in Chapters 10 and 11. A major distinction is that the control program, written in the language 'C', runs on a personal computer (PC) and communicates with the DSP through a 9600-baud serial connection.

Fig 11.31 is an overall block diagram of both the hardware and DSP software for the transceiver. Dual conversion is used in

the mixing process to convert between the 144-MHz RF frequency and the 10-to-20-kHz DSP I-F. Coarse tuning with 5-kHz steps is done at the 126-MHz first conversion synthesizer. Fine tuning to less than 1-Hz steps is provided by in DSP software. PIN-diode and CMOS switches select the direction of signal flow in the RF hardware.

All signal generation and detection is DSP based in the general style of the 18-MHz transceiver described previously in this chapter. At the 10-to-20-kHz I-F, two software I-Q mixers are driven by software generated sine waves at 0 and 90-degree relative phase shifts. This forms

the basis for precise SSB conversion to audio. For FM, an *arc tangent detector* is used as outlined in section 10.9, FM Reception. Audio processing starts with an AGC followed by FIR filters for either band-pass filtering or *LMS denoise* filtering.

An FFT spectrum analyzer operates continuously, providing a spectral display on the PC. The spectral data is sent to the PC via a serial port operating at 9600 baud. The UART* for the serial port is in the DSP software, again simplifying the needed hardware. A continuous display of the data is very useful for determining the usage of the spectrum as well as for detecting the presence of signals that are too weak to be heard by ear. The DSP-10 also has provision for very weak signal (but slow) com-

munications using this data.** More is said about this in Chapter 12.

DSP-10 Front Panel

In order to provide an adequate human interface for a transceiver of this complexity, the control comes from a PC. Even at that it represents a rudimentary approach to a “front panel” in that only keyboard commands are used and the program runs under DOS. Control settings, such as **FREQUENCY** and **AUDIO GAIN** are displayed along the left side of the panel. On the right side, the topmost portion of the screen is keyboard driven transmit data that will be sent in Morse code. Following down the right side is a spectrum analyzer display that represents the current receiver audio.

Below the spectrum analyzer display is a large block containing a long-term presentation of spectral signal strength, called a *waterfall display*. Brighter colors represent greater signal strength as illustrated in Fig 11.32. Each time that the spectrum is calculated for the upper display, a new row of pixels is added to the waterfall display. Eventually the display area is fully used and the display must scroll up to show only the newest data. This general type of spectral display has been widely used to look for patterns representing “coherent” signals. The human capability for pattern recognition operates well here.

Finally along the bottom of the screen is a status line that can be used for a variety of purposes ranging from diagnostic status information to the current position of the Moon or Sun.

Additional DSP-10 Features

Also available through the software are:

- Eight audio filters of varying characteristics
- One audio filter that can be customized

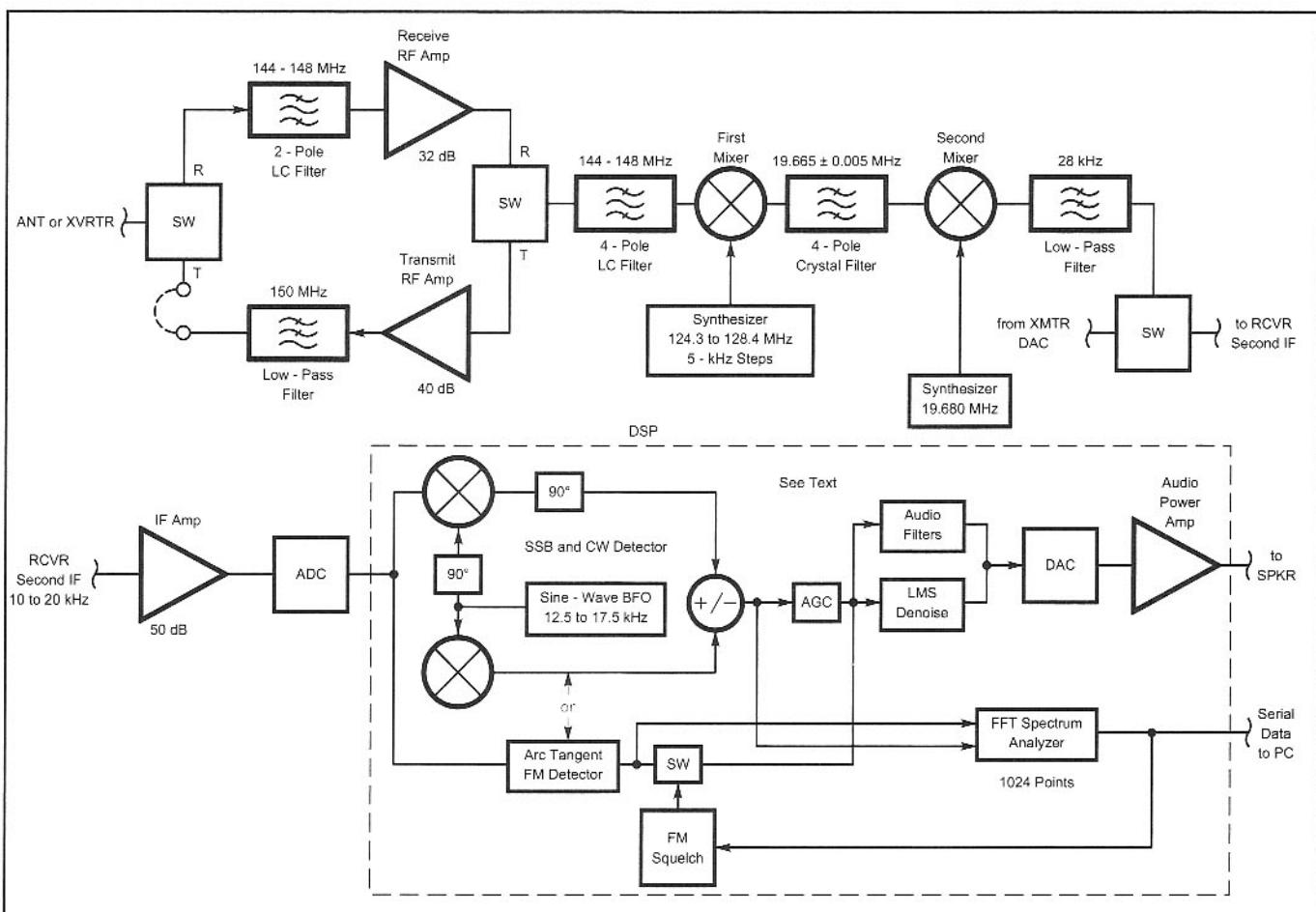


Fig 11.31—Overall block diagram for the DSP-10 2-meter transceiver. The portion inside the dashed lines is implemented as a DSP program. Not shown here are the control and display functions that are implemented in a PC.

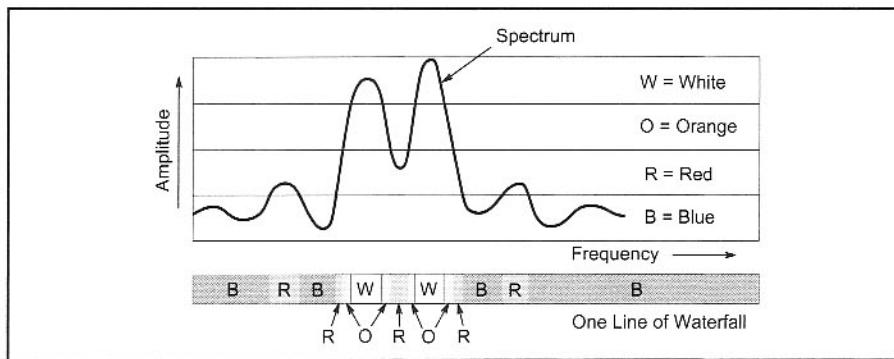


Fig 11.32—Diagram showing how the upper spectral is “sliced” into colors to form the one line of the waterfall display. While this simplified diagram has only four colors, the waterfalls usually have 16 colors or more. Added colors improve the ability to see weak signals against a noise background.

- Auto-Notching of tones
- Automatic correction of receiver frequencies for EME* operation⁸
- A variety of long-term averaging methods
- Frequency corrections for external transverters**
- Accurate S-meter reading displayed in dBm
- Saving of spectral data in computer files

This summary of the features illustrates the potential of adding sophistication to the radios operation through software. The initial radio can be quite primitive with the features growing with time. New features are added to existing radios by loading the new software. This process lends itself to group activities, where the final product can be shared by software distribution.

An additional characteristic of the software-based radio is the ability to change its “personality” by the loading of different software. Often, new modes of operation and control of the radios operation may be added as software is written. However, the hardware design process is challenged to anticipate future applications. Adding a little more control, such as a gain adjustment, to the hardware may allow considerable growth in capability by future software changes. However, adding control of enough functions and having

adequate bandwidth for future needs may instead add considerably to the cost and complexity of the hardware. Which brings back the point made for all-hardware radios, that the price of trying to make a software radio totally flexible may well be an unfinished project!

DSP-10 Multi-Rate Processing

As discussed earlier, the only hardware interrupt occurs at a 48-kHz rate. Certain processes, such as the audio filtering and serial data transmission, do not require this high rate of processing. To minimize the processing time requires, much of the process is performed at 1/5 rate, or 9600 Hz. Since this is a sub-multiple of the basic rate, only the one interrupt routine is needed.

Within the interrupt routine, a software divide-by-five is used to determine which of the 9600 rate routines are to be pro-

cessed. Even though the processing load will generally not be evenly divided between the five 9600 rate routines, all of the remaining time is still available for the background routines. The key design parameter is the longest running of the five routines. This must not exceed the 1/48000 second (20.833 microseconds) that is available between interrupts.

Provision is made for using a triggered oscilloscope to measure the amount of time spent in the interrupt routines. At the start of each interrupt routine, a hardware logic level output is set high. Returning from the interrupt routine sets the line low. This allows an oscilloscope to see each of the five routines and their running times. Most triggered oscilloscopes have a variable “time/div” which needs to be set to just cover the $5 \times 20.833 = 104.2$ microseconds. Usually it is undesirable for the oscilloscope to trigger for the next 104.2 microseconds. If there is a “Hold-Off” adjustment on the oscilloscope, this is easily handled. Otherwise, some care in setting the trigger level will normally result in a consistent trigger point.

DSP-Based Audio Processor

The DSP-10 radio uses an I-F of 10 to 20 kHz with a digital sampling rate of 48 kHz. However, nothing restricts using the I-F portion of the radio without RF hardware by extending the input frequency range down into the audio range. When the “BFO” gets to zero Hz, one has an audio processor. What this means is that the same EZ-KIT Lite DSP board used for the other projects in this chapter becomes a full-featured audio processor, suitable for use with any transceiver. Only two el-

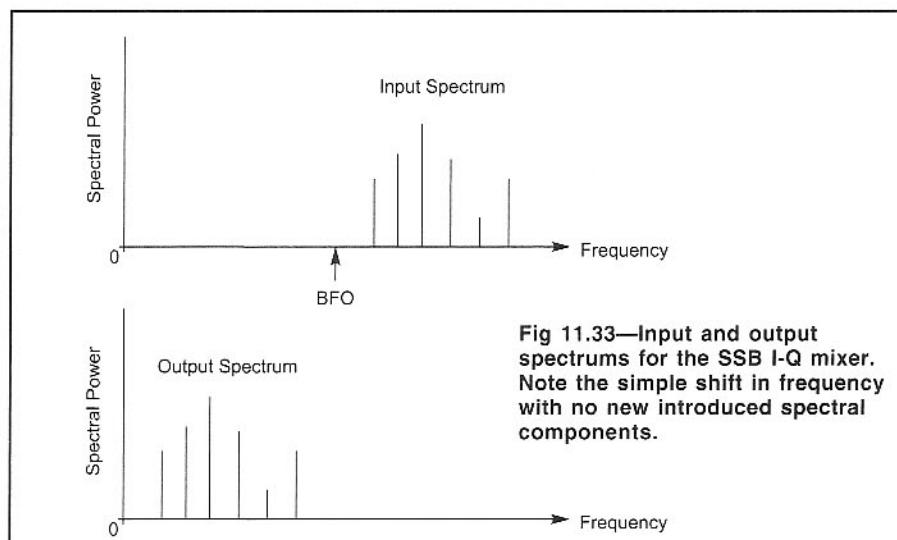


Fig 11.33—Input and output spectrums for the SSB I-Q mixer. Note the simple shift in frequency with no new introduced spectral components.

*EME refers to the Earth-Moon-Earth path of signal reflection. Due to the Earth's rotation and the non-circularity of the Moon's orbit, there is a Doppler shift in the returned signal. This shift is up to about ± 400 Hz at 2-meters and proportionally more at higher frequencies.

**Operation at frequencies other than 2-meters is possible by using *transverters* to produce external frequency mixing of both the transmitted and received signals.

ements are *not* fully achieved without adding the DSP-10 RF hardware:

- Accurate RF frequency control under an external 10-MHz reference
- Tight integration of the control functions, such as frequency display and transmit/receive sequencing.

The overall block diagram of the audio processor is the DSP portion of Fig 11.31 that is inside the dashed lines. Modes such as FM make little sense when the input is the audio coming from a receiver, but they remain available waiting for an application! Since the SSB mixing structure remains on the input to the audio processor, it is possible to provide a frequency offset,⁹ as shown in Fig 11.33. The I-Q mixing removes the lower sideband that would appear as a mirror image of the input spectrum, folded about the BFO frequency. The very high balance of the DSP multiplier mixers then allows the input and output spectrums to overlap without interference. The frequency display is modified for the audio processor and displays a *Frequency Offset* in Hertz in place of the radio frequency.

The DSP-10 audio processor can be used as a 0 to 20-kHz spectrum analyzer. At any time the frequency band being observed can be 1200, 2400 or 4800-Hz wide with resolution bandwidths of about 3, 6 or 12 Hz respectively. The vertical display can be set to 1, 2, 5 or 10 dB/div and unlimited video averaging is available through the PC software.

The DSP and PC programs that are used for the DSP-10 RF operation also support the audio processor. The executable programs, along with all source code are available on the *Experimental Methods in RF Design CD*. The general requirements for the audio processor are:

- An EZ-KIT Lite to run the DSP program.
- A PC to run the control program. This runs under DOS and uses 640x480 VGA 16-color graphics. A serial port is needed for communicating with the EZ-KIT. The computer need not be fast; a 486 level is adequate. This is a great application for the old computers that are collecting dust somewhere.
- An audio cable connecting between the receiver audio output and the EZKIT input.

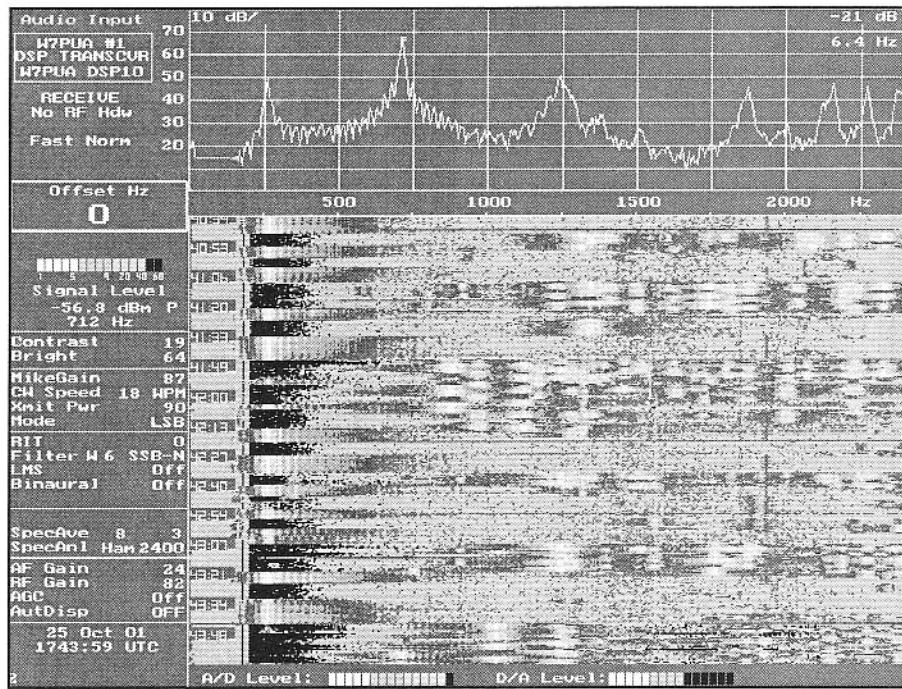


Fig 11.34—Audio processor display with operation on 10-meter CW. The top graph is the latest measured audio spectrum, which is updated every 0.6 seconds. Each of the approximately ten peaks are CW stations. The lower waterfall display shows the signal strength for each frequency plotted downward as time progresses. The time in minutes and seconds is shown at the left edge of the waterfall display. As explained in the text, brighter colors on the waterfall represent stronger signals.

The station at about 250 Hz is the DX station. He has asked stations calling him to operate at higher frequencies. The multiplicity of stations desiring a QSO and responding to the request are to the right at offsets up to at least 2400 Hz.

The bandwidth occupied by each station is mainly set by the rise and fall waveforms of the CW keying (key clicks) as was discussed for the 18-MHz transceiver.

- If transmit functions are to be used, an audio cable and possibly level adjustment circuitry is needed between the EZKIT output and the transceiver microphone jack.
- If a parallel port is available there are optional T/R controls from PC program. These come from the parallel port as TTL levels and usually need some level conversion.

With these minor adaptations the audio processor is compatible with most of the other projects in this book.

Fig 11.34 shows the audio processor screen with a CW DX pileup. This is interesting to observe, but there was no magic as far as copying the stations! However, there is utility in using this type of spectral display for choosing a frequency on which to operate.

Extensions

The features of the DSP-10 and the associated audio processor happen to be associated with weak-signal communications. Since all of the source files are available, it can be a good place to begin a project for very different uses. This might be a data communications mode, a propagation monitor or a radio astronomy project. Or it might be some only slightly related area such as ornithology research. It is often easier to modify a software project that is working than to bring up a new one from an "empty file." Either way, though, the software approach allows a different kind of flexibility than can be achieved in hardware modification. The opportunities for exploration are endless!

REFERENCES AND NOTES

1. D. D. Rasmussen, "A Tuning Control for Digital Frequency Synthesizers," *QST*, Jun, 1974, pp 29-32. This article on the inner workings of the rotary optical encoder has all of the information needed to construct an encoder instead of purchasing a manufactured version.
2. There are many registers that control functions or select options. Those that are selected through data memory mapped locations must not also be used for other data storage. More information on these registers is available from "EZ-KIT Lite Reference Manual," Analog Devices that is supplied as part of the EZ-KIT.
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5. W. Hayward, "Measuring and Compensating Oscillator Drift," *QST*, Dec, 1993, pp 37-41.
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8. An excellent discussion of the general characteristics of EME communications is Chapter 10, "Earth-Moon-Earth (EME) Communications" by D. Turin and A. Katz, from the book *The ARRL UHF/Microwave Manual, Antennas, Components and Design*, ARRL, 1990.
9. J. Forrer, "A DSP-Based Audio Signal Processor," *QEX*, Sep, 1996. This article provides background information on several of the basic routines as well as a set of routines that can be run on the EZ-Kit Lite. This material is contained on the book CD.

Field Operation, Portable Gear and Integrated Stations

This book is perhaps more personal than its predecessor with the individual chapters written by easily identifiable individuals. But there is also a strong common thread of interests among us: we all enjoy a wide sampling of frequency bands, ranging from VLF through microwaves; we all have equipment that we have built that we take to unusual locations, ranging from the hills of Michigan's Northern Peninsula to

the mountains of the Pacific West to the coastal waters of Oregon; We all operate stations from home, with virtually all of that operation using, or relating to equipment we have built; Although QRP is a frequent pursuit, we all use higher power at times, and we all integrate experimental activity with station operation.

This chapter illustrates some of that activity, both from the field and at home. A vari-

ety of rigs are described, showing one or more of our interests. The equipment is presented not for exact duplication, but mainly as encouragement for other experimenters. None of the equipment we have built will include the features that another designer/builder will want. But, the tools of the other chapters can be evoked for the design of whatever you might need.

12.1 SIMPLE EQUIPMENT FOR PORTABLE OPERATION

A longtime favorite activity at W7ZOI has been portable operation, predominantly from the mountains of the western United States. Many of our mountain rigs are simple (non-phasing) direct conversion CW designs. While not optimum for contests (such as Field Day), they are otherwise adequate. These are the rigs that are thrown into the pack when we just want to make a few enjoyable backcountry contacts. They also provide a link to the outside world when we hike alone. The several rigs described here are not presented for exact duplication, but as a source of ideas for the designer/builder.

Batteries and Power Sources

A wide variety of batteries offer portable power for the experimenter. Rechargeable Nickel-Cadmium (NiCd) or Nickel Metal Hydride (NiMH) batteries are ideal for radio applications, for they are capable of high current output, reasonable total capacity, and are easily charged. They also feature rather stable output voltage.

In spite of these virtues, the ubiquitous alkaline flashlight cell remains the most popular energy source. The reason is simple: the total energy per pound contained is far in excess of that available from popular rechargeable cells. A 1.2-V NiCd AA cell has a typical capacity of 500 mA-hours with the ability to be recharged for up to 1000 cycles. An alkaline cell, used only once, weighs about the same amount with a rated capacity of 2800 mA-Hours. The cell voltage can vary from 1.5 V at the beginning of use to 0.8 V for complete discharge. Data is available on the Web at data.energizer.com/ and www.duracell.com/OEM/Primary/Alkaline/. Some emerging but more expensive battery technologies are also of interest.

The experimenter may wish to measure battery performance. Single cell testing is adequate, but the test should emulate the expected duty cycle, for total energy available from batteries may depend upon the way it is extracted. Accordingly, we graphically examined a typical CW transmission. A dash length is three times that of a dot while a space following either is one dot length. The pause after a letter is

three dot lengths while the pause after a word is five. Our sample "transmission" then produced a duty cycle of just over 50%. A similar receiving period accompanies this during a contact, reducing operation to a 25% key down duty cycle. Most of us spend at least as much time listening as we do making contacts. So, we estimated a typical key down use as being $\frac{1}{8}$, or 12.5%, increasing to 25% during contests.

A circuit that will test batteries with a 12.5% duty cycle is shown in Fig 12.1. A 7555 timer IC oscillating at an audio rate is divided with a chain of 14 divide-by-2 elements within a 74HC4060 IC. Q13 and Q14 outputs are decoded to produce a 25% duty cycle. These are then combined with the Q6 output to create a "string of dits" with net duty cycle of 12.5%. A 74HC138 one-of-eight decoder extracts the keying signal, which then controls a power MOSFET switch.

Resistance RRX sets the load during receive periods with RTX switched in during "key down" intervals. A 1- Ω MOSFET on-resistance is part of the transmit load. The resistor values can be changed to accommodate other conditions

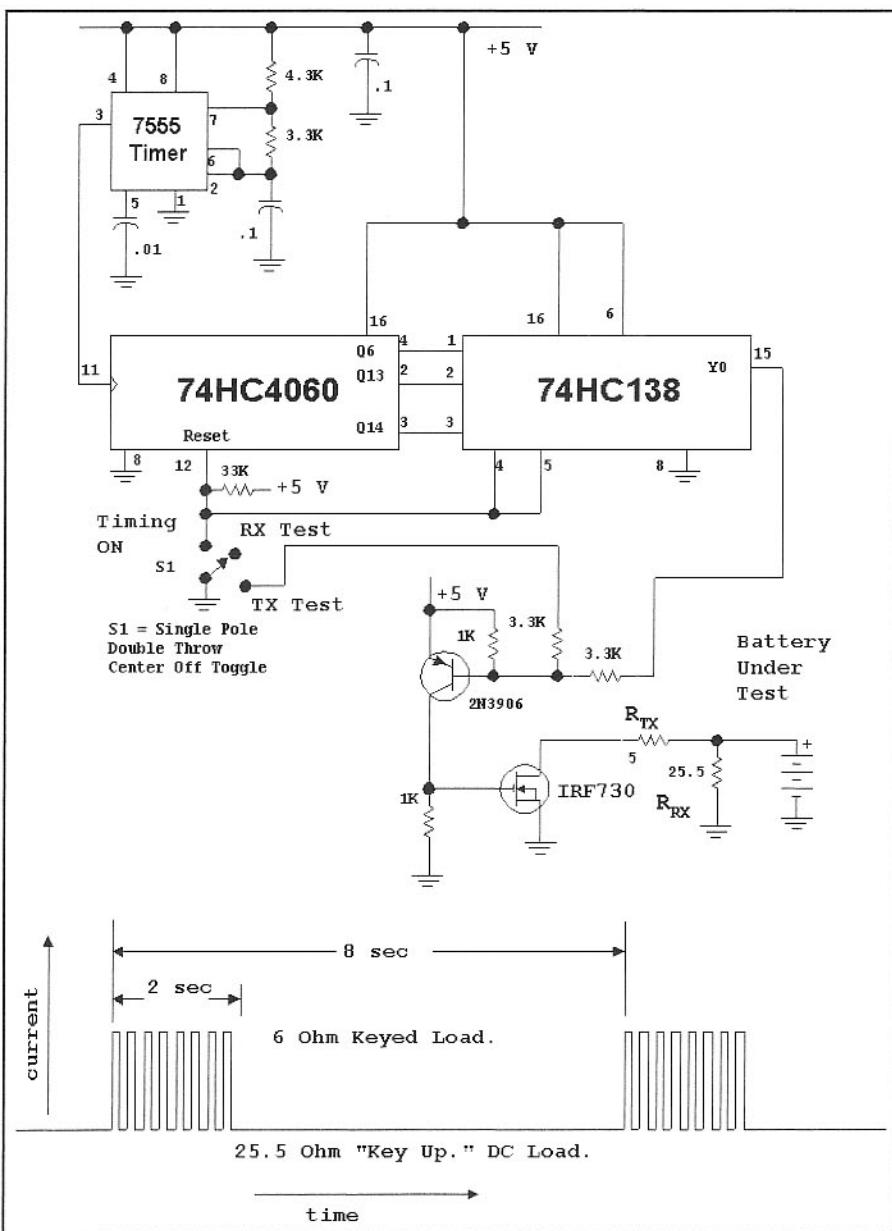


Fig 12.1—Timing circuit for testing a single cell battery at 50-mA receive and 300-mA TX current. RTX and RRX will change with a different transceiver.

or batteries. While the scheme is certainly not a standard, it approximates actual use with a repeatable experiment. This scheme tests the battery with a pulsed constant resistance load. The manufacturers also show battery behavior with constant current. Switch S1 allows the circuit to be switched off to read the receive voltage or toggled to a "key down" mode to measure transmit current. Manual measurements are done with a DVM.

Fig 12.2 is typical of the data we obtained, based upon the load presented by the "Western Mountaineer" transceiver described later. There was about a 0.1-V difference between R and T loading over

the entire battery life. This is the result of internal battery resistance of about $0.33\ \Omega$. The perturbation at 360 minutes showed the result when the test was terminated in the evening, but restarted the next morning.

The battery life exceeds 1000 minutes for an AA cell for a key down voltage of 1.1 at "end of life." This constrains our equipment design if we wish to obtain maximum battery life. The AA cell is probably suitable for higher transmit current, limited by internal resistance.

We have modified one transceiver (below) to include a voltage measurement circuit and use a battery pack that can be

switched between 8 and 10 cells. Clearly, there are numerous opportunities available for the experimenter.

Portable Antennas

Choosing a backcountry antenna presents interesting problems. The stay-at-home radio amateur generates numerous exciting ideas when first considering field operation. Thoughts of exotic beams hanging between the trees or other available structures are common. But these grand plans often change after the first trip when the complications of getting lines into available trees are encountered. Also, the impact of long runs of coaxial cable is greater when they must be carried over a few miles of trail.

Our main antenna is an inverted-V dipole. The inverted form is preferred over a flat dipole because only one support is needed. We usually carry three 50-ft pieces of $\frac{1}{8}$ inch nylon cord. Two pieces are tied together and attached to a rock that is launched into a tree. This line supports the dipole center and the feedline. Once in the tree, only one line is needed to support the center. The remaining two pieces then support the dipole ends. If suitable rocks are not found, a cloth bag filled with smaller rocks, sand, or even snow can be used.¹ Some back-country radio amateurs will tie antenna ends to a cord that is then tied to a rock. The rock is flung into the tree where it remains suspended during operation. This is a poor practice if there is the slightest chance that the knot will become undone in the wind and drop the rock on a passing hiker!

Dipole center insulators are easily fabricated from hardware store plastic water pipe fittings. Plastic insulated wire is usually used for portable antennas, with the ends secured with nylon cord or rope, so end insulators are never needed.

The height of a dipole impacts performance. More often than not, we are satisfied with an antenna that is only 25 or 30 feet above ground, high enough for effective daylight 7-MHz operation. A higher antenna will do as well during the day, and will develop the low angle radiation needed for longer distance nighttime operation. But it will also require that more rope and feedline be packed up the trail. A simple transmatch (shown later) is usually used, even with dipoles.

End fed wire antennas are especially useful in the field, featuring a complete lack of feedline. A halfwave wire (67 feet at 7 MHz) is easily hauled into a tree with a single line. The polarization is usually a mixture of vertical and horizontal. The wire end near camp is fixed in place with

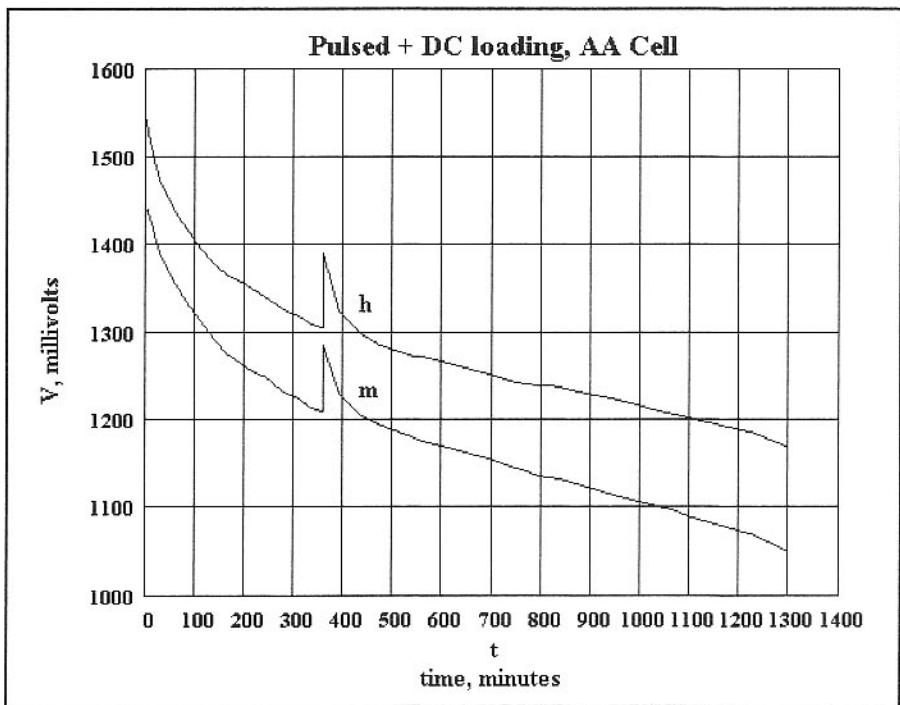
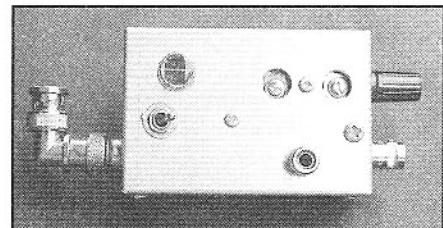
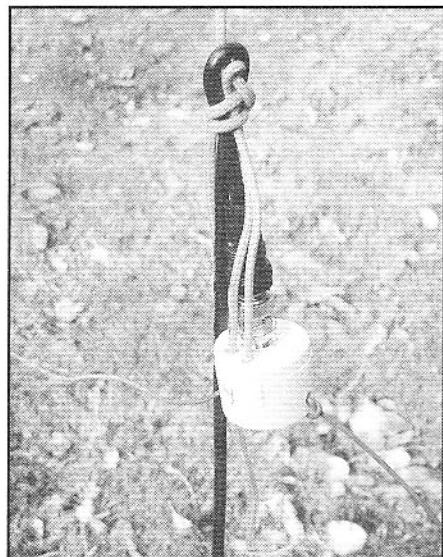


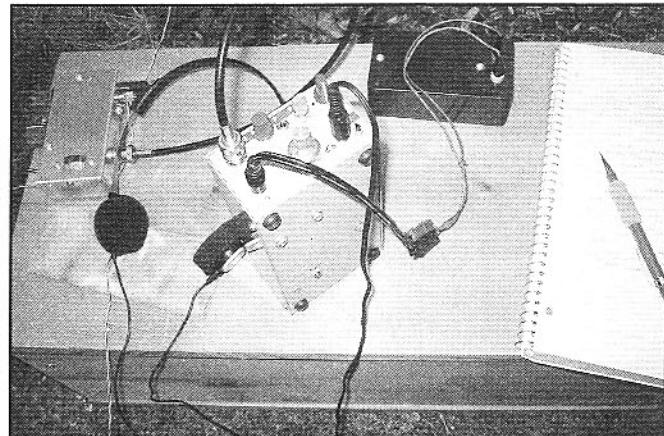
Fig 12.2—Battery voltage during pulsed testing for a single AA cell. See text for conditions.



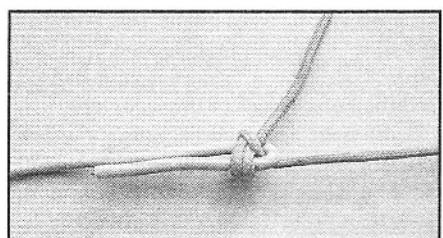
Portable transmatch using screwdriver adjustments.



Center of inverted-V dipole. The rope supports both the antenna and the transmission line.



Back yard experiments should include some listening to be sure the antenna is really functioning.



The end of a portable antenna requires no insulator. A tie-off cord or rope with the insulation on the wire is sufficient.

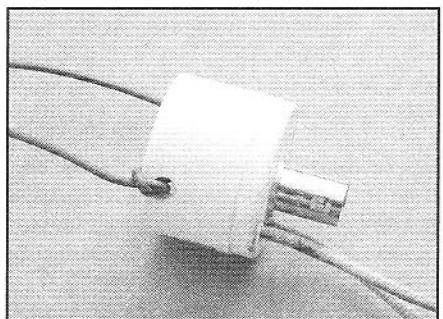
a short piece of rope and fed with a transmatch. One or two quarter wavelength pieces of wire are laid on the ground to form a reference for the transmatch. A transmatch that differs from that used with dipoles is usually required, for typical Z is around 3000Ω . Measurements on back yard systems show that while an end fed wire without a reference radial or two can sometimes function, the match is then susceptible to hand capacitance effects. These problems disappear with even one radial. Slip the radials into the brush where they won't be under foot.

An end-fed full wavelength wire also enjoys a lack of feedline, and can be configured to generate a dominant horizon-

tally polarized signal with lower angle components. The full wave wire can also be configured as a loop.

An antenna support is a problem when operating above timberline. We have carried a 12-foot telescoping whip (14 inches collapsed) to support a dipole. The whip base is lashed to a rock, ice ax, or ski pole. Fishing poles of various sorts are popular among QRP enthusiasts, some coming in lengths of 20 ft or more. Sometimes no support at all is needed; a dipole on snow or dry rocks can still function, although experimentation is required.

VHF antennas present a different challenge. Our standard portable mast uses 0.625-OD aluminum tubing in the form of



A dipole insulator is fabricated from an end cap of PVC pipe. This cap is 1.25-inch OD.

two 5-foot tent poles, each in three sections. A ten-foot length is formed with a connecting piece of 0.75-inch OD tubing. A slip ring provides a guy point at the 5-foot level. The usual antennas used at 144 and 432 MHz are coax fed Yagis.²

Bands and Modes

The dominant band we use in the mountains remains 7-MHz CW. Other operators have different preferences. A good friend and hiking companion, WA7MLH, has done a great deal of winter camping from snowshoes or skis. Jeff has found both 80-meter CW and 75-meter SSB to be effective. Unfortunately, 80-meter CW often lacks people with whom to converse. The higher bands can be great fun when working other QRP stations. The antennas are usually a bit easier at 14 MHz and above. Simplicity remains the best guideline. Some simple beams are useful for Field Day and other committed radio events, but are not recommended for routine backpacking where the radio gear is a secondary goal.

The Trail-Friendly Radio

The term "Trail Friendly Radio," or TFR was introduced in 1996 by members of the "Adventure Radio Society (ARS)," an informal group of QRP enthusiasts who regularly take radio gear beyond the limits of motorized travel.³ A TFR need not look like the usual home bound transceivers that must sit on tables or shelves. Some of the following equipment is in the TFR category. Also see the "Sleeping Bag Radio" described elsewhere in this chapter.

Equipment for backpacking or other field use should be lightweight, compact, and should be easy to operate. A minimum of controls is desirable, and they should be capable of use even when the operator wears gloves or mittens. Temperature testing prior to use is vital.

The Adventure Radio Society sponsors an informal, monthly contest called the "Spartan Sprint" that emphasizes these ideals. The scoring for this contest is essentially the number of contacts divided by the total station weight, including key, headphones, and batteries. It is common to encounter several stations in the contest with total station weight under a pound, with some around 0.1 pound! This is realized only with meticulous attention to details such as small circuit boards with less than normal thickness, screwdriver tuning (with very light-weight tools), rigs without cabinets, Lithium batteries, and absolute minimum power. While most "winners" are operating from a home

environment, some are taking this minimalist equipment into the field. More is to be found on the ARS Web site.

Alternative Power

Many of the folks participating in QRP and in backpacking radio are also intrigued with alternative energy. The most common form is solar power, although the present "wind-up" broadcast receivers suggest many mechanical sources, including wind and waterpower.

Some simple circuits for use with solar panels are shown in Fig 12.3. With some solar cells and rechargeable batteries, it is

permissible to merely connect the panel to the battery, perhaps with a diode to prevent leakage into the panel. The current from the panel should be less than the maximum allowed charging current for the battery. Current is confined with a series current limiter, shown in Fig 12.3A. With the components shown, current is limited at either 50 or 130 mA from the charger. This circuit should not be used without a rechargeable battery, for that would allow voltages greater than 15 to be applied to the transceiver. Figure 12.3B uses a shunt regulator with current limiting to either charge a battery or to supply a voltage regulated output. The latter occurs when

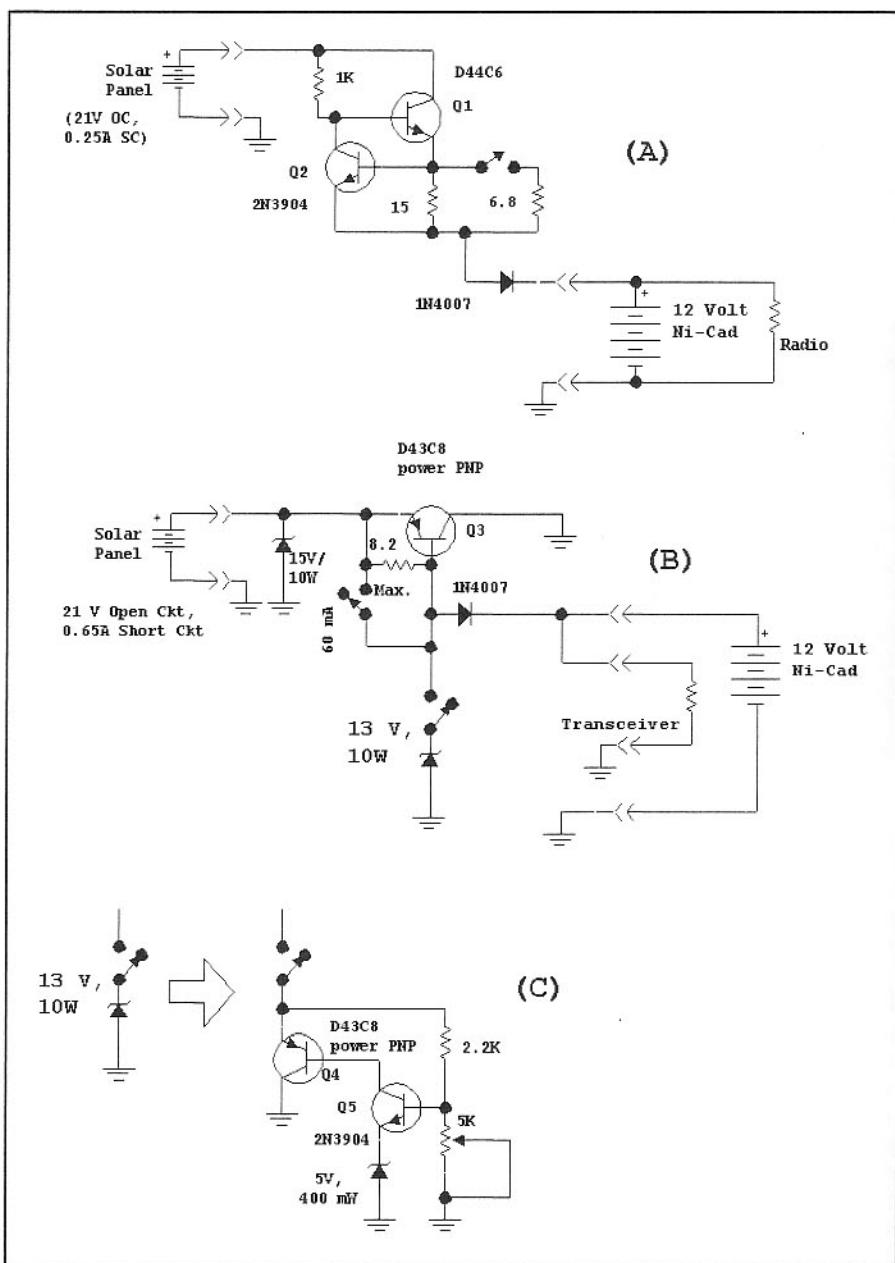
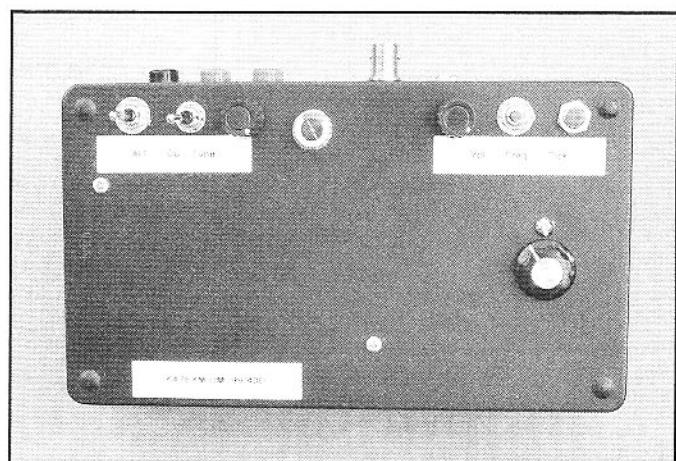


Fig 12.3—Some circuits for handling solar panels. See text for discussion. A TIP-32 may be used for the power PNP, replacing the D43C8.



A solar panel provides energy to keep batteries "topped off" during a 1993 Field Day operation. The operator is sitting in the tent to escape a light rain.



Front panel of Portable CW transceiver. The station weight, including batteries, earphones, keyer paddle, transmatch, and an end fed antenna, is about 2 pounds. The transceiver includes a bridge and VSWR indicating meter, so the transmatch consists of nothing more than the matching network.

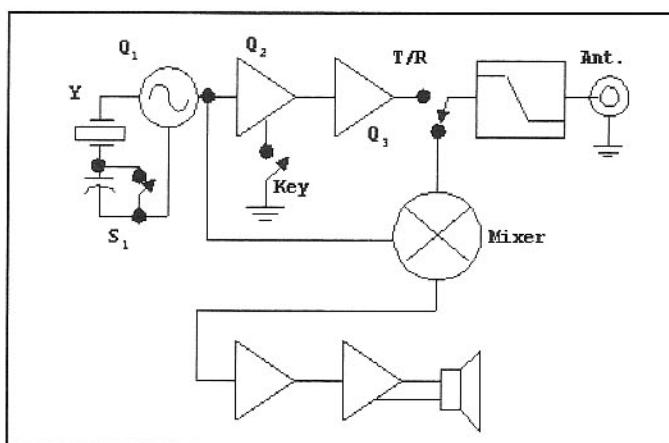


Fig 12.4—Block diagram for a simple direct conversion transceiver. A single crystal oscillator serves a dual function.

the 13-V Zener diode is switched into the circuit and is useful when making contacts with the solar panel being the only energy source. The 15-V Zener diode protects the transceiver against excessive voltage. Q3 can dissipate the full energy capability of the panel, so a heat sink should be used. Solar panels are capable of short circuit operation without damage. Power Zener diodes are expensive and are best replaced with the adjustable shunt regulator circuit shown in Fig 12.3C with Q4 also attached to a heat sink. The designer/builder should investigate modern battery management integrated circuits from Maxim and other vendors.

Micro-Mountaineer-Class Transceivers

A simple transceiver can be built with a single crystal controlled oscillator serving a dual function: The oscillator is the frequency control for a simple two or three stage transmitter; the oscillator is also the

LO for a direct conversion receiver. A block diagram is shown in **Fig 12.4**.

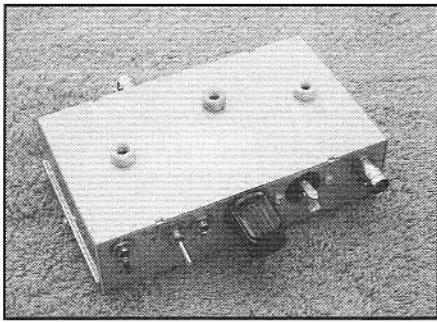
This transceiver topology is the result of current operating practices where operators calling CQ will rarely look for an answer more than a kHz away from their transmitter frequency. With such a practice, there is little value in receiving on frequencies other than those where your transmitter can function.

Some sort of offset capability is required for the crystal oscillator in such a transceiver, needed to produce a beat note that can be heard when a station is zero beat with your transmitter. This can be an inductor or capacitor in series with the crystal. The extra element can be switched in or out automatically with the keying, or can be manually activated by the operator. These differences are all details that the experimenters can individually implement.

A simple Micromountaineer transceiver results from combining the "Beginner's Transmitter" of Chapter 1 with the Micro-R1 basic direct conversion receiver of Chapter 8. The sidetone oscillator and transmit-receive switch included with the transmitter complete the station.

A contemporary version of the Micro-mountaineer was presented in *QST* for July, 2000 with the article included on the book CD. That version featured 2N3904 transistors throughout the RF portion of the design with a NE602-LM386 combination as the receiver. (See the beginner's receiver in Chapter 1.) MOSFET switches are used in the T/R system for a rig that can be built for any band from 1.8 to 50 MHz. The 28-MHz version has been used for contacts all over North America and Japan.

The July 2000 version lends itself well



A Micromountaineer class transceiver uses internal crystals, but accepts an external VFO.

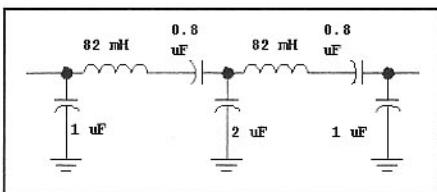


Fig 12.5—An audio bandpass filter for use with the *QST* July 2000 Micromountaineer.

to modifications. **Fig 12.5** shows a passive LC audio filter that can be added in the headphone lead to substantially improve selectivity. Ed Kessler, AA3SJ, built this circuit.

A variable frequency oscillator is easily added to Micromountaineer class portable rigs. **Fig 12.6** shows one that was added to the *QST* July 2000 version built by Roger Hayward, KA7EXM. The VFO operates at the 7-MHz output frequency, so it is vital that the oscillator be shielded from the rest of the circuitry. If the oscillator frequency was reduced to 3.5 MHz and was followed by a frequency doubler, no shielding would be needed. This transceiver is shown in the photographs. **Fig 12.7** shows the modifications used within the transceiver. The previously tuned output at Q2 was replaced with a ferrite transformer. The VFO signal is then injected at the base of that stage. The gain is set with the addition of Q2 emitter components while a dc signal from the AIT switch is routed to the feed-through capacitor feeding the 1N4152 diode. The capacitor marked "sel" in the VFO may be selected to set the offset with the value shown producing about 800 Hz in the KA7EXM transceiver.

A 1-k Ω resistor is added to the transceiver to feed a sample of the oscillator signal to a frequency counter. KA7EXM used a Frequency Mite from Small Wonder Labs for this function. See the discussion of counters in Chapter 4. The interface from the main transceiver board to the

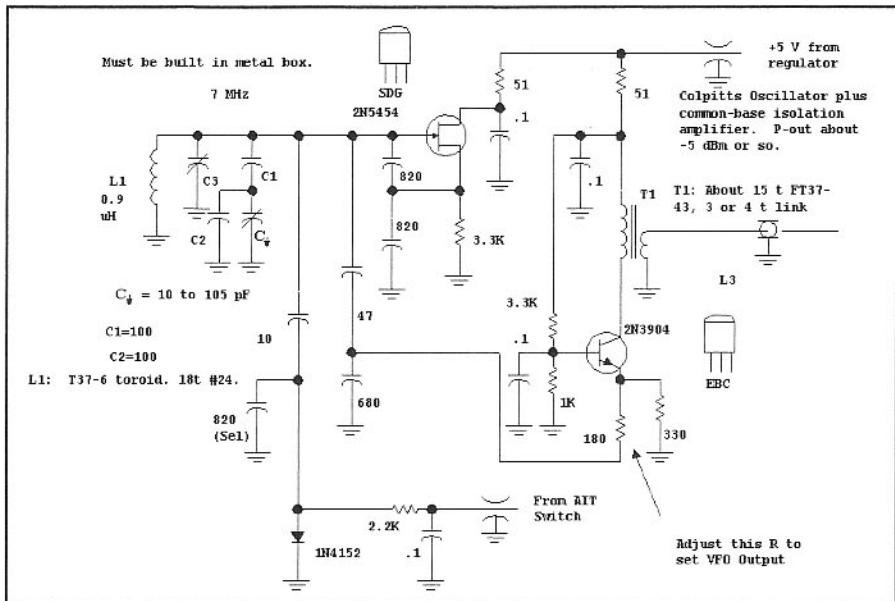


Fig 12.6—7-MHz VFO for use with the July 2000 *QST* transceiver.

counter should be coaxial cable or a twisted wire pair.

This transceiver also includes a built in electronic keyer. Both the keyer and frequency counter provide sidetone outputs that are routed to the audio system. The modification to the audio on the trans-

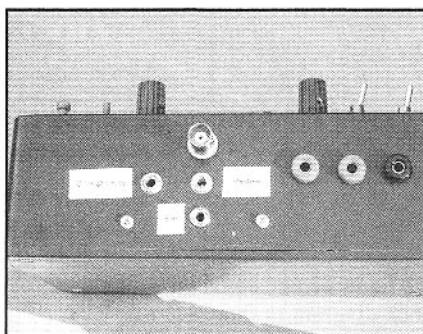
ceiver is shown in **Fig 12.8**. The user may wish to disable the sidetone oscillator included on the original *QST* design.

The KA7EXM version of the *QST* transceiver was built as a Trail Friendly Radio as described above. It was put in a plastic box (approximately 3 × 5 × 9 inches) with internal shielding of the VFO, shown in the photographs. Controls are on the larger surface with all interface attachments to one end. While this may not be optimum for a classic home station environment with table and chair, it worked well when used on backpacking trips in Oregon's Cascade Mountains.

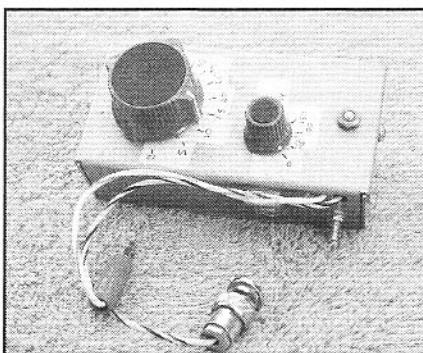
Earphones, rather than speakers, should always be used with portable transceivers. This is a courtesy to other back-country travelers.

There are clearly numerous modifications and variations that can be applied to this project with new bands being of special interest. Versions with the VFO operating at the output frequency would work well at 1.8, 3.5 and 10.1 MHz. Variations using a frequency doubler following the VFO would be preferred at 7 MHz and higher with a heterodyne VFO offering better performance at 21 MHz and higher.

A photograph shows a diode ring product detector based variation that we built and used in the mid 1980s time frame. Crystal control was included with a pair of internal crystals. However, an outboard VFO could also be attached when desired. Banana plugs and jacks provided a convenient mechanical interface. Coaxial cable provides a VFO output connection and a power supply interface between units. The offset control to the VFO was multiplexed



End view of the KA7EXM 7-MHz Micromountaineer.



The external "plug-on" VFO for use with the hand held rig.

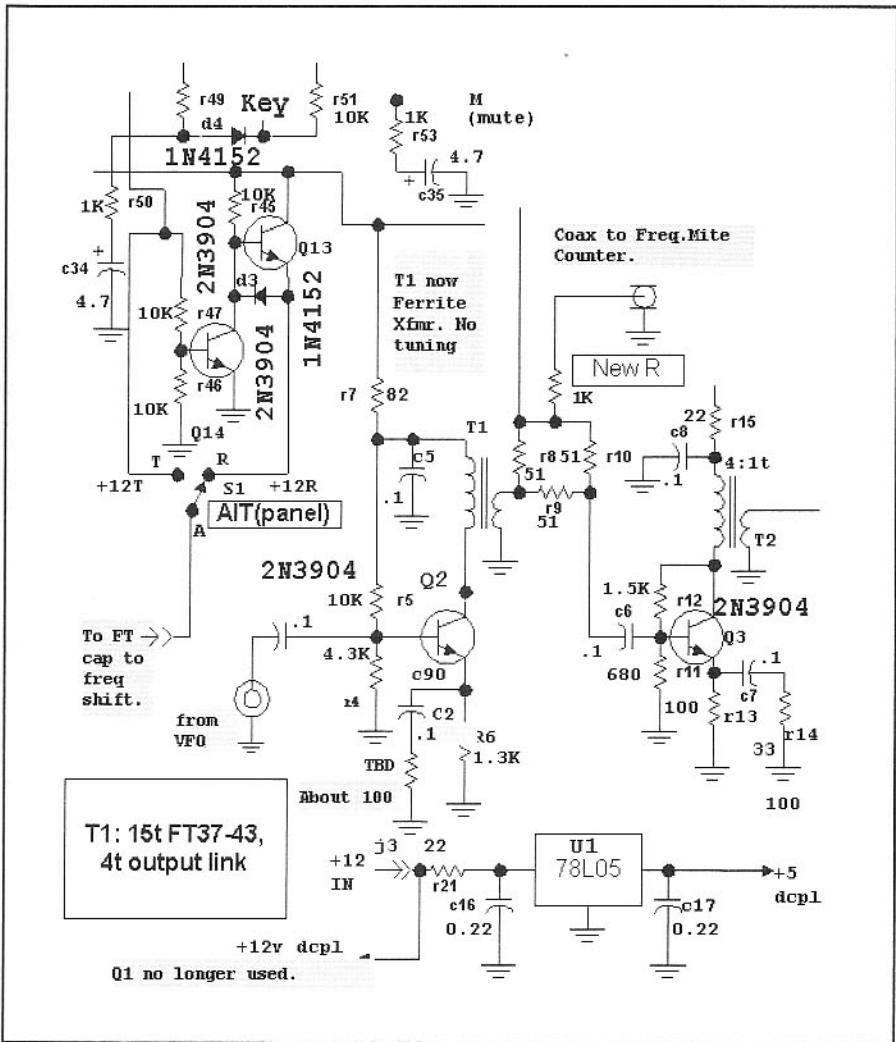
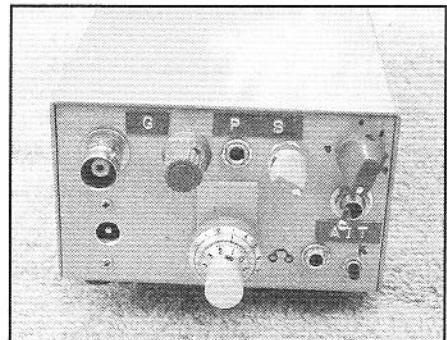


Fig 12.7—Modifications applied to the July 2000 *QST* transceiver when a VFO was added. See text.



All controls and I/O lines attach to the end of the "Western Mountaineer," allowing it to reside in a small camera case inside a pack. The turns counting dial is on a 10 turn pot to control a temperature compensated VCO. The knob in the upper right corner allows the supply voltage to be "measured."

with the RF line. This transceiver has seen nearly two decades of 40-meter CW use. The VFO is usually included, but is left at home or in a base camp during summit climbs where weight must be minimal.

The "Western Mountaineer"

This rig is a simple direct conversion transceiver based upon the popular Phillips NE-602 Gilbert Cell mixer. The name was chosen because the rig was designed for use in the mountains of the western USA where strong international broadcast signals are rarely a problem. Builders in the eastern USA or in Europe will find this circuit unsuitable and should consider a diode ring based design such as the still excellent W7EL transceiver.⁴

The VFO and transmitter, shown in Fig 12.9, begins with a high-C Colpitts oscillator tuned with a varactor diode, D2. This circuit is temperature compensated with two methods. Part of C2 consists of polystyrene elements with most capacitance built from NP0 parts. The tuning diode is then compensated with D1, a second silicon diode. This oscillator was discussed in Chapter 4. R1 is selected to determine the diode current. It is vital that a thermal chamber be used to adjust the temperature compensation. Details are presented in the book CD⁵ and in Chapters 4 and 7.

The VFO operates directly at the 7-MHz transmitter output frequency, making oscillator shielding vital. The shield was built from tin sheet stock. A wall was built around the part of the circuit board containing the oscillator and soldered directly to the ground foil. A lid was attached, leaving access to C1. Compensation diode D1

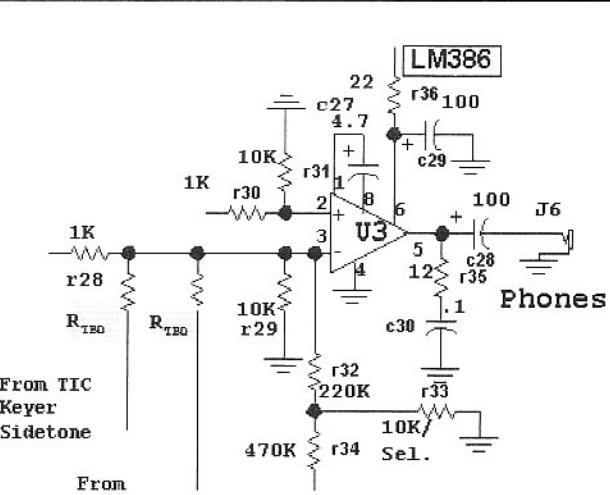
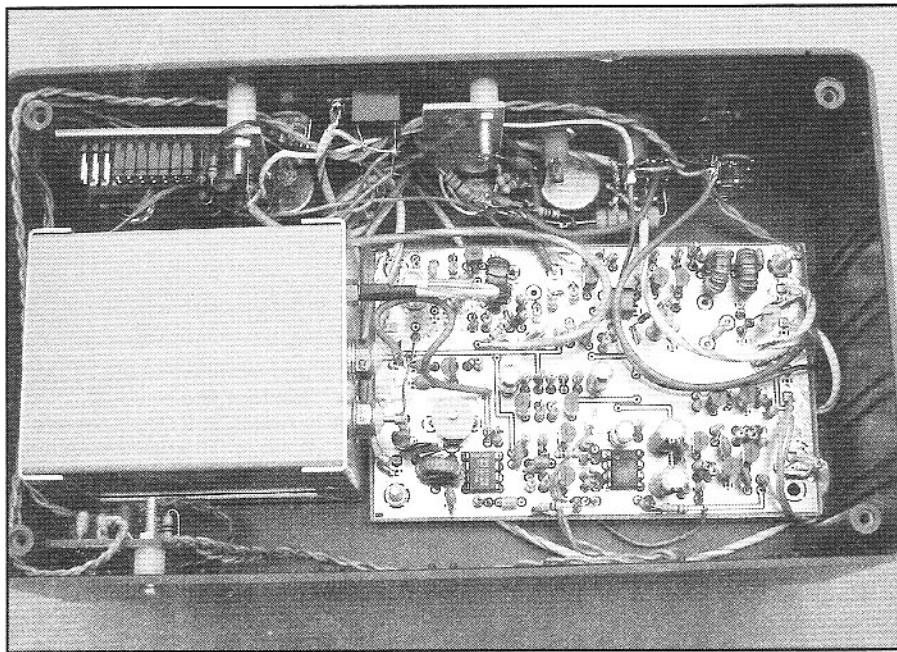


Fig 12.8—Sidetone signals from the counter and the keyer may be injected as shown. Removing R23 will disable the original sidetone from the output.



Interior of KA7EXM transceiver. The original plan called for internal batteries, but they didn't quite fit.

is enclosed in the same compartment.

The VFO is tuned with R2, a pot controlling a current pulled from the summing node of op-amp U3A. A CW offset of about 800 Hz is provided with Q13. This is configured for the Almost Incremental Tuning scheme outlined in Chapter 6. RIT could be implemented if desired; see Chapter 4.

The VFO output is buffered and amplified in several stages, eventually driving a power amplifier, Q5 and Q6, consisting of a pair of 2N3904 transistors with an output of 0.6 W. An output low pass filter provides impedance matching to the PA and harmonic attenuation.

The receiver, shown in Fig 12.10, begins with the NE-602 product detector, U2. The detector output is then dc coupled to U4, which then drives U6, an RC active peaked low pass filter. An interesting subtlety was discovered when this topology was first built: although the bias was as expected with about 4 V dc through the chain of U4 and U6, the voltage changed

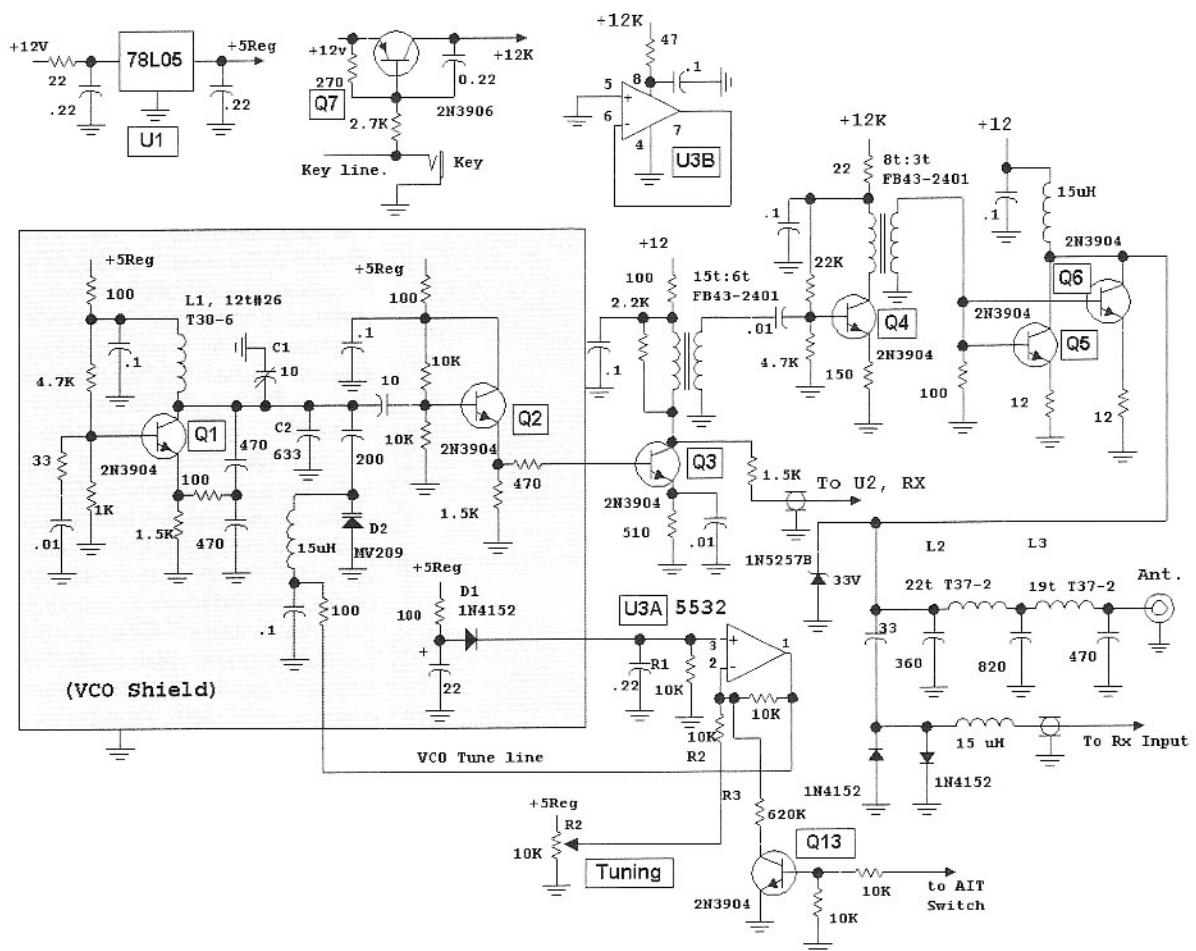
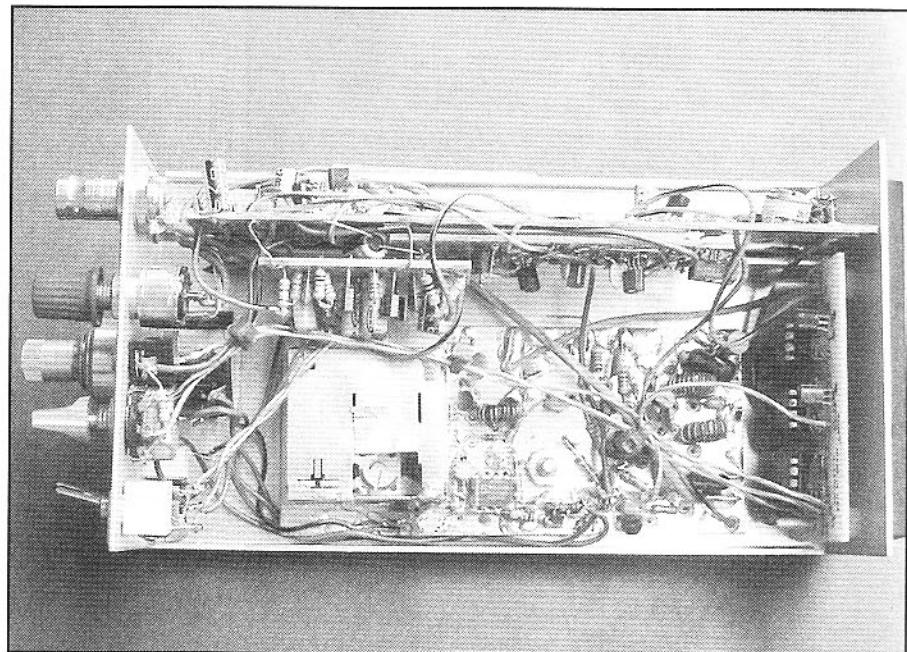


Fig 12.9—The VFO and transmitter portion of the "Western Mountaineer" direct conversion transceiver.

by several volts when the LO was attached to U2, pin 6. This was the result of unbalance in the input circuitry driving pins 1 and 2. Changing to a fully balanced topology at T1 eliminated the problem. If the circuit was duplicated today, we would use ac coupling between U2 and U4.

The receiver is muted with two FETs during transmit intervals. Q12 was usually adequate. Initially a pair of back-to-back diodes was used across U5A, but they distorted on loud signals. Complete muting was not possible after diode removal, so Q14 was added. Q12 could probably be eliminated.

The receiver schematic includes a voltage comparator using U7A. This circuit is driven by a front panel mounted potentiometer, R4. As R4 is varied, the voltage on the non-inverting input of U7A also changes. The reference voltage at the inverting input is merely the 5 V regulated supply. The output of U7A changes state when the two op-amp inputs are equal, which toggles the sidetone (Q9 and Q10)



Inside shot of the Western Mountaineer showing the VFO and transmitter, excluding voltage-measuring circuitry.

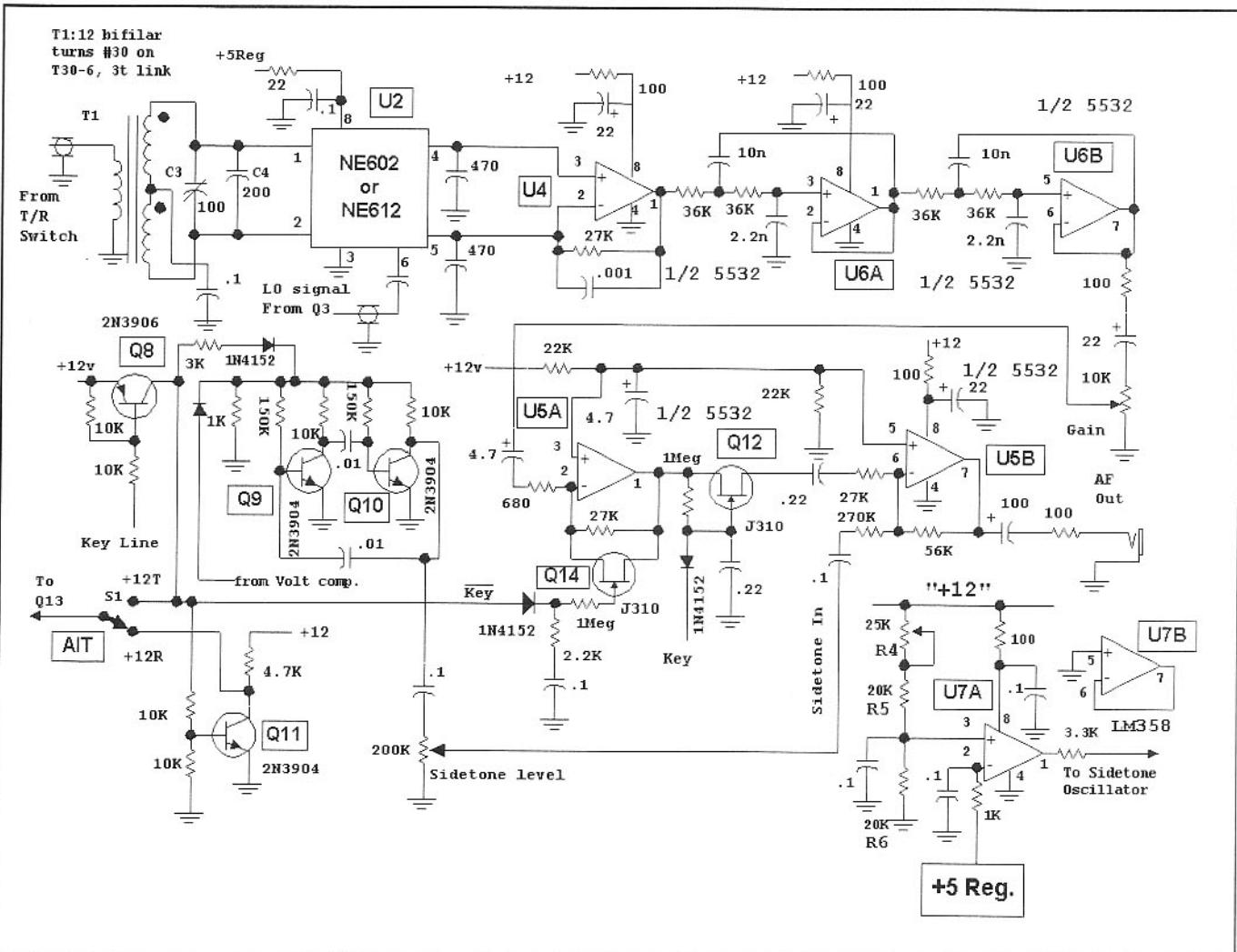
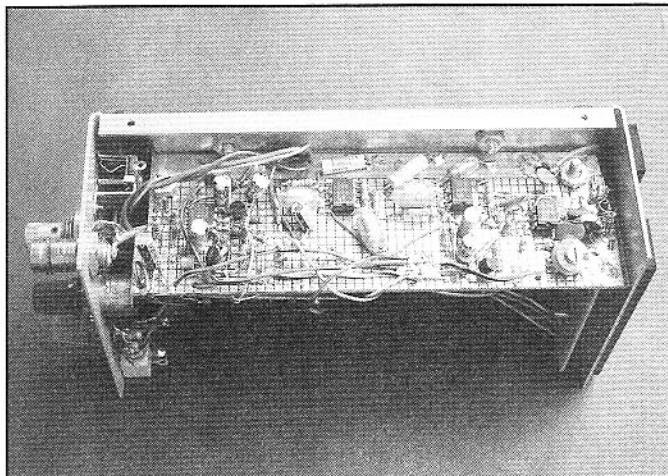


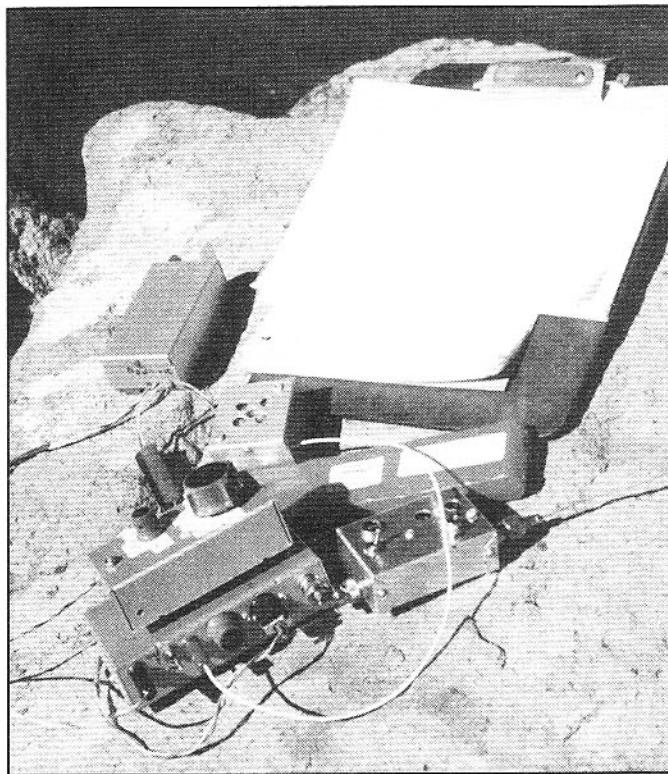
Fig 12.10—Receiver portion of the “Western Mountaineer” transceiver.



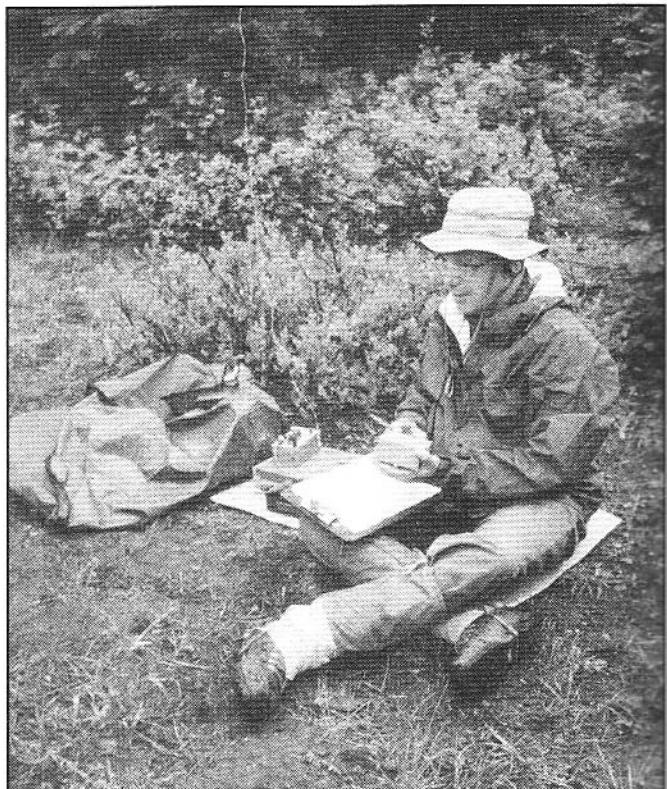
Inside shot of the Western Mountaineer showing the receiver board.



Shot of the Western Mountaineer installed in a protective case, including battery pack.



A Micromountaineer-Class transceiver in use for Field Day.
The rig is in use here on the 9500-foot summit of Oregon's Mt McLoughlin.



Here W7ZOI tries to get in just a few more Field Day contacts before the rain becomes more intense. KK7B photo.

oscillator on or off. This serves as a method for measuring the battery voltage without a voltmeter. R4 is a 25-k Ω pot, a small part that was on hand. The designer/builder may wish to use other values. The same results will be obtained if R5 and R6 are scaled with R4. The pot is normally set to rest in a position that inhibits its oscillation.

The transceiver was examined for output power and key down current consumption as supply voltage changed. This is

vital information for equipment that will operate from a power source that may change as it is consumed. The results are shown in Fig 12.11. The receive current is nearly constant at 50 mA for this transceiver, the result of having used a large number of 5532 op-amps. The designer/builder may wish to find substitutes that consume less power while still offering low noise. U4 and U6A should use fairly low noise parts while the rest of the op-amps are less critical.

The transceiver is breadboarded on PC board material containing a matrix of islands where components are mounted. The TX board had components on the ground foil side while the RX used a surface mount like scheme with standard leaded components. The rig has most input and output cables attached to the small end of a 2 × 3.5 × 6 inch box, shown in photos. This allows it to reside in a small camera bag that also includes a battery pack. The rig can even be operated from inside a down parka during winter

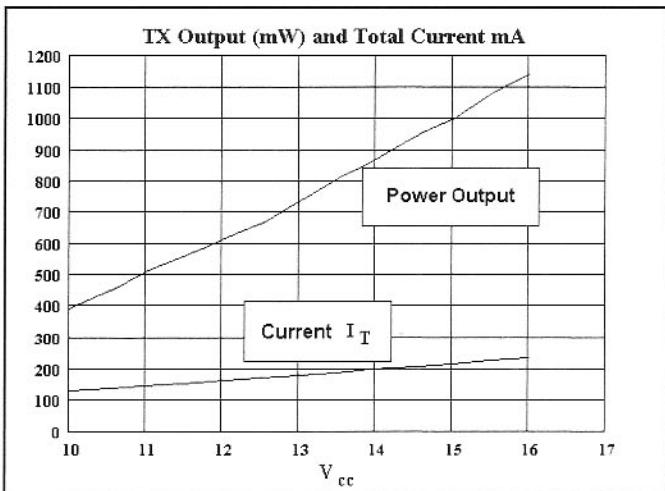


Fig 12.11—Power output and key down power consumption for the transceiver for voltages from 10 to 16 V.

excursions. A keyer is built into the rig.

A portable transmatch is shown in two forms in Fig 12.12. This circuit uses screwdriver adjusted trimmer capacitors. While less convenient than capacitors with knobs, the compact and lightweight features are useful for backpacking applications.

Single Signal Systems

While the work reported here uses direct conversion for portable rigs, there is certainly nothing to preclude the use of super-heterodyne equipment. The "Unfinished" transceiver described next has been used for a number of Field Day events, always with good performance. The ultimate portable rig might well be a single signal design (superhet or phasing) optimized for low current. An excellent beginning design is a transceiver described by Benson.⁶ This design has been extended in numerous kits built by QRP clubs world wide including the popular NorCal-40. Additional information is presented in the ARRL compendium, *QRP Power*, ARRL, 1996.⁷

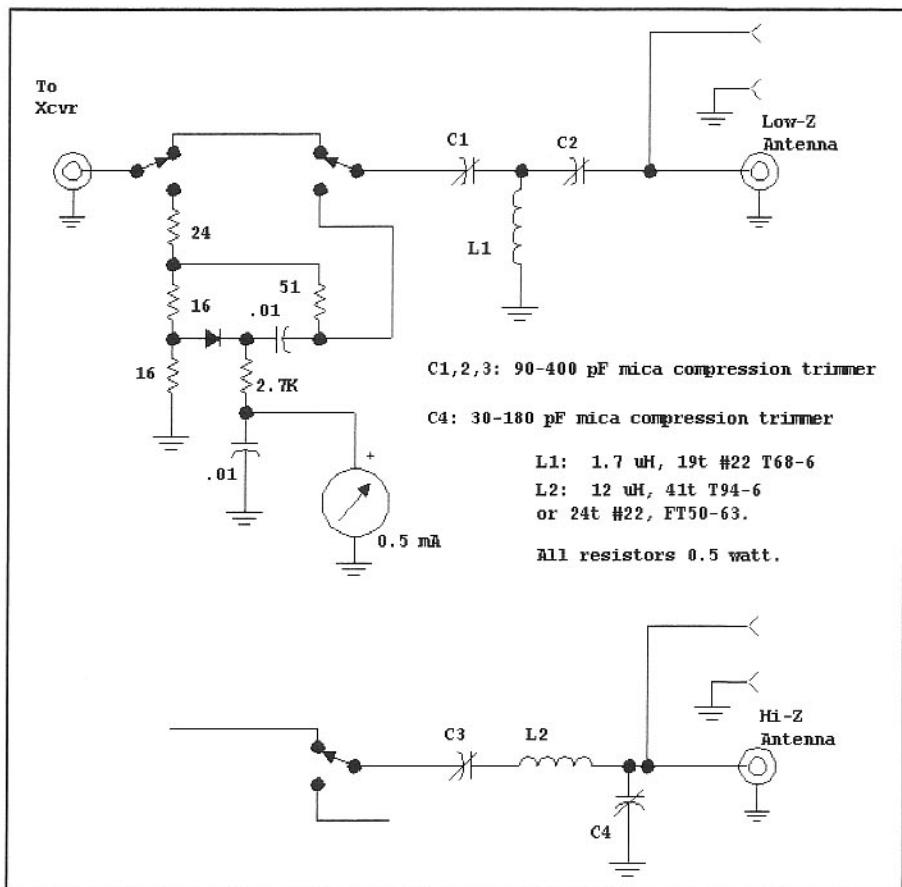


Fig 12.12—A small transmatch suitable for portable use. The bridge is switched into the signal path only when tuning. A small screwdriver is included for tuning. The upper circuit is suitable for coax lines while the lower one is intended for end fed wires. Component values are set for 7-MHz antennas.

12.2 THE “UNFINISHED,” A 7-MHz CW TRANSCEIVER

This transceiver (single conversion super-heterodyne, 5-MHz IF with 2-MHz LO) has earned the name “Unfinished,” for it is an ongoing effort that has been in a state of transition for over a decade. It has been a perpetual design platform to try new circuit ideas as they are generated. A homebrew crystal filter provides selectivity. This is intended here to be a source of ideas rather than a construction project.

Fig 12.13 shows the LO and RIT system, which tunes from 2 to 2.1 MHz, producing coverage of the bottom 100 kHz of the band. A JFET, Q7, serves as an oscillator with a bipolar buffer, Q6. Temperature was compensated with a polystyrene capacitor, adjusted with an experimental oven. (See Chapter 7) Q8 and a Zener diode provide a stable voltage for the system, although an IC regulator would serve as well. The output is low pass filtered and routed to a diode ring receiver mixer. A low power tap is extracted for use with an IC transmit mixer. A pair of varactor diodes are used as part of a RIT system.

The 2-MHz LO is built in an aluminum box, approximately $2 \times 2 \times 5.5$ inches. No lid is used, for isolation requirements are minimal.

The receiver front end is shown in **Fig 12.14**. A diode ring mixer, U1, is preselected with a double tuned circuit and followed by a bipolar post-mixer amplifier, Q1. A 2N5109 or equivalent is used, although a 2N3904 could also be applied. This transceiver is sometimes used for portable applications, so post-amp current is modest. A pad and a homebrew crystal filter follow the amplifier. The circuit shown here has a bandwidth of 250 Hz with 500Ω terminations. The filter is designed for a Gaussian-to-6 dB shape, which has minimal ringing, even with the narrow bandwidth. The rounded peak shape is selective enough to be extremely effective, yet the low number of crystals produces a response that maintains a receiver “brightness” rarely experienced with narrow, multi-resonator filters. Impedance match is carefully controlled at 500Ω around the crystal filter.

The Gaussian-to-6 dB filter shape is an especially good one for the experimenter, for it is very tolerant of changes in crystal characteristics or filter capacitors. Altering crystal motional L from the design value of 0.1 Henry by $\pm 30\%$, or dropping Q_U from 200,000 to 50,000 still produced useful filters.

The receiver has a noise figure of about 17 dB with an input intercept of around +15 dBm for a two-tone DR of 97 dB. High-level mixers and a higher current

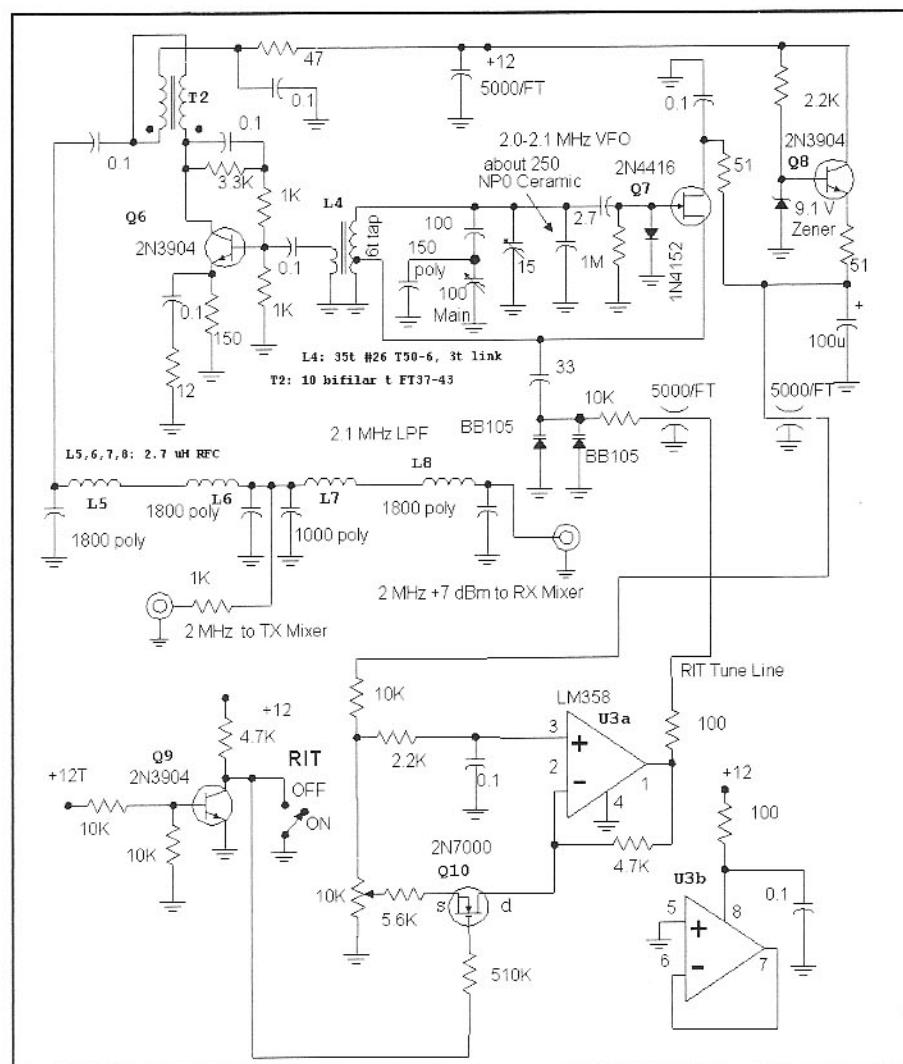
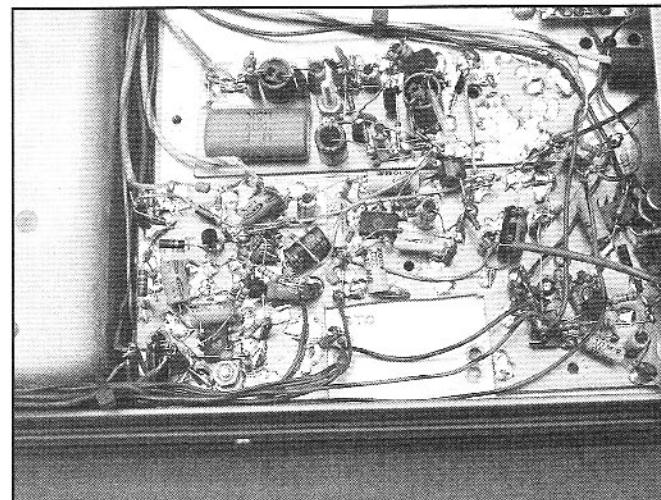


Fig 12.13—VFO and RIT for the Unfinished.



Audio circuitry for the “Unfinished-7” Transceiver. The rectangular cutout locates a crystal filter from an earlier version.

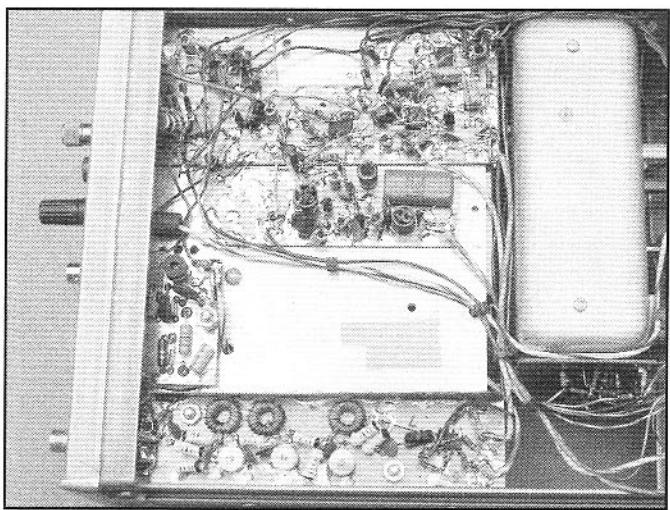
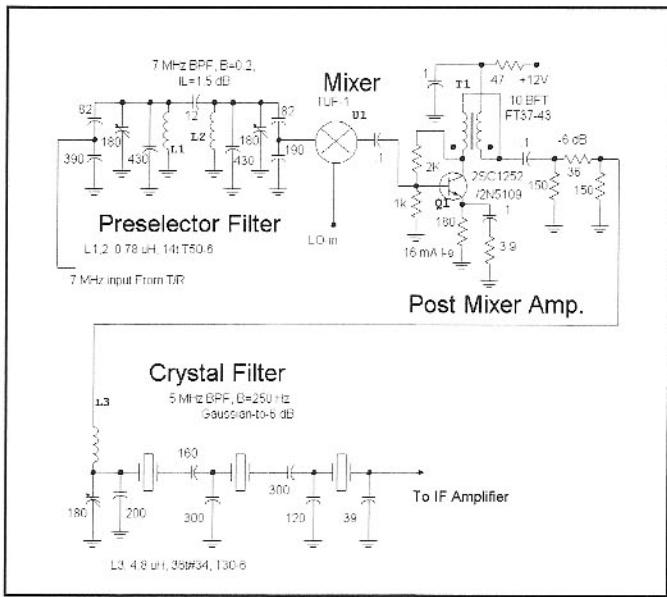


Fig 12.14—Receiver front end for the Unfinished. A Gaussian-to-6 dB shaped crystal filter is included. The double-tuned circuit is not symmetric, because an adjustment was made to compensate for interaction with the tuned circuit in the T/R system.

The bottom inside view of the "Unfinished-7" Transceiver. The upper circuitry includes audio, regulators, and sidetone. The board along the lower edge is the transmit mixer and triple tuned bandpass filter. The transmitter driver is the small board above the bandpass. The VFO module is at the right.

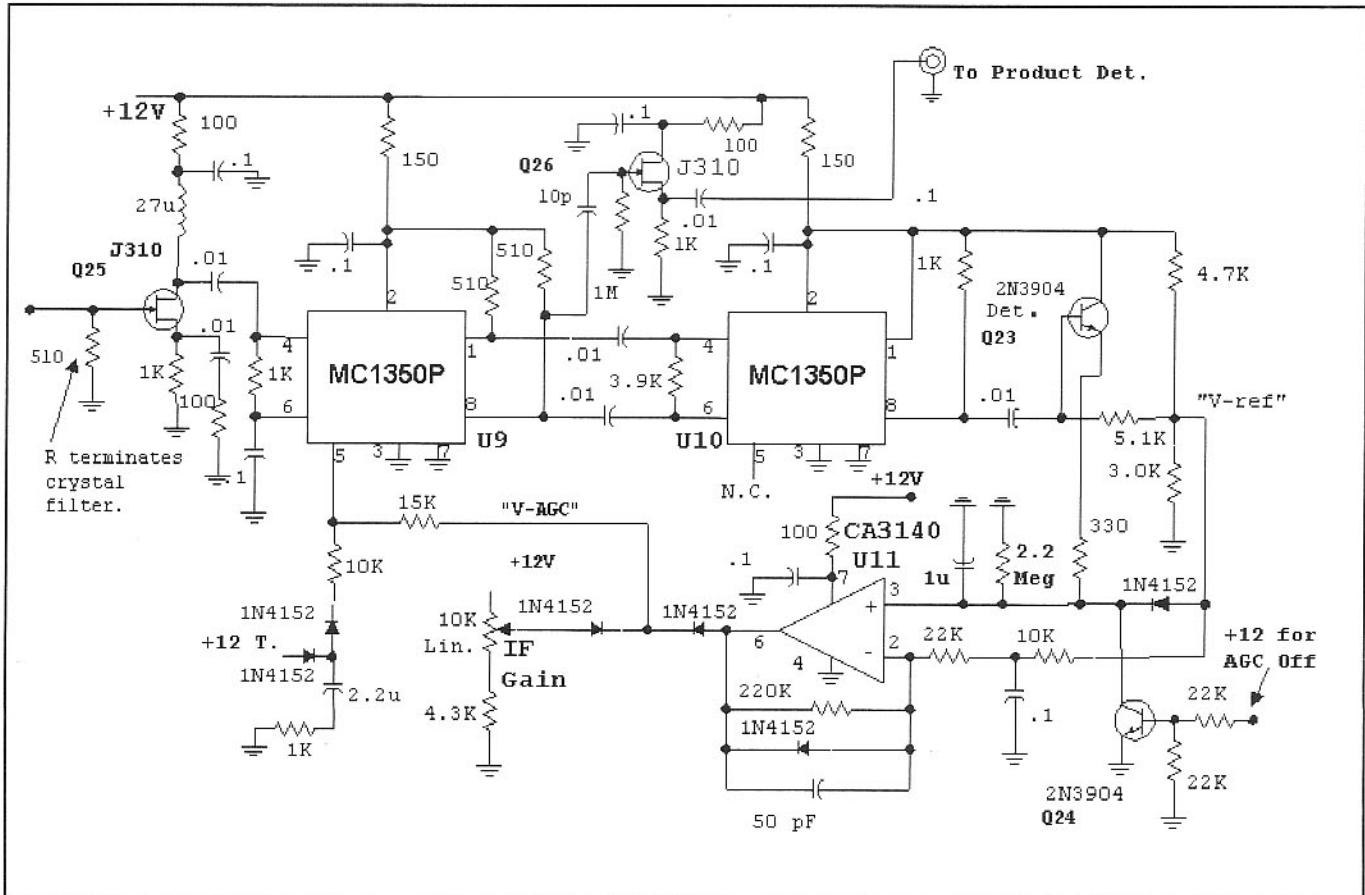


Fig 12.15—IF Amplifier. See text for details.

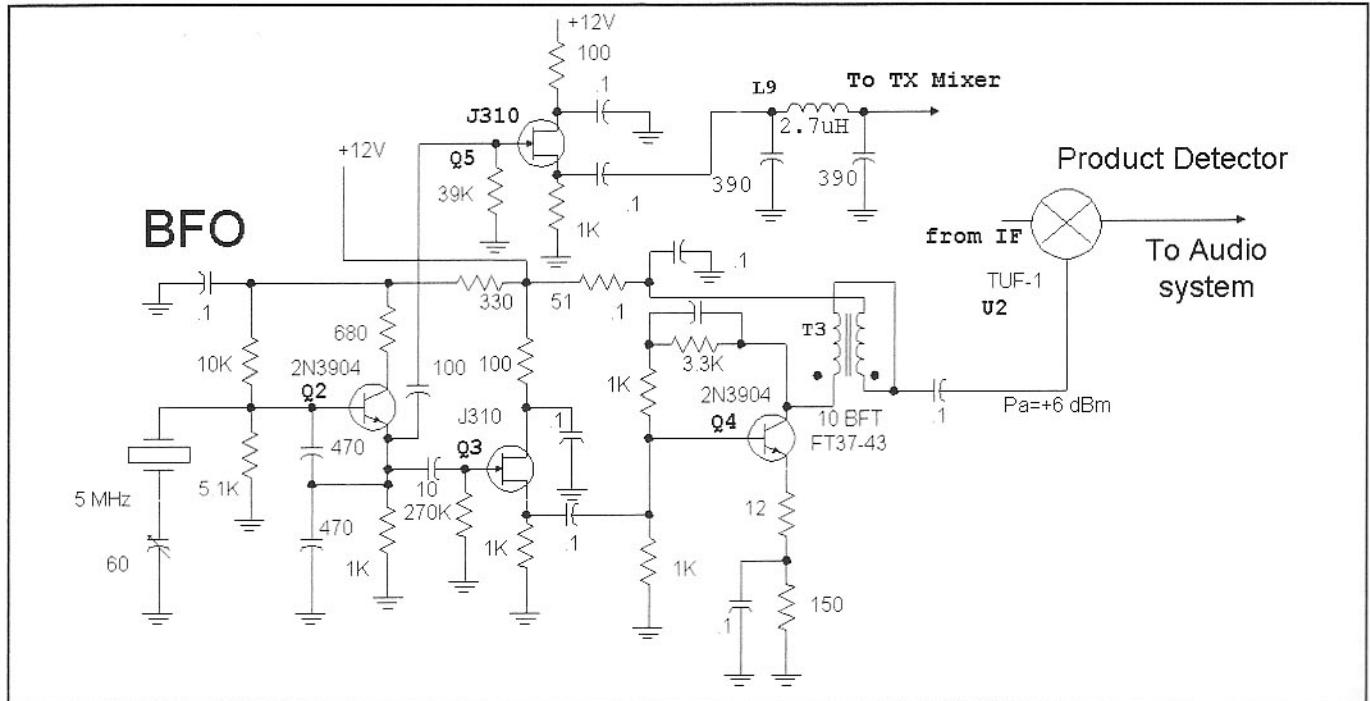
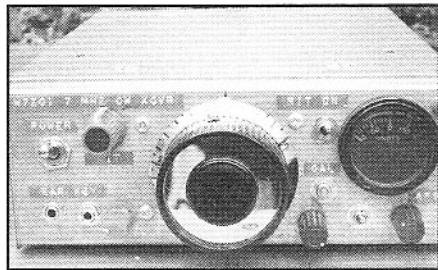


Fig 12.16—BFO and product detector for the Unfinished.



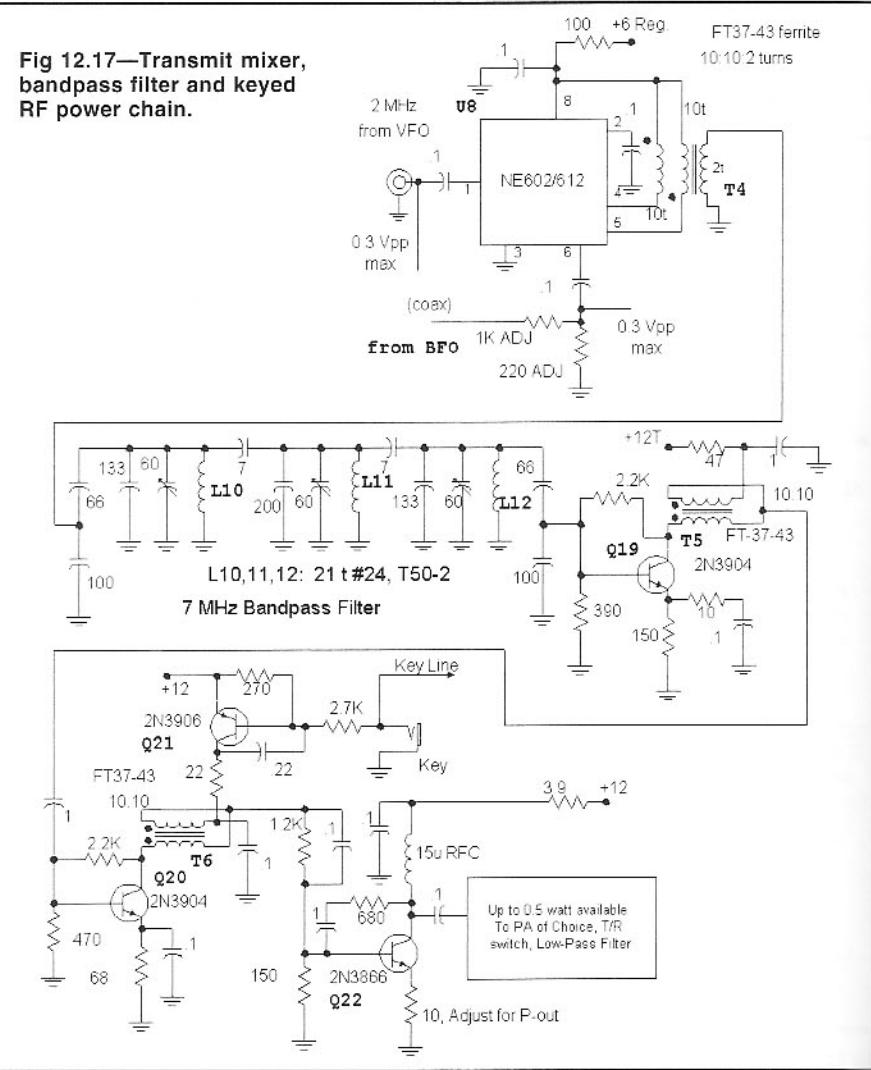
The “Unfinished-7” Transceiver front panel.

post mixer amplifier should easily extend this well past 100 dB.

The IF amplifier, shown in Fig 12.15, is effective, but is probably the weak point in the design. A lower noise IF would extend the overall receiver two-tone DR slightly, as discussed earlier in this chapter. This system uses a pair of MC1350P integrated circuits, but only one has AGC applied. The output of the second is detected with transistor Q23, producing a dc signal that is applied to op-amp U11 that feeds AGC signal to the first MC1350P. A JFET follower, Q26, provides output to the detector. A JFET follower, Q25, precedes the first MC1350. However, the impedance is only $500\ \Omega$, set by an input resistor. A higher impedance at this point would drop the IF noise figure. This AGC system is strictly an “ear-saver,” with a threshold set high to preserve a clean response. This is a choice available to the designer/builder.

The product detector and BFO are

Fig 12.17—Transmit mixer, bandpass filter and keyed RF power chain.



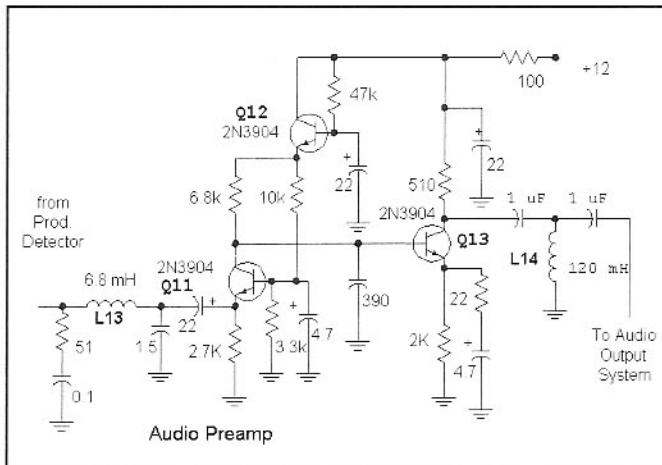
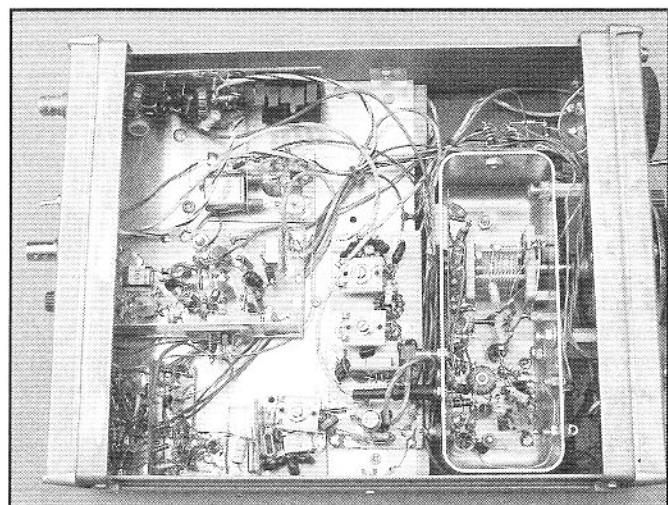


Fig 12.18—Audio preamplifier for the Unfinished.



Top inside view of the "Unfinished-7" Transceiver. The VFO module is at the right. The board parallel to the VFO is the double tuned front-end filter, mixer, and post-mixer amplifier. The third order Gaussian-to-6-dB crystal filter and IF amplifier are along the bottom with the BFO and product detector just above. The crystal calibrator and transmitter output amplifier are toward the upper left.

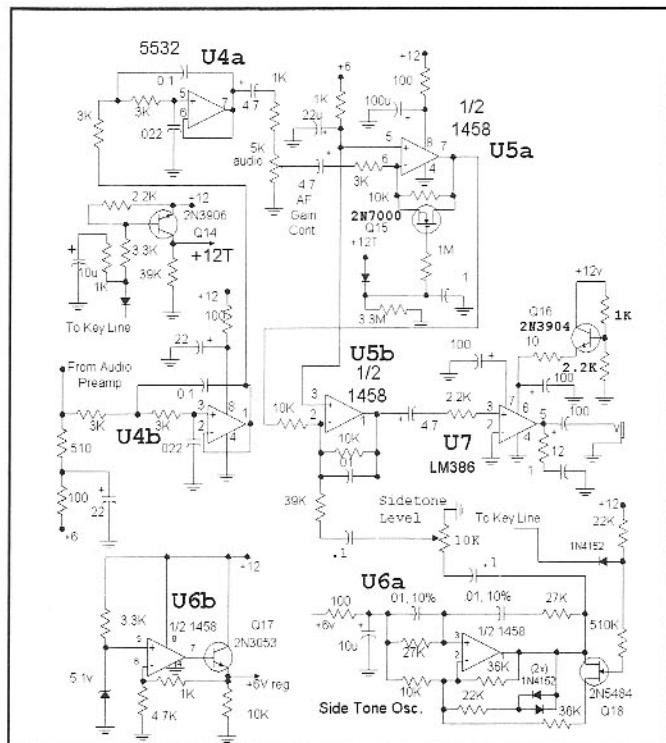
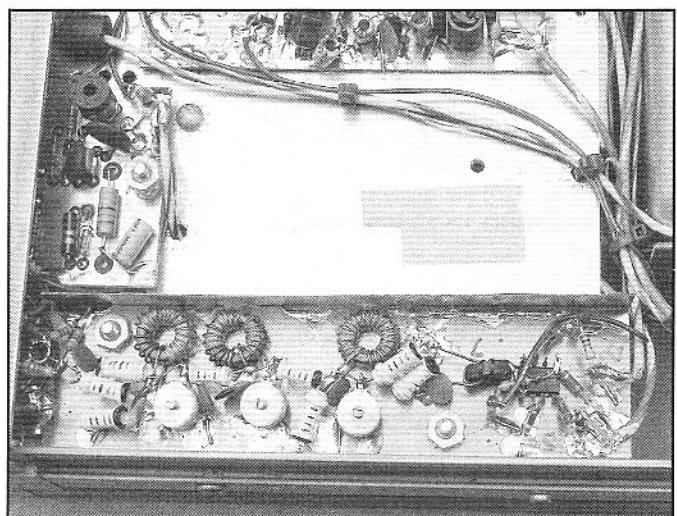


Fig 12.19—Audio output system. An RC active low pass filter, sidetone oscillator, 6-V regulator and T/R control are included.



The transmit mixer and triple tuned bandpass filter. Shield strip along one side of the board helps to confine ground currents.

shown in Fig 12.16. A bipolar transistor oscillator is followed by a pair of FET followers. One drives a bipolar power amplifier that then drives a diode ring product detector while the other routes signal to the transmit mixer. A separate keyed carrier oscillator was originally used. However, this produced a slight chirp. Any detectable chirp was deemed intolerable, so the design was altered. The RIT is always activated during use, with the "center" position providing a zero offset situation. A simple crystal calibrator (not

shown) allows calibration in the field.

The transmit mixer, 7-MHz bandpass filter, and RF power chain are shown in Fig 12.17. A modest NE602, U8, works well as the transmit mixer. The BFO and VFO signals are both confined to 0.3 V peak-to-peak at the IC. This is a place where measurement is important, for "more" is not better. A triple tuned bandpass filter terminated in an un-keyed amplifier, Q19, follows the mixer. The circuitry from U8 through Q19 is built on a separate board with a long narrow shape

with little shielding. The signal from Q19 is routed to a keyed amplifier, Q20 and Q22 with output up to 0.5 W. The Q22 emitter resistor is adjusted for the desired drive to the PA in use. No power amplifier design is shown, allowing the designer/builder to use what he or she needs. Spectral purity was measured with a high efficiency 8-W PA in place (See the W7EL "Brickett" described in Chapter 2). Two non-harmonic output spurs found close to the 7-MHz carrier at the -60 and -63 dBc levels.

The product detector drives an audio preamp, shown in Fig 12.18. An input LC low pass filter drives a familiar common base stage, followed by a common emitter amplifier driving a high pass LC filter.

The rest of the audio system is shown in Fig 12.19. U4a and b form a 4-pole RC active low pass filter with a peak at 850 Hz, -6 dB cutoff at 1.3 kHz, and a -40 dB response at 3.3 kHz. This low pass is a wonderful supplement to the minimal, but carefully designed IF crystal filter. U5 provides additional audio gain and a convenient place for receiver muting. U7, an

ubiquitous LM386, provides audio output. Bypassing of pin 7 improved power supply rejection problems that produced a thumping sound with strong CW signals.

U6a and Q18 form perhaps the best side tone oscillator we have used. The op-amp is a Weinbridge oscillator with back-to-back limiting diodes. The circuit is close to oscillation with an open key. Circuit gain is changed by FET switch Q18 when the key is pressed. Q18 was picked for low pinchoff of -1.5 V. The relatively small gain shift produces a sidetone output that is free of clicks. Output is

extracted from a point that does not change dc level when keyed.

U6B with Q17 form a 6-V regulated supply. This is used in the audio system as well as in the transmit mixer. Q14 provides a switched +12 V in transmit. The transceiver is breadboarded with no printed circuits, allowing frequent and convenient changes.

Although this rig is featured here as an experimental vehicle, it has done well in extended operation for several years of home use as well as several backpacked Field Day efforts.

12.3 THE S7C, A SIMPLE 7-MHZ SUPER-HETERODYNE RECEIVER

This receiver began with a long list of goals. It was to be a super-heterodyne design, offering the basic selectivity, sensitivity, and stability of the classic topology. The design was to use generic devices, avoiding the market driven whims of the semiconductor manufacturers. An adaptable circuit was desired, something that could be altered for other bands and modes. Low power consumption was a goal, allowing the circuit to function for an extended period with a handful of AA cells. And, above all else, it was to be a simple design, suitable for both the beginner and the seasoned designer/builder. The resulting superhet example shown is for the 7-MHz CW band, generating the S7C designator.

A block diagram for the receiver is shown in Fig 12.20. A cascode JFET mixer front is driven by a VXO. While the tuning range is restricted, the stability is excellent. The restricted range simplifies construction, for no dial drive mechanism is required. The mixer then drives a two-crystal filter embedded between two bipolar transistor amplifiers. The output is routed to a product detector, audio amplifier, and headphones.

The circuit, shown in Fig 12.21, began with the elements of the "Micro-R1" Minimalist Direct Conversion Receiver presented in Chapter 8. Q1 is an audio output amplifier driven by audio preamplifier, Q2. A crystal controlled BFO, Q3, provides the needed injection for a two-diode product detector. The only changes of significance are the addition of an audio gain control and a few component value changes. The most significant of these is C4, which is larger than the value used in the original direct conversion receiver. This component was increased to provide greater flexibility in setting the

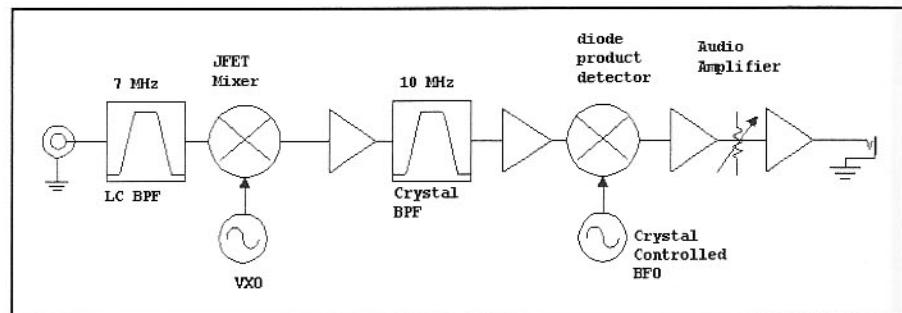
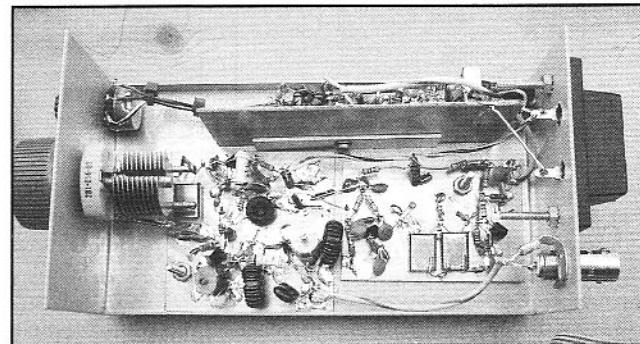


Fig 12.20—Block diagram for the S7C.



Top inside view of the simple superhet receiver. The left board houses the front-end mixer and the VXO. The board at the right contains the IF and crystal filter. The power connector uses a quick disconnect normally used with audio speaker cables.

BFO, Q3, to the proper frequency.

The audio and BFO sections were breadboarded on a scrap of circuit board material, a 7-MHz crystal was dropped in at Y2, and the receiver was tested as a direct conversion circuit. The original Micro-R1 of Chapter 8 was driven by a link coupled double tuned circuit. The low impedance of the link provided the low audio impedance needed for proper detector operation. We added a radio frequency choke (value not critical) to the circuit to obtain the required gain. C1, a 5-65-pF trimmer capacitor in the BFO allowed some tuning around the crystal frequency. We eventu-

ally substituted a fixed capacitor in the circuit for C1, saving the trimmer for yet another project. The builder should review the discussion in Chapter 8.

The IF amplifier was built next. This design obtains selectivity from a double tuned circuit using two crystals. The filter is placed between two feedback amplifiers, each followed by a 6-dB pad. Each amplifier is biased for a 3-mA emitter current with a 9-V supply. The amplifiers and pads are designed for a characteristic impedance of $150\ \Omega$, a departure from the more common $50\ \Omega$ designs. The product detector works well when driven from this

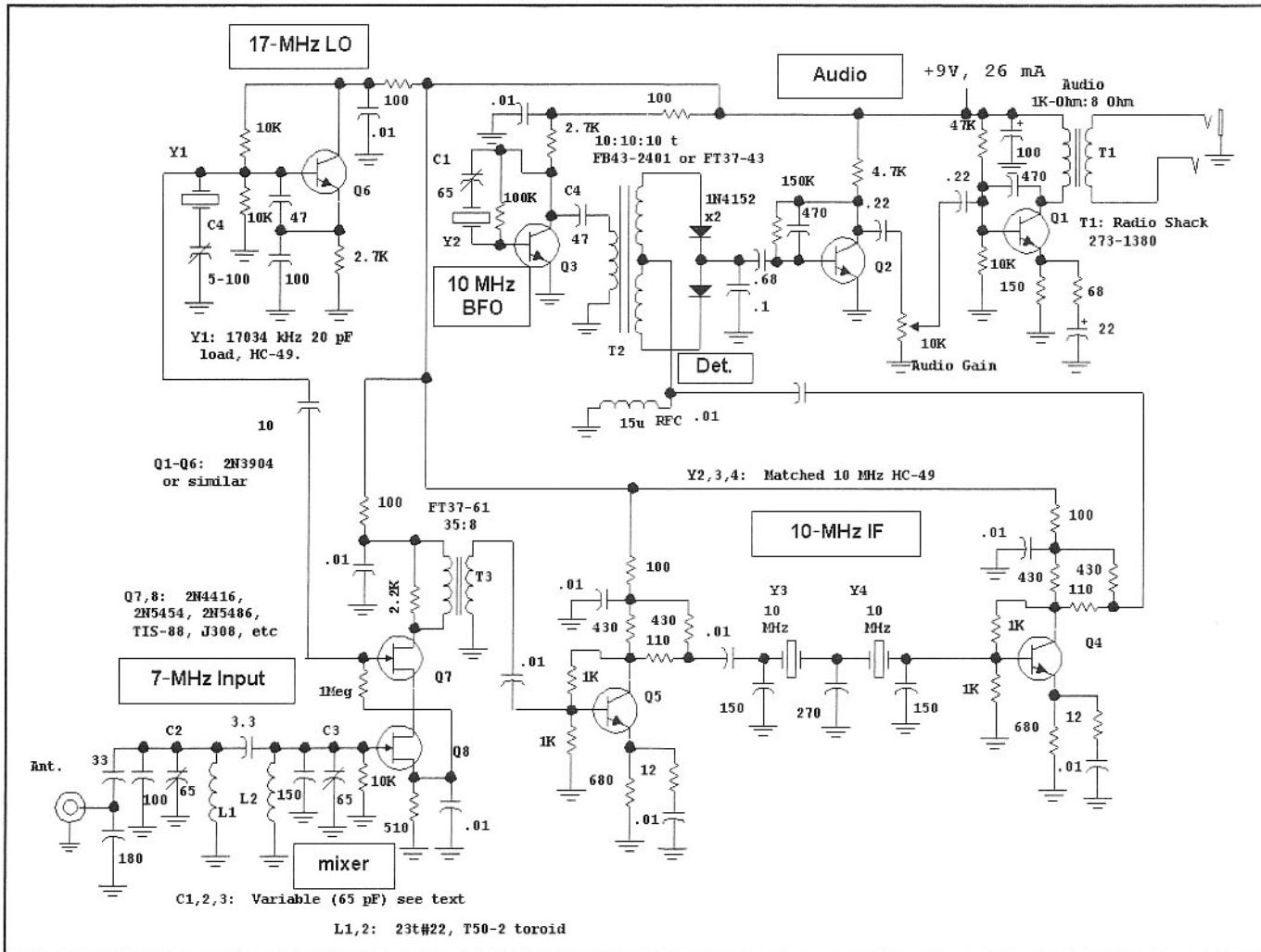
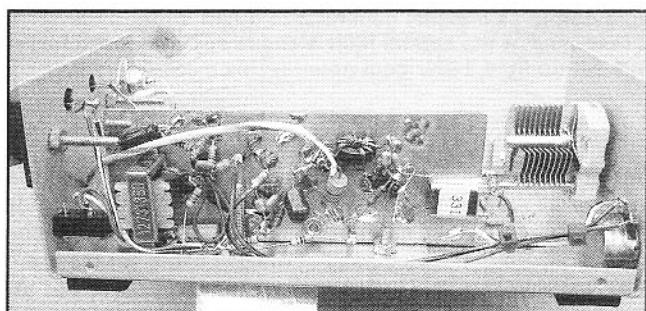


Fig 12.21—Schematic for the 7-MHz super-heterodyne.



The audio and product detector board for the simple superhet receiver.

This emphasizes the need for front-end selectivity. We'll discuss this later.

The IF system was breadboarded on a small scrap of PC board material and tested with the product detector, which had been outfitted with a 10-MHz crystal. While detailed evaluation of the IF filter would happen later, we used a signal generator to confirm that the functionality of the circuit. The single signal response was dramatic, considering the circuit simplicity.

The next part that was built was the 17-MHz VXO, Q6. This circuit used a crystal that had been specially ordered for the desired frequency, although the crystal is not otherwise special. We wished to have the tuning approximately centered at 7.040 MHz, the gathering spot for North American QRP operators. Our IF turned out to be centered at 9.9989 MHz, just over one kHz below 10 MHz. The sum of these frequencies is 17.039 MHz. VXOs tend to tune upward with much greater ease than they do downward, so we picked a fre-

impedance. The crystal filter was also designed for 150- Ω terminations at each end.

The builder should purchase a few inexpensive HC-49 crystals from one of the popular mail order sources (Mouser, Digi-Key, etc.). The crystals are then matched with an oscillator circuit and a frequency counter. The BFO (Q3) could even be used as the test oscillator if you don't wish to build a separate test circuit. Y3 and Y4

should be within about 50 Hz of each other. Y2, the BFO crystal, is much less critical, for that frequency will be adjusted with C1. See Chapter 3 for information on crystal filters.

We used a 10-MHz IF in this example, for crystals were available in our junk box. This presented a problem, for 10-MHz signals from WWV and/or WWVH leaked through the front end and could be heard.

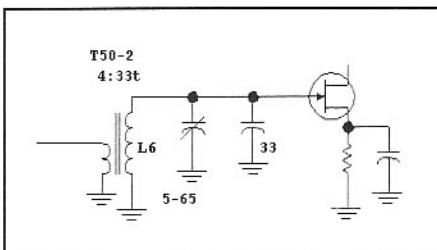


Fig 12.22—Single tuned mixer input circuit.

quency of 17.034 and ordered an HC-49 cased fundamental mode crystal, specified for a 20-pF load capacitance. The final tuning range for our receiver was from 7030 to 7045 kHz. (The crystal was measured using equipment described in Chapter 7, resulting in $L_m = 3.72 \text{ mH}$ and $C_0 = 6 \text{ pF}$.) The builder will need to pick a different crystal frequency for compatibility with an alternative IF or target frequency. The VCO was built on yet another scrap of circuit board, and was eventually moved to the breadboard containing the mixer.

The receiver is completed with a front-end mixer. Several circuits were tried, producing the cascode of two JFETs, Q7 and Q8. This mixer has no balance, so it will function as an amplifier, allowing input RF signals to appear at the output. This is the route of the 10-MHz feed-through problem mentioned earlier. The mixer can also become an oscillator operating at the frequency of the input tank. This oscillation was easily suppressed with the 2.2-kΩ resistor in the Q7 drain circuit. If you encounter a problem here, reduce the value of this resistor. A tuned circuit at T3 on a powdered iron toroid would be a preferred solution.

This mixer has some strong virtues. First, it is quiet: We measured a 10-dB noise figure with this circuit. The current is low at about 3 mA. Very little LO power is required, allowing drive from simple oscillators. We found that the performance is best with a signal at the gate of Q7 of about 5 V peak-to-peak. This circuit is similar to the popular dual gate MOSFET mixers that were common in receivers in the 1970 to 1990 timeframe. We measured IIP3 of +5 dBm for this mixer, making it suitable for wide dynamic range applications.

The mixer is also breadboarded on scraps of PC board material. The ferrite output transformer, T3, is wound on a low loss -61 core material, offering better gain than a more common -43 core. The FET type used was a 2N5454, again a choice dictated by the junk box. These parts had $I_{DSS} = 10\text{mA}$ and $V_p = -3 \text{ V}$. However, there is nothing special about this FET.

Front panel view of the simple superhet.

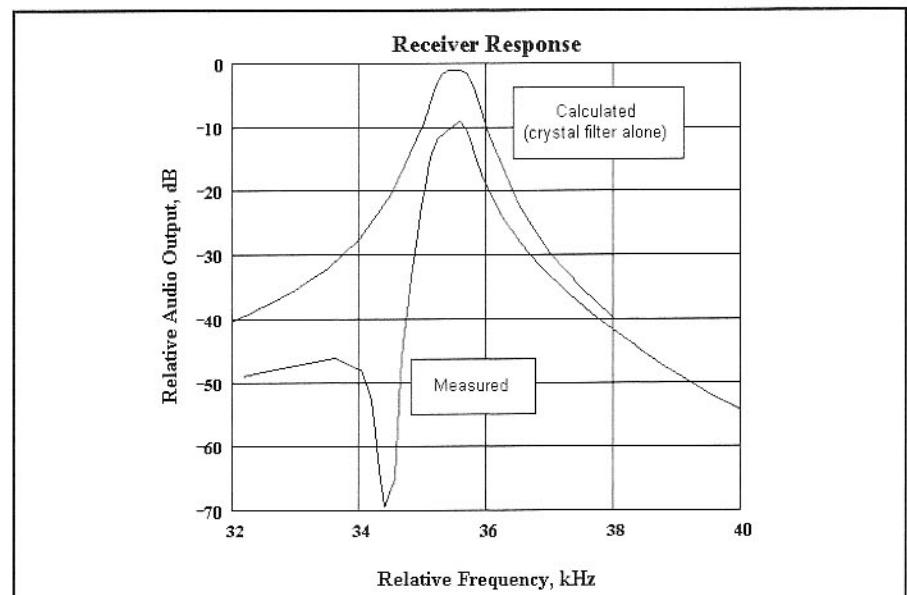
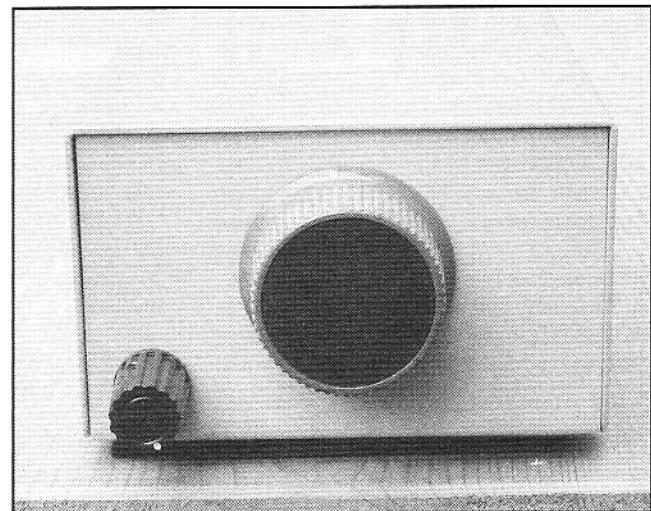


Fig 12.23—Measured audio output as a signal generator is tuned through the receiver. The calculated response of the crystal filter alone is superimposed for comparison. The BFO was set up for a 1-kHz beat note for this measurement.

Virtually any of the common JFETs will work well. If a higher I_{DSS} part is used it may be worthwhile to experiment with the bias resistor.

The mixer in our receiver used a double tuned input circuit. The front-end selectivity eliminated all traces of the feed-through from WWV. Initial experiments used a single tuned input, shown in **Fig 12.22**. An external low pass filter (7th order 7.5-MHz cutoff Chebyshev, see Chapter 1) was then effective in eliminating WWV feed-through. A 10-MHz trap (LC or crystal) could also suppress the spurious response.

Results and Variations

This receiver is a joy to use. The first

experiment that is always performed with a new receiver is a session of listening. The narrow bandwidth is effective on a moderately crowded band, yet the use of just two crystals produces a bright and lively sound not compromised by excess filtering. The constrained gain, modest selectivity, and lack of AGC make the receiver especially useful when the 40-meter band is dominated by the thunderstorms of late summer.

After a period of listening, we measured the receiver and experimented with some alternative circuits. A 7-MHz signal generator was applied to the receiver to determine the selectivity, shown in **Fig 12.23**. The single-signal character is clear. The response null occurs as the generator is tuned through zero beat, a result of the

audio characteristics.

We measured MDS of -138 dBm with this receiver, consistent with the NF measurement and an overall bandwidth slightly narrower than the 500 Hz of the crystal filter.

The stability of the V XO was excellent, but left us wondering what was happening down just a few kHz down the band. So, we temporarily replaced the V XO with a

3-MHz signal generator, which worked well. A simple single transistor oscillator would serve in this application.

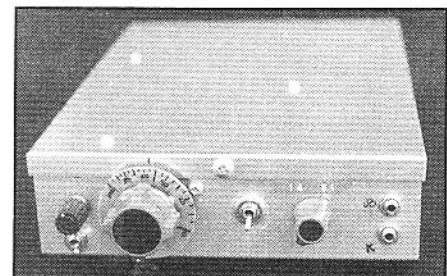
Some users will want more selectivity. The crystal filter could be redesigned to use more crystals. A simple alternative would add another crystal filter just like the first one. The impedance at the output of T3 and the input impedance of Q5 are both $150\ \Omega$, so the filter would be properly terminated in this position. The additional two crystals should be frequency matched to Y3 and Y4.

Ed Kessler, AA3SJ, built a similar receiver with inexpensive off the shelf crystals for the IF and the V XO. In his version, he used 4.0 MHz for the IF with a LO at 11.046 MHz. The LO used a "super V XO" with two parallel crystals, a topology discussed in Chapter 4.

12.4 A DUAL BAND QRP CW TRANSCEIVER

This transceiver began as an experiment to investigate electronic band switching methods, but evolved into an enjoyable QRP rig. The super heterodyne design, Fig 12.24, covers the 14- and 21-MHz CW bands with an output of two watts. An available junkbox 9-MHz crystal filter provided receiver IF selectivity. This circuit is described to illustrate ideas rather than for duplication.

Band selection begins with a mechanical switch in the transmitter portion of the circuit. The three-section switch selects the two ends of the transmitter low pass filters and establishes dc lines that route throughout the transceiver for frequency control. For example, a line labeled "+12(21)" provides +12 V only when the rig operates in the 21 MHz band.



Front panel view of dual band transceiver.

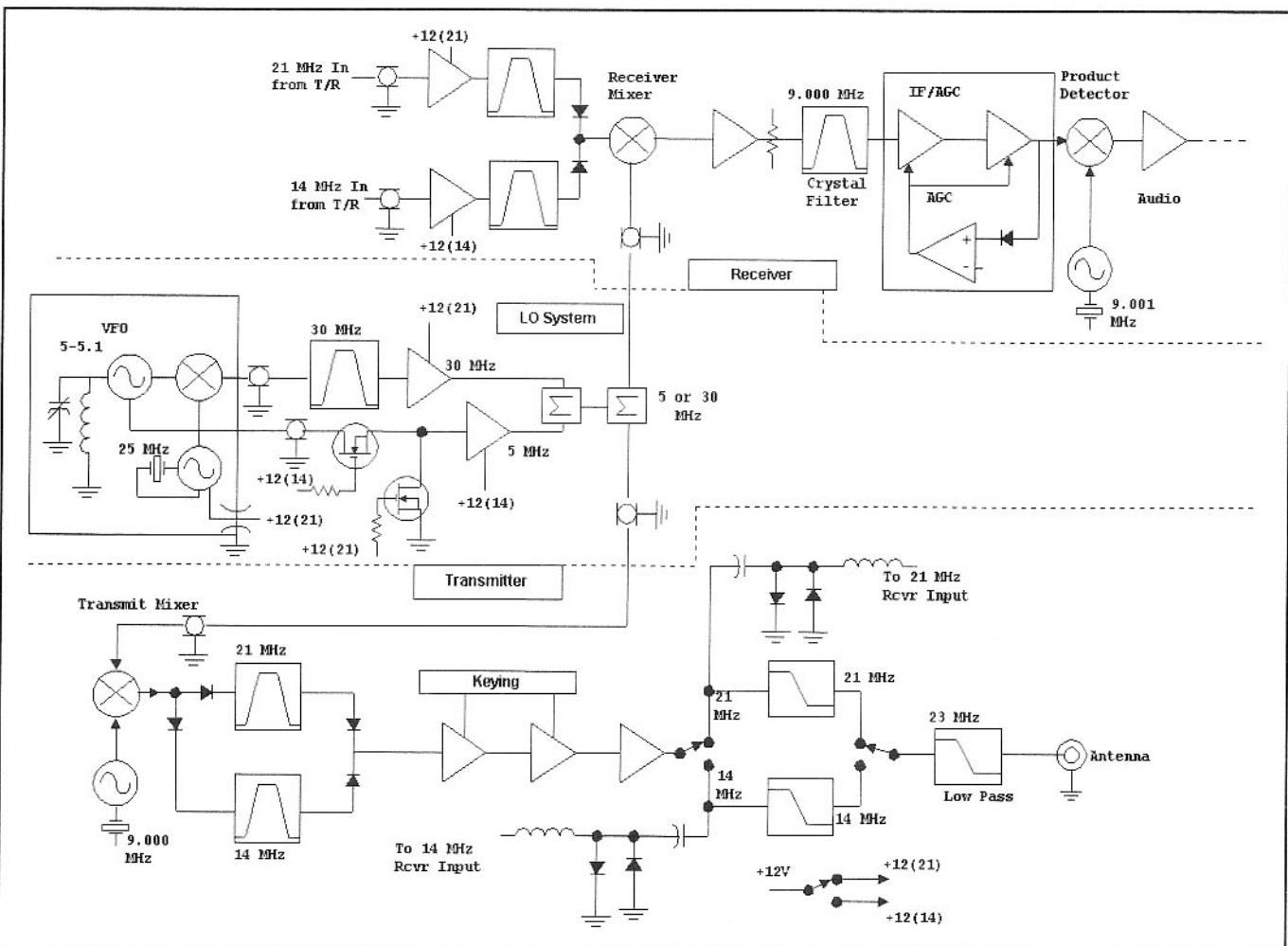
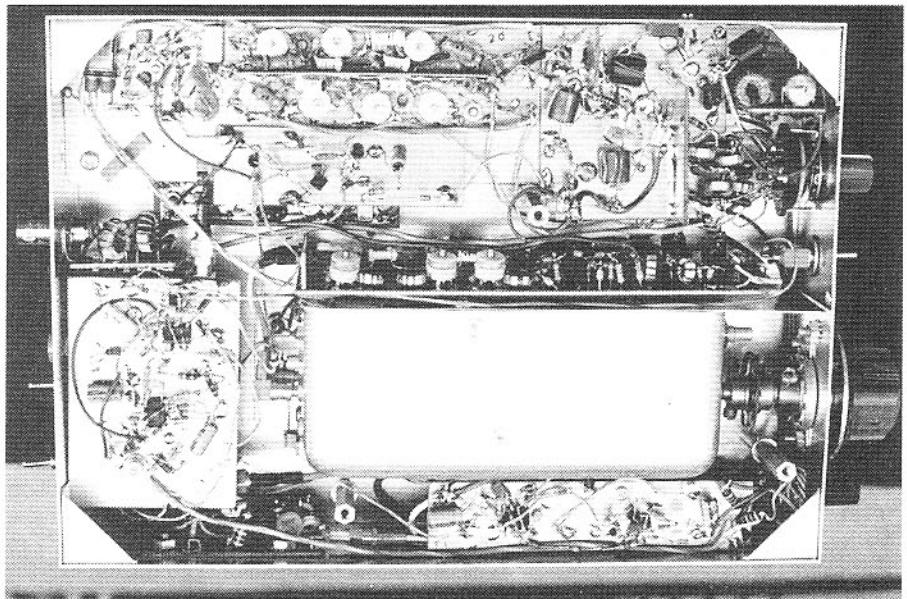


Fig 12.24—Block diagram for the dual band transceiver. The upper region is the receiver with the transmitter at the bottom of the page. LO details appear in the middle of the block.

Inside view of dual band transceiver. Mounted below the VFO enclosure are the LO chain bandpass filters. The PA is bolted to the side of the box near the bandswitch. The triple tuned transmitter bandpass filters are along the lower edge of the photo. Most receiver front-end circuitry is hidden below the transmitter chain. Audio, product detector, and BFO circuitry are along the upper edge of the photo. The IF amplifier is between the VFO and the rear apron with the crystal filter under the board.



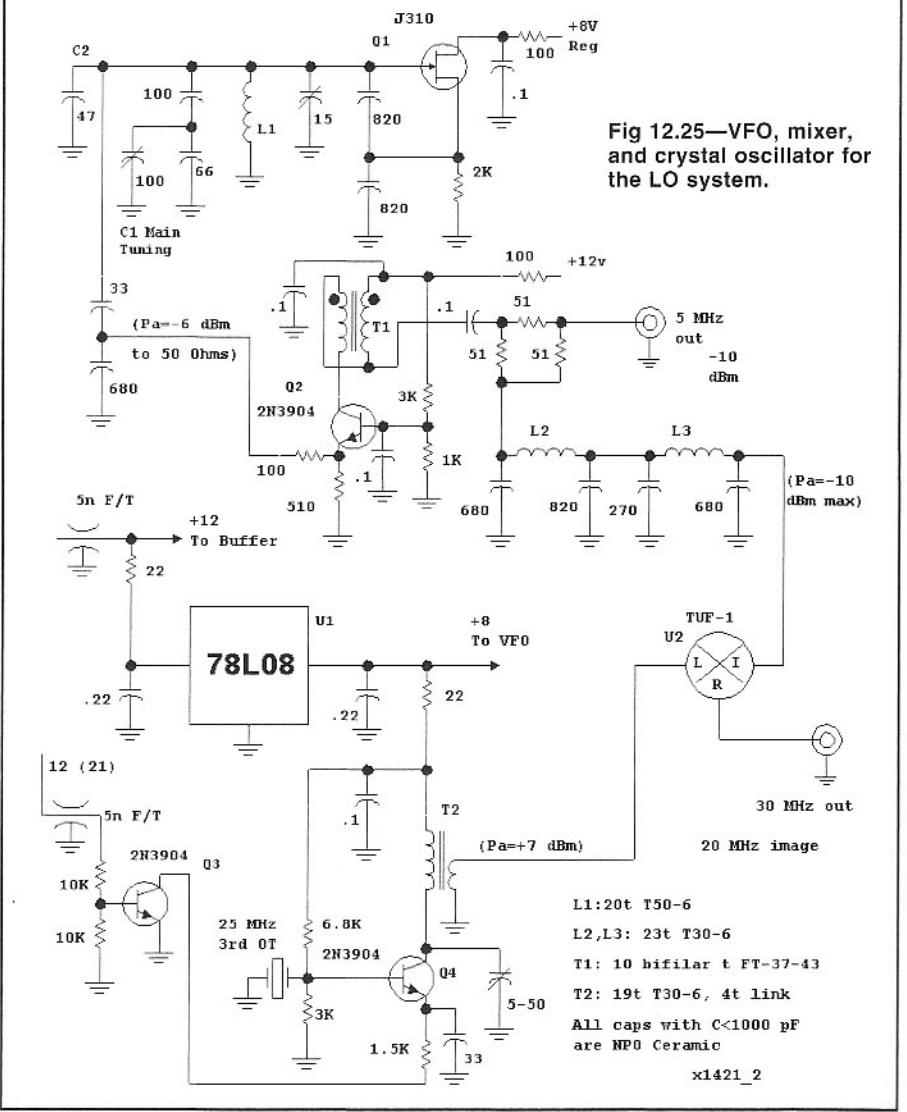
Local Oscillator System

The LO uses a 5-MHz LC oscillator, a mixer, and a 25-MHz crystal controlled oscillator, shown in Fig 12.25. This portion of the LO resides in a shielded box. A signal is extracted from the VFO resonator to drive a common base buffer, Q2. The output is applied to a resistive power splitter with one output available at a coaxial connector. The other output is filtered and applied to a diode ring mixer, U2. The "LO" for that ring mixer is the 25-MHz crystal controlled oscillator which is active only when the 15-meter band is selected. Signal levels are stabilized with an 8-V regulator. Powers are measured and carefully established before the module is sealed, ideally with a spectrum analyzer. The mixer output is attached to coaxial cable with short leads and then to an output connector with the desired 30-MHz signal and a 20-MHz image.

RF outputs from the oscillator module are applied to a filter board, shown in Fig 12.26. The 30-MHz signal drives a three-section bandpass filter. Feedback amplifiers Q5 and Q6 increase the 30-MHz level to +11 dBm after low pass filtering.

The 5-MHz signal from the VFO module is attenuated in a 6-dB pad and then applied to a series MOSFET switch, Q9. This switch is "on" only in 14-MHz operation. The output is then increased in cascaded feedback amplifiers, Q7 and Q8, and low pass filtered, generating an available power of +12 dBm for use with 14-MHz operation. The gain is slightly lower in Q7/Q8 than in Q5/Q6. Only one of the two outputs is available at a time, for only one

Fig 12.25—VFO, mixer, and crystal oscillator for the LO system.



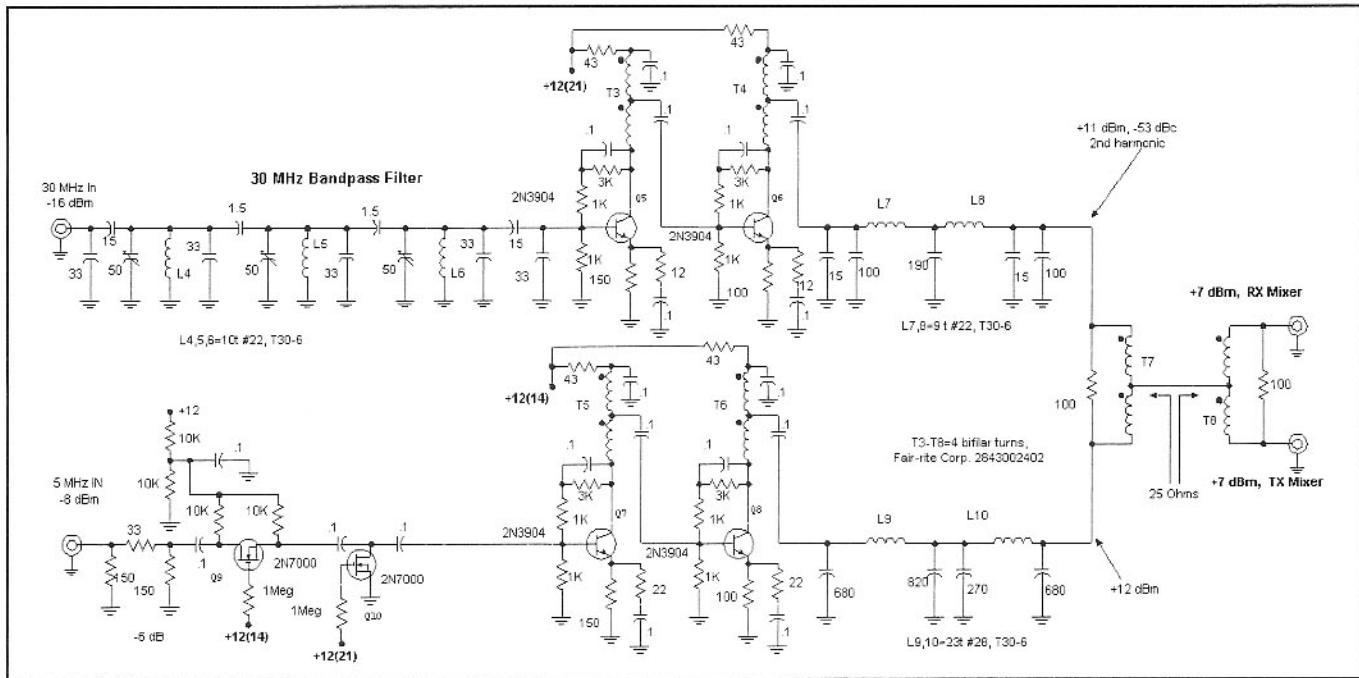


Fig 12.26—The LO signals are processed in this board. The 30-MHz signal is bandpass filtered, amplified, and low pass filtered. The 5-MHz signal is amplified and low pass filtered. Outputs are combined with a 0-degree hybrid. Another hybrid splits the signals, providing +7 dBm for both the transmit and receive mixers.

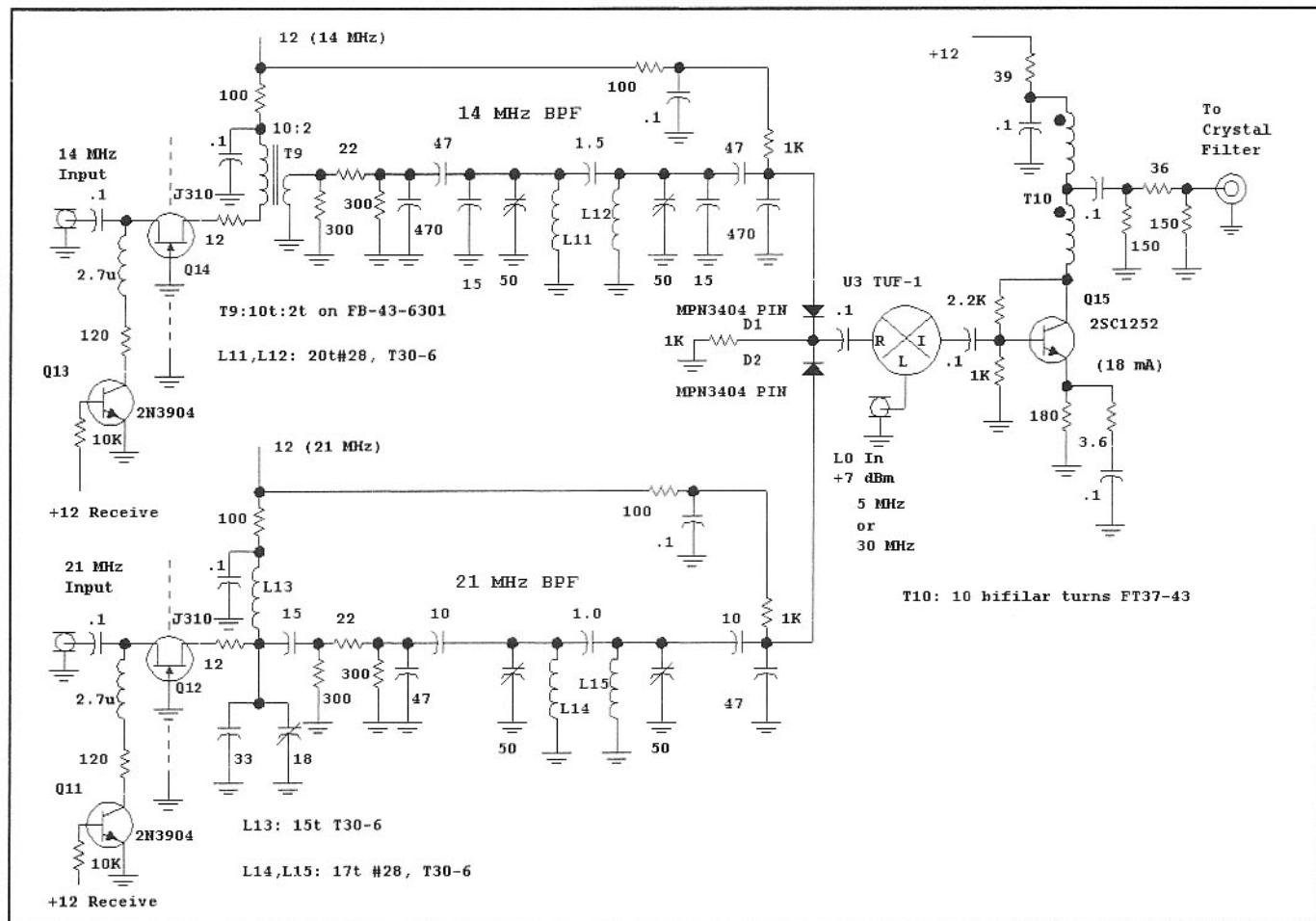


Fig 12.27—The receiver front end for the dual band transceiver. PIN diode switching is used to select the bandpass filter output appropriate to the band in use.

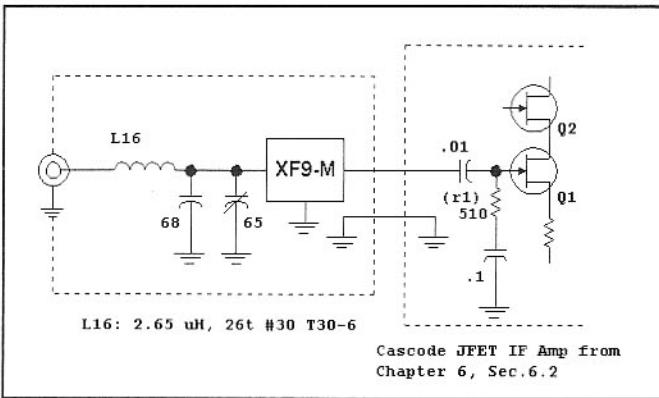


Fig 12.28—Input section of the crystal filter and IF amplifier for the transceiver. See text.

bank of amplifiers is biased on. Suppression of the 5-MHz component during 21-MHz operation is improved with a shunt MOSFET switch, Q10. The two outputs are combined without switching in a 0-degree hybrid built from T7. The output would contain both signals if both were on at the same time. The resulting output is split into two equal, but isolated components with another hybrid, T8. The result is a pair of +7-dBm signals for the two diode ring mixers in the receiver and transmitter.

The harmonics are more than 50 dB below the desired LO outputs, and images are difficult to find. Before the shunt FET switch, Q10, was added, some 5-MHz energy could be seen when the 30-MHz component was dominant. However, adding the switch pushed the 5-MHz component to the -80 dBc level. This is more extreme than needed, but instructive.

Receiver Circuits

The receiver is much like others we have described. A low-gain, moderately low-noise RF amplifier drives a diode ring mixer. The RF amplifiers were designed for good input match rather than lowest noise. A post mixer amplifier, Q15, provides signals to a crystal filter. A JFET based IF amplifier adds gain and provides a convenient place for AGC. Another diode ring serves as the product detector with a conventional audio chain.

The front end, the only place where band switching is needed, is shown in Fig 12.27. Each of the RF amplifiers, Q12 and Q14, is powered only when the respective band is selected. Transistor switches remove current from the RF amplifiers during transmit intervals.

MPN3404 PIN diodes are used for band selection. There are slight differences in the two RF amplifiers. That for the 14-MHz band uses a ferrite transformer

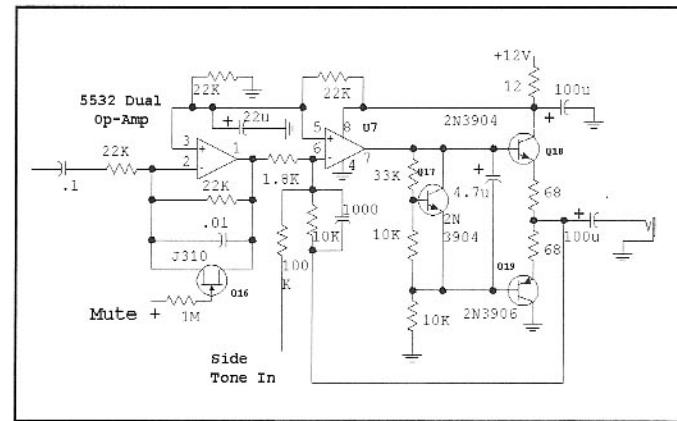


Fig 12.30—An audio output amplifier for the receiver.

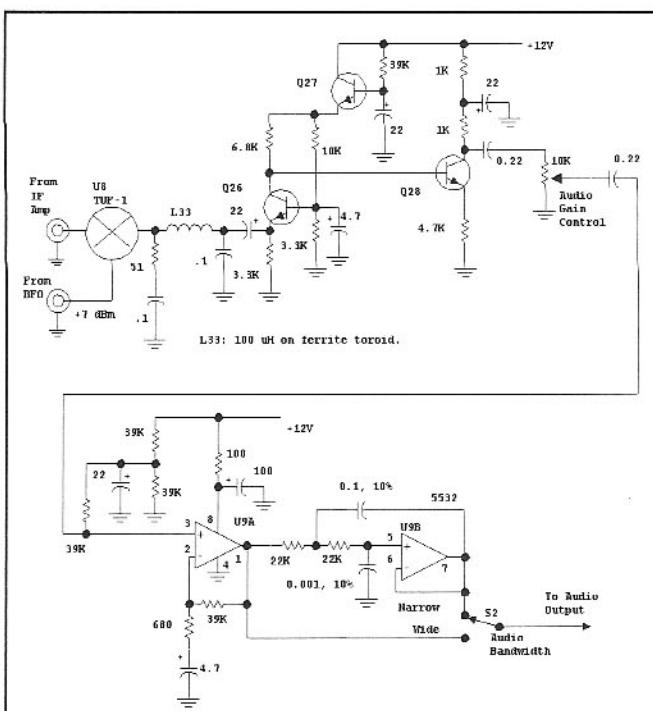


Fig 12.29—Product detector and audio amplifier. The emitter of Q28 may be bypassed for gain higher than needed here.

while the output in the 21-MHz circuit is tuned. A pad (just over 3 dB) drops the gain a bit and helps to fix the impedance for the following double tuned bandpass filters.

The diode ring mixer is followed by a post mixer amplifier with modest current of 18 mA. This then drives the crystal filter and IF circuit, shown in the abbreviated circuit of Fig 12.28. The input $50\ \Omega$ is transformed up to $500\ \Omega$ with the L-network shown. A variety of IF amplifiers have been used in this circuit, most with low gain. The one presently in use is that from Chapter 6 using cascode connected J310 JFETs. The original circuit was modified by changing the input resistor to $510\ \Omega$ to properly terminate the German (KVG XF9-M) crystal filter we used. The

designer/builder may wish to add a transformer to match between the crystal filter and the $2.2\ k\Omega$ originally in place; the higher impedance will allow greater gain, lower noise figure, and greater flexibility in AGC threshold adjustment.

An early version of this receiver used nothing more than a single JFET as the IF amplifier. Only manual IF gain control was used; most of the overall gain was obtained at audio. Performance was excellent for use in working other QRP stations. However, we found it lacking for general use when stronger signals were routine. The present system includes AGC with an adjustable threshold.

The detector and audio system, shown in Fig 12.29, is the "standard" used throughout the book for direct conversion

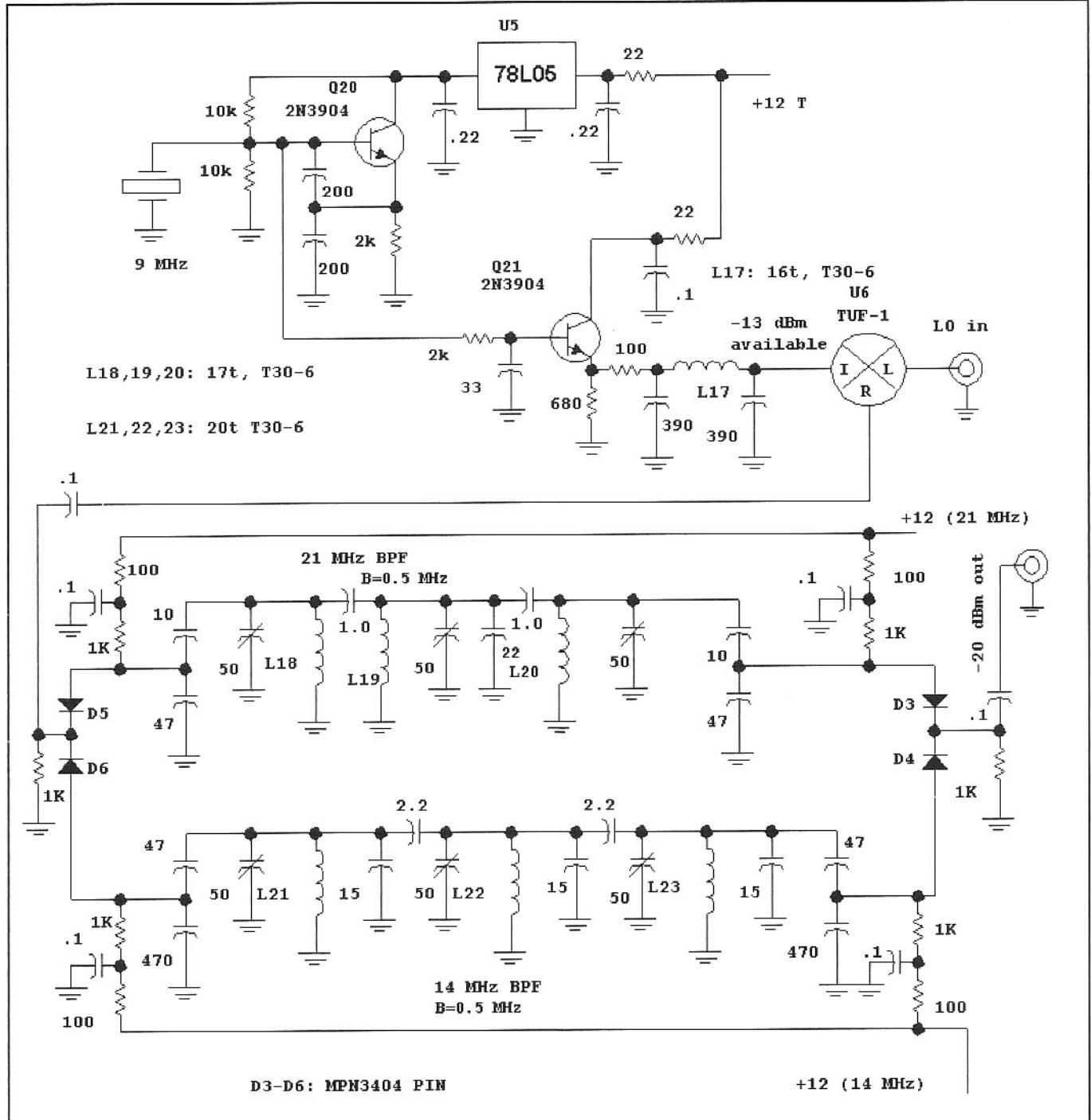


Fig 12.31—Transmit mixer with PIN diode switched bandpass filters. See text for details.

systems and simple superhets. A TUF-1 diode ring product detector drives a common-base amplifier. The second audio stage operates at a gain of about 0.2, but it could be increased as needed. After the audio gain control, an op-amp provides voltage gain, followed by a switchable peaked low pass filter with a Q of 5.

The circuit shown in Fig 12.30 using plastic transistors and an op-amp will drive a small speaker. The high open loop gain of the

op-amp keeps distortion low. This circuit, with only 10 mA in Q18 and Q19, would benefit from increased standing current, reducing clipping that occurs with high output.

The rest of the receiver is routine and is not repeated here. The crystal controlled BFO and sidetone oscillator are not shown. This receiver measured NF=11 dB, IIP3=+3 dBm, for DR=93 dB with a 500 Hz bandwidth. The receiver AGC is degraded by BFO energy reaching the IF

system. BFO and IF shielding would both improve performance.

Transmitter Details

A simple heterodyne process generates the output signals for the transmitter, shown in Fig 12.31. A 9-MHz crystal oscillator is applied as the RF signal to a diode ring mixer. The larger drive at 5 or 30 MHz comes from the LO chain. The

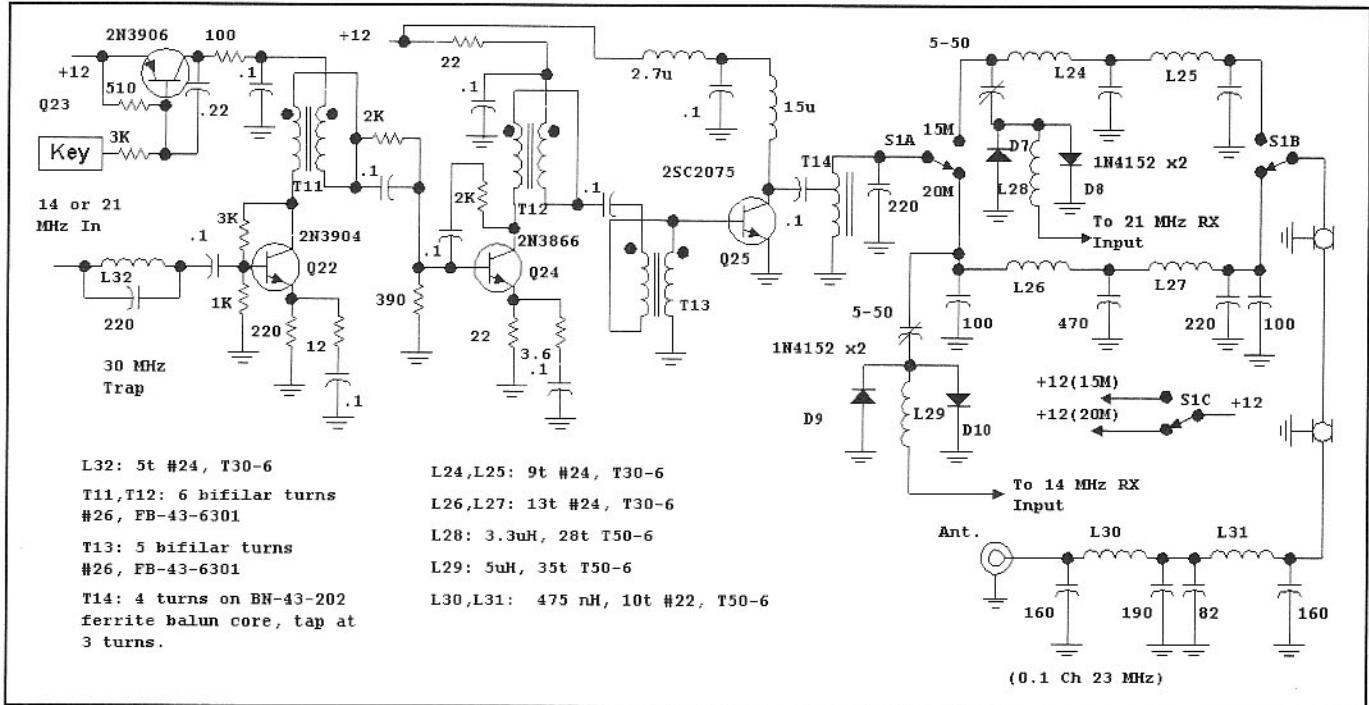


Fig 12.32—RF power chain for the transceiver.

mixer output is then filtered in one of two PIN diode switched bandpass filters.

The initial transmit mixer system used double tuned circuits for both bands and had no 9-MHz low pass filter. The results were interesting. Although the 21-MHz observed output was clean, there were spurious outputs related to the 14-MHz band. These occurred at 13 and 16 MHz at -52 and -56 dBc. The 13-MHz spur was a 1:2 spur that could be solved with reduced harmonics in the 9-MHz drive. The higher frequency spur was related to a 5:1 product. (A N:M spurious output frequency results from $Nx f_{LO} \pm Mx f_{RF}$; See Chapter 5.) The third order low pass filter was added to the 9-MHz RF, pushing the first spur to the -72-dBc level with no change in the other.

The 14-MHz double-tuned circuit was changed to a triple tuned filter with a bandwidth of 0.5 MHz. The higher frequency spur was now suppressed to -75 dBc and the lower one was lost in the noise. We later found some 30-MHz energy in the 21-MHz output, which prompted a change to a triple tuned filter for that band as well. None of these results would ever have been observed without the use of spectrum analyzer for the experiment. But the result is a justification for using a triple tuned bandpass over a simpler double tuned circuit when one seeks improved spectral purity. While triple tuning uses more components, it is no more difficult to design or tune at HF than one with two resonators.

The transmitter powerchain, shown in Fig

12.32, begins with a 30-MHz trap, tuned by compressing turns on L32. A two-stage driver amplifier then provides the bulk of the gain and adequate drive power for Q25, the 2SC2075 output stage. A wideband transformer, T14, reflects a load of about 28 Ω to the PA collector. Both driver stages are keyed to produce a backwave below -70 dBc. Low pass filters for both bands are selected with the mechanical band switch. A final 23-MHz low pass is then added to the output.

We were still able to find two spurs in the output for each band. They were, however, all at -62 dBc or less. The worst harmonic was the 2nd when operating at 14 MHz at -63 dBc. With the exception of the VFO, only incidental shielding is used.

12.5 WEAK-SIGNAL COMMUNICATIONS USING THE DSP-10

Chapter 11 contained an overview of the DSP-10 DSP-based 2-meter transceiver and the associated audio processor. The published material on this project is on the CD-ROM and has the details necessary to build and modify this radio. An interesting application of the DSP-10 is the processing of signals to allow detection of stations too weak to hear with the ear, and to allow communication with these stations at very slow data rates. This is an example of what is practical to achieve using the programmable aspects of the radio. As was discussed in the overview, there are many other possible appli-

cations. In addition to the following summary of weak signal operation, detailed material is available on the CD-ROM that accompanies this book.⁸

Additive Noise

The expression *weak signals* is a relative term. Normally, the signal is referenced to the received noise level. Of course, the nature of this noise changes with frequency and conditions. Interfering signals and static from lightning can provide a complex noise environment that is most challenging to the weak-signal

enthusiast. Simplifying matters for our consideration here, the primary noise source considered is the well-behaved thermal noise, also known as white Gaussian noise (WGN). The "white" refers to the flatness with frequency and "Gaussian" refers to the probability distribution, also called normal or bell-shaped. WGN dominates the VHF and higher frequencies, but this source extends down into the HF bands as well.

This WGN is added to the signals received at the antenna terminals. This is a result of our receiver being linear. As was discussed in Chapter 2, filtering can

reduce this additive noise, since it is flat with frequency. This gives us a way to remove noise from signals, so long as the bandwidth of the signal is less than the filter bandwidth.

Signals and Multiplicative Noise

The signals being transmitted for weak-signal work can generally be chosen to occupy reasonable bandwidths.⁹ Simple modulation methods are the most easily dealt with and can generally be used. An example is a single frequency tone, transmitted for a predetermined amount of time. This signal can be extended to two or more tones in order to convey information as frequency shift keying. This idea will be explored further below, but here it is important to observe that the received signal is not generally an attenuated version of that transmitted. Instead, as the signal passes through the transmission media (atmosphere, ionosphere, Moon reflection, etc.) modulation is applied to the signal. This is akin to the modulated signals described in Chapter 6.

As the signal passes through the transmission media the amplitude varies—in amateur lingo, this is QSB. Typically, this variation is random in nature. What we have is a signal with amplitude modulation (AM). Frequency sidebands will appear on either side of the transmitted carrier as with all AM signals. The frequency offset of the

sidebands depends on the speed with which the amplitude varies. Faster changes produce sidebands farther from the carrier. In addition, the length of the transmission path will vary, again often randomly. Movement of the refractive and reflective layers causes this. In this case, we have phase modulation (PM), again producing sidebands on either side of the signal.

It is possible for the AM and PM sidebands to add and cancel in different ways for those above the carrier than for those below. Consequently, the modulation placed on the signal by the transmission media is not symmetrical about the carrier frequency, and may not look like a typical modulation spectrum. As a modulation it is multiplicative noise and different from the additive noise just discussed. We do not have the option of removing this noise by filtering, since lowering the bandwidth removes the signal along with the noise. The propagation media places a lower limit on the filter bandwidth usable with a narrow-band signal.

A General Approach

A wonderful paper by K3NIO¹⁰ outlines this weak-signal communications problem and proposes a practical solution that he and K8DKC demonstrated on 20 meters. Poor's model for signal and noise were the ones we have above and his communications system, built around RTTY and FSK, applied these principles:

- Maximize the transmitter average power by having it on continuously
- Minimize the receiver (pre-detection) bandwidth, consistent with the signal and propagation path modulation
- Use detectors to estimate the signal amplitude at each frequency
- Trade off time and sensitivity by following the detectors with low-pass filter(s) to provide averaging (integration) of the signal amplitude.

The performance of the system was limited by the availability of low-pass filters (RC networks), suitable for very long integration times. But as Poor points out, so long as one can build a low enough cut-off to the filter, the ultimate sensitivity of this approach is limited only by our patience for the answers to appear.

Going to more than two frequencies was not part of the 1965 system, but was known to offer improvement for communications systems.¹¹ Today the multi-tone filtering can be performed by discrete Fourier transforms (see Chapter 10). Long-term integration is easily done in a digital computer. The following two examples, taken from the DSP-10, show how these ideas can be applied using DSP techniques.

Example 1 - EME-2 for Moon-bounce Echoes

THE GOAL

A 2-meter station, with the antenna

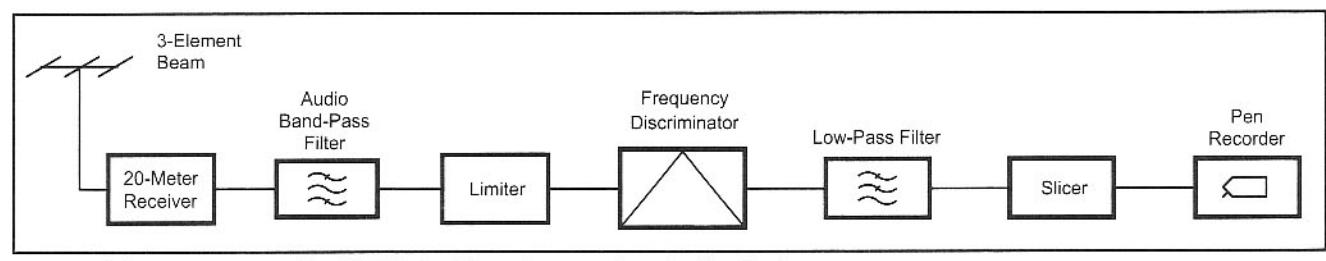
The K3NIO Experiments

The 1965 experiment reported by K3NIO represented an early attempt at signal processing to receive beyond the limits of the human ear. K3NIO and his collaborator in this effort, K8DKC, were RTTY enthusiasts and had frequency shift keying (FSK) equipment available. They did their 14-MHz experiments in the late evening hours when the band was essentially dead. The transmitters were set up for narrow FSK and keyed with standard CW, driven with an automatic keyer set for a typical speed of 3 words per minute. The two stations were separated by 500 miles, used three element Yagi antennas and 1-kW transmitters. The stations were crystal controlled to provide stability that was not common in 1965.

Their receiving system is shown in the block diagram

below. The normal 14-MHz receiver had improved selectivity, provided with an audio bandpass filter. The audio signal was applied to a limiter, and then to a frequency discriminator. The output from that circuit is a dc level indicating the frequency of a tone moving through the system. The dc was filtered, or averaged with an RC active low pass filter with a 1-Hz cutoff. The resulting dc then drove a comparator and a strip chart recorder, allowing visual copy of CW.

The results were dramatic. Essentially, they found it possible to make slow speed contacts, even when they could not detect the presence of any signal when listening to the receiver operating in the normal mode.



The receiving system used by K3NIO for his early experiments. See text.

pointed at the Moon, can transmit a pulse for roughly two seconds and then receive the resulting echo. This comes back 2.6 seconds after it was transmitted, as shown in Figure 12.33. Adding to the challenge, if this “Moon-bounce” station is of modest proportions, the received signals will be extremely weak. For instance, a station with two 12-element Yagis and 500 W of transmitter power can expect to see an average power return of about -160 dBm. For the noise levels encountered on this band the resulting signal-to-noise ratio might be about -5 dB in a 50-Hz bandwidth, which is totally inaudible. Regardless, the goal of this example is to be able to measure this and much weaker echoes coming back from the Moon. The value, in addition to satisfying a general curiosity, is allowing the measurement of the system performance of the station and the propagation path.

As a reference point, we should examine just how well this “marginal” Moon-bounce station can hear his echoes. Helping the situation, the signal strength fades above and below the average return. This is due to the irregular surface of the Moon and the shifting nature of the path. With some patience, the signal will appear for a second or so at, perhaps, 6 dB higher level or 1 dB S/N. Additionally, if the antenna is along the Earth’s surface the signal reflected from the ground will sometimes add to that coming in directly, adding as much as 6 dB more to the signal. Now we are up to about 7 dB S/N. At this level, a perceptive operator will sense by ear the presence of a Moon-bounce echo. However, if the station is located where ground reflections are poor, such as at the edge of the forest, the echoes may never be heard.

Looking for a way to use DSP to enhance the detectability of the echo, one should explore the elements outlined above. First, we narrow the pre-detection

bandwidth to the limit set by the modulation of the propagation path. On 2-meters this is generally 1 Hz or less. Next, any amount of improvement is possible by post-detection averaging that we call long-term integration. This resulted in a mode called EME-2 that was implemented in the DSP-10 software, as will be described below. However, before exploring these receiver concepts, it is worth considering the transmitter side to see if we might do better there as well.

TRANSMITTER WAVEFORMS

In the discussion above, we decided it was desirable to increase the average power of our transmitter by having it on as much as possible. Holding the key down for two seconds and listening for about 3 is only on 40% of the time. It might be possible to transmit on one frequency for 2 seconds and then move a MHz higher and transmit for seconds two through four. If the transmitter and receiver could be separated sufficiently, either in a geographical sense or by use of filtering, such as that of FM repeaters, this might be a preferred method of operation. But for most stations, the simplicity of merely sharing a single antenna by means of an antenna relay is an overwhelming consideration. The loss of average power can still be made up for by more integration.

The waveform considered here is a constant-frequency sine wave, keyed on and then off two seconds later, generating a pulse. One might hope that a more elaborate modulation would be helpful for identifying the returned signal. Radar designers have considered this problem for many years. In terms of detectability, the theory offers no encouragement in this area. The key factors are the power in the transmitted pulse and the care with which the receiver pre-detection filter is “matched” to the received waveform.¹²

Thus, we might as well work with the simple approach and that is a keyed sine wave.

PRE-DETECTION FILTERING

The one-Hz filter for our system is a major challenge for LC construction, but is easily accomplished with the discrete Fourier transform (DFT) of Chapter 10. There are other possible DSP implementations, but the DFT provides a bank of filters that is useful for estimating the noise level and for the case that the signal is not received on frequency for some reason. The filter response of the DFT may not be the exact matched filter, but the bandwidth is close to proper and the losses for improper shape are not large.

The DSP-10 implementation of the DFT has several bandwidths available, in steps of two, with the narrowest being about 2.3 Hz. This is not a fundamental restriction, but neither does it provide optimal performance. Those with an interest in this area might explore using narrower bandwidths by increasing the sampling time interval.

LONG-TERM INTEGRATION

At each filter bin of the DFT the power can be calculated as the square of the received envelope (see Chapter 10). This power can be added up for a number of bins near that where the signal should be received. The bins on either side are estimates of the noise power and the center bin is signal-plus-noise power. From these two quantities an estimate of the signal strength alone can be made, using only subtraction.

A complication in continuing the integration process for extended periods is the changing Doppler shift of the return signal.¹³ In the DSP-10 implementation of this process, the Doppler calculation is quite elaborate and accurate to better than 1 Hz at 2-meters. This allows the integra-

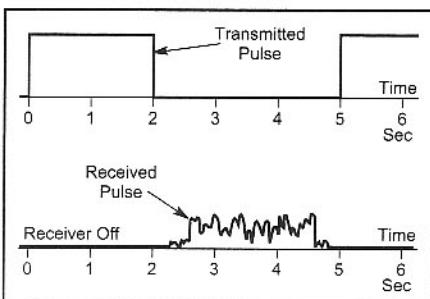


Fig 12.33—Timing diagram showing the two-second pulse being transmitted and the delay before the reception of the weak echo. This timing is repeated every five seconds for the EME-2 measurement mode.

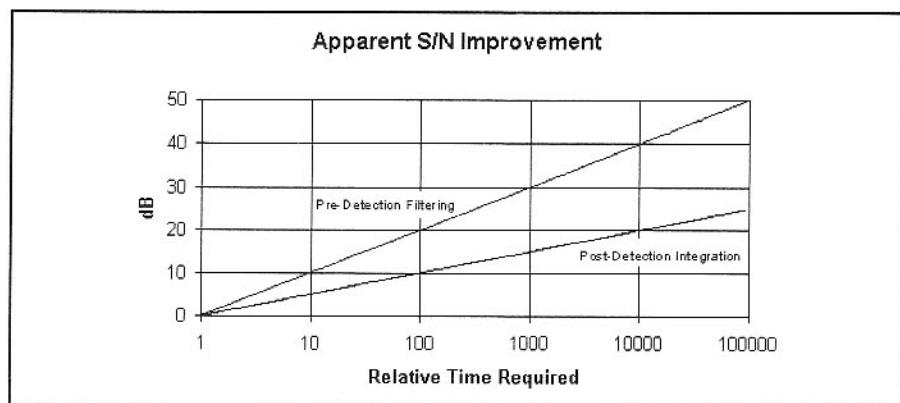


Fig 12.34—This is a comparison of the improvement in apparent signal-to-noise ratio for the pre-detection filtering and long-term post-detection integration.

tion to continue as long as the Moon is within view.

The remaining element is a means of displaying the return value. Two systems have proven of value for EME-2. A simple table of the signal-plus-noise estimates, expressed in dB, for 21 bins, centered on the return frequency provides most of the data. Along with this is the number of power values that have been integrated. A graphical plot of this same data also allows one to easily digest the results of a test and is always available.

A comparison of the improvement in apparent signal-to-noise ratio for the pre-detection filtering and long-term post-detection integration is shown in Fig 12.34. For either method, the parameter describing the amount of improvement is time. Expressed in dB, the rate of improvement is twice as great for the pre-detection filtering. This obviously only applies to the extent that multiplicative noise from the modulation path is not a limiting factor.

A SAMPLE OF EME-2

A number of tests have been made using EME-2 in the DSP-10. These have verified the concept that the amount of integration determines the sensitivity and there is no obvious lower limit to the process.¹⁴ One of these test results is shown in Fig 12.35, where a reasonably modest 100 W was used by W7PUA with a single Yagi, having a 34-foot boom. This antenna, a

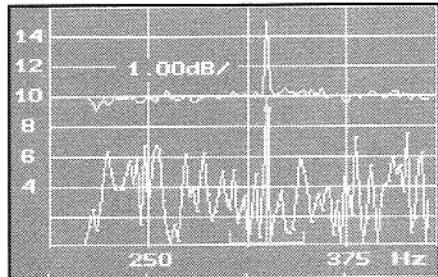


Fig 12.35—This portion of a DSP-10 screen shot shows the graphical output with the EME-2 mode Moonbounce echo. Some editing has been done to remove uninteresting parts of the display. The vertical scale is relative power in dB and the horizontal scale is audio pitch in Hertz. The bottom trace is the power average of one return. The upper trace results from averaging 71 of the lower traces together. The return signal has had its frequency adjusted for Doppler shift and always lines up with the vertical line at 323 Hz. The scale is different for the two traces, with 2 dB per division for the lower trace and 1 dB per division for the top averaged trace. At 144 MHz, the transmitter power was 100 W and the antenna was a single 34-foot Yagi.

commercial M² 2MXP28 product used with a home-built combining hybrid, has circular polarization to minimize the degradations from Faraday rotation.¹⁵

The lower trace is the result of one two-second-pulse return. Because the bandwidth of each DFT is wider than that of the pulse, there are nine DFT's involved in generating this trace. The amplitude of the signal-plus-noise shown here is about 6 dB over the average noise and somewhat stronger than average. The upper trace is the result of averaging 71 two-second pulse returns together, requiring about six minutes. The noise averages to its power at all frequencies while the signal-plus-noise at the 323 Hz line is about 2.4 dB greater. After this many pulses, the signal return on the upper trace becomes very well defined and the level of the return can be measured quite accurately. This signal echo was never heard by ear.

Example 2 - PUA43 for Weak Signal Communications

The work of K3NIO suggests the possibility of using the EME-2 approach with frequency-shift keying as a modulation

method for weak-signal communication. Looking at the spectral plot for EME-2 certainly supports the idea that one might communicate by lining up multiple frequencies, each somehow corresponding to a portion of a message. The reference by Murray Greenman, ZL1BPU, points out the advantage of using more frequencies than the two used by Poor. With an eye towards pushing the limits of slow, weak-signal communication, a modulation and coding system was implemented in the DSP-10 that applied these principles. This used 43-tone modulation, where each tone represented a different symbol such as an alphabetic character. At the time a number of different schemes were being tried, and this particular one was nicknamed *PUA43*.

PUA43 sends the same message repeatedly, once or twice during each minute. It is quite structured. The message length can only be either 28 or 14 symbols long, each corresponding to specific two-second time periods. The number of minutes that the message is sent is determined by the users, giving flexibility for improving weak-signal copy by using many repeats of the same message.

Power received for each of the symbols is added over multiple repeats, just as was

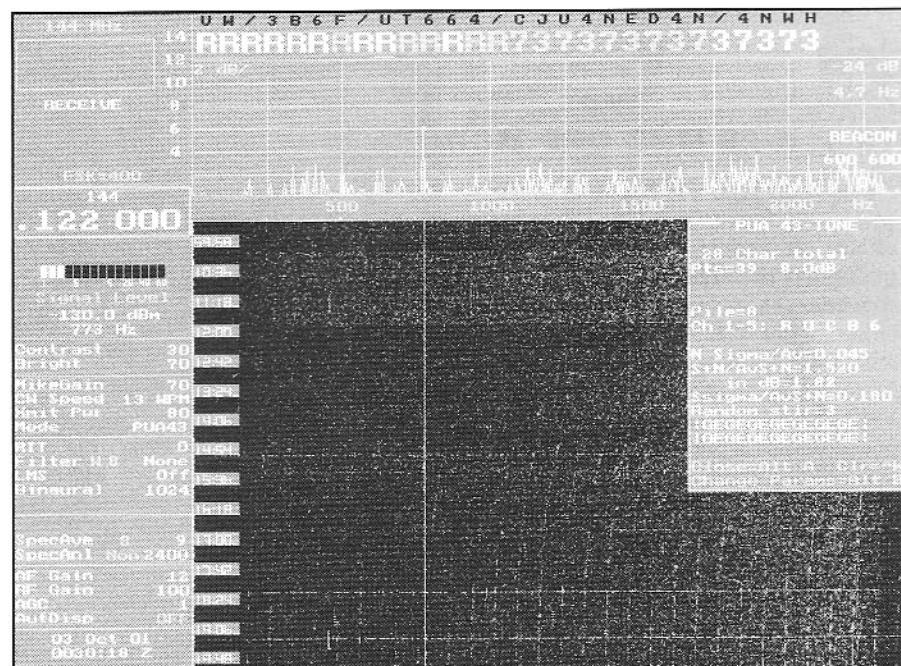


Fig 12.36—Screen shot from DSP-10 showing the reception of a PUA43 message by W7LHL. The signal-plus-noise to noise ratio of this plot is similar to that of the EME-2 reception of the previous example. The frequency band for the 43 frequencies in use extends from 450 to 1238 Hz, corresponding to the DFT bin spacing of 4.3 Hz that was being used. The large characters at the top of the screen are the most likely possibilities. The smaller characters above them are the second most likely. Various informational items relative to both transmission and reception are in the box on the right side of the screen. The straight line down the waterfall is a local interfering signal that is being ignored by means of frequency randomization.

done for each frequency in EME-2. Examining the power corresponding to the 43 possible symbols generates the display of the 14 or 28 characters. The most likely (highest power) and second-most likely symbols are displayed. The display color depends on the confidence of the particular character being correct, based on the measured noise characteristics.

An example of signal reception is in Fig 12.36, again on 144 MHz. The waterfall display (see Chapter 11) shows very little evidence of any signal being present, other than an interfering signal that is coming straight down the waterfall at about 770 Hz. The copy of the message, seen in large letters at the top of the screen is the result of integration of power for 39 minutes.

Several provisions of the PUA43 mode enhance the copy of signals. Every minute the frequency corresponding to a particular symbol changes by a positive offset that is the same for all symbols. The frequencies outside the frequency band being used for the 43 symbols are wrapped around to the bottom part of this band. This randomization, called stirring, causes coherent interfering signals (birdies) to get moved around to various symbols, rather than appearing as a false symbol. Additionally, there are unused frequencies between the 43 symbol frequencies. These are for noise estimation and serve two purposes. Know-

ing the noise levels across the band allows any variations in gain to be corrected so that they do not bias the symbol selection toward particular frequencies. Also, knowing the signal-to-noise ratio allows the confidence in a particular character being correct to be found, enhancing the data presented to the operator.

A characteristic of most weak-signal schemes is a need for accurate frequency control at the transmitter and receiver. This mode works best when the frequency can be controlled within a few Hz. As was done for EME-2, the PUA43 type of modes can be used for Moon reflections with the Doppler corrections that are available in the DSP-10. This adds a slight complication in needing to know the latitude and longitude of both stations.

The performance of this type of mode can be very good. A signal-to-noise ratio of -10 dB in a 50-Hz bandwidth will allow good copy of a message in about 6 minutes. As noted above, CW copy by ear might need 16 to 18-dB higher levels. Additional time allows even lower signal-to-noise ratios, but quadrupling the time used only has the effect of doubling the transmitter power. Though most people will not have interest in using extremely long times for a transmission, even a few minutes of transmission will provide a major improvement relative to audible copy. A

number of terrestrial and EME contacts have been made using the PUA43 mode. Perhaps one of the more interesting early EME contacts is that done Feb 25, 2001, by Ernie Manly, W7LHL, and Larry Liljeqvist, W7SZ, on 1296 MHz using only 5 W on each end. The antennas were ordinary surplus TVRO dishes of 10 and 13-foot diameter.

Further Directions

The DSP enhanced copy of weak signals provides an alternative to bigger antennas and higher power. One can expect that various schemes will be developed to use this capability. These should improve on the examples that are shown here.

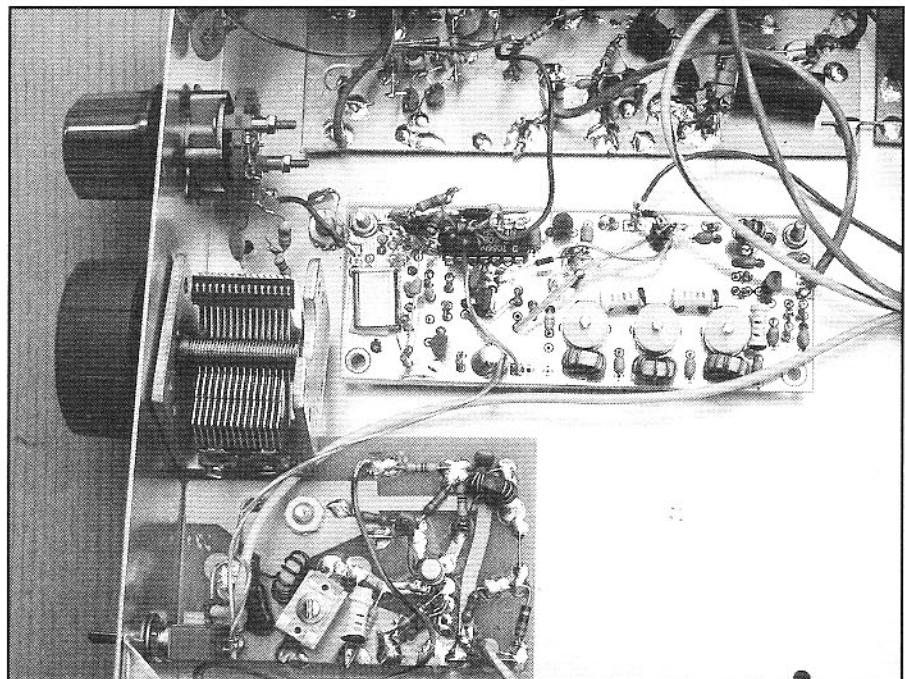
Other avenues exist that emphasize different elements of signal propagation. One example of this is the work of Joe Taylor, K1JT with the *WSJT* program.¹⁶ This uses a multiple frequency modulation and coding scheme, called FSK441, that is optimized to use bursts of signal, such as occur with meteor scatter. This contrasts strongly with the approach of the PUA43 mode that must grind out signal copy, based only on the average power being received. Each propagation situation needs to be considered as a strong determining factor in the system to be used.

12.6 A 28 MHZ QRP MODULE

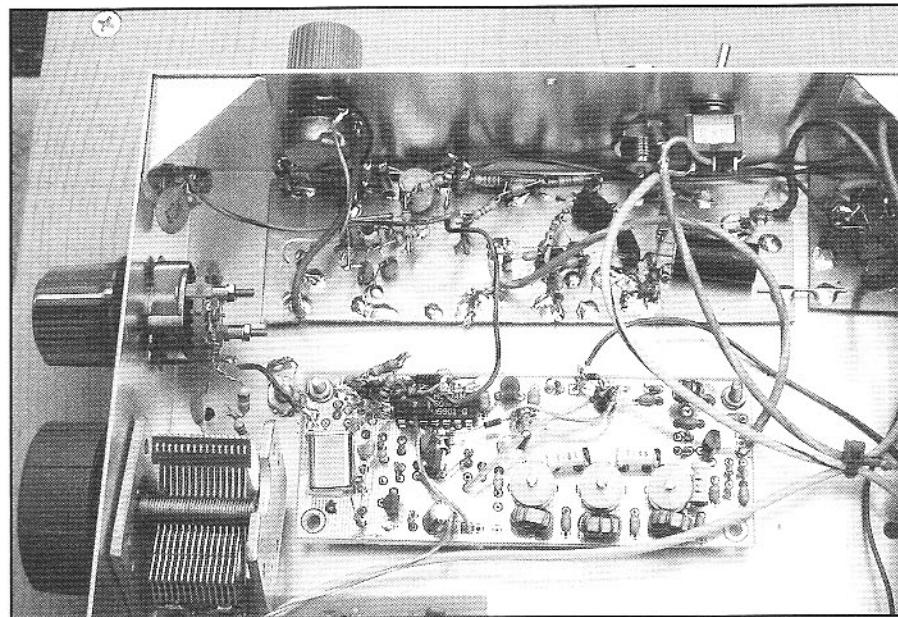
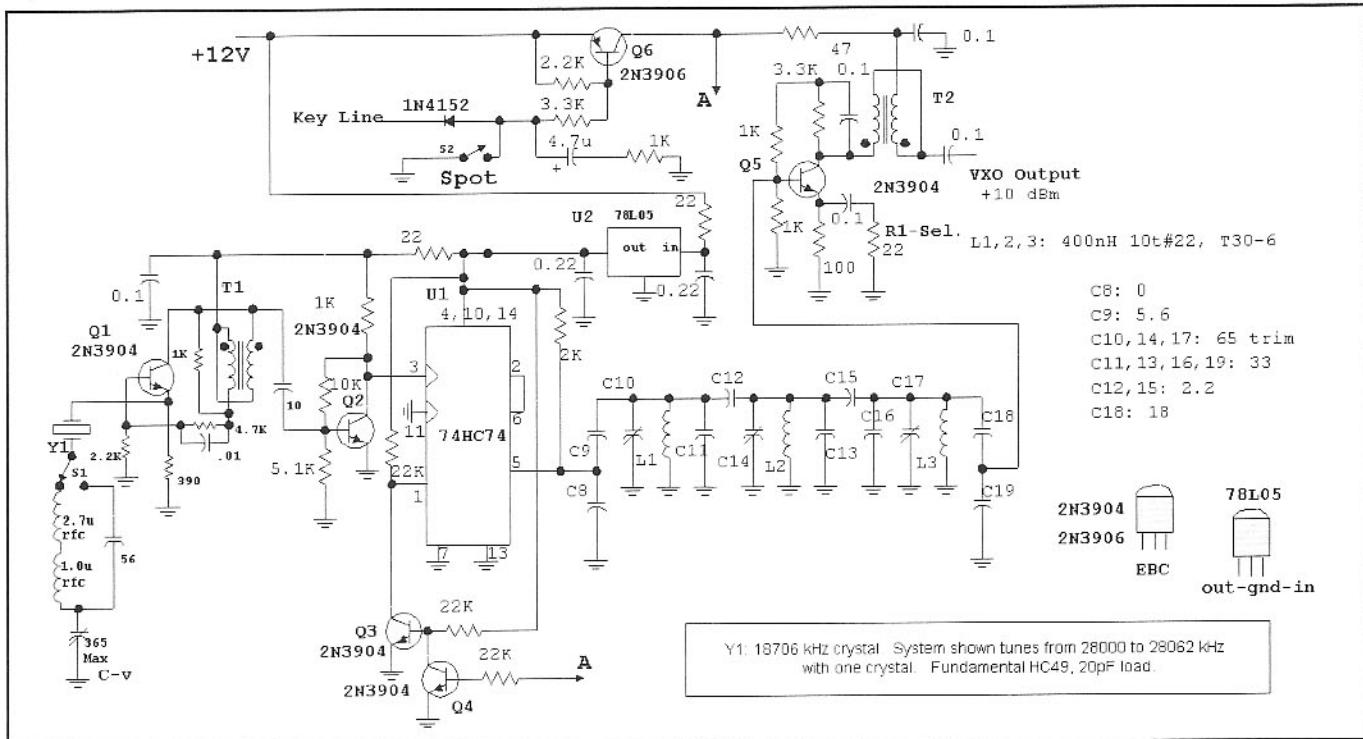
One approach to adding new bands to an existing low power station is to build an add-on module where a stand-alone transmitter is combined with a receiving converter. This example interfaces with a home station CW receiver (Chapter 6) with a 4-MHz input. This module uses a 28 to 4-MHz receiving converter and a VXO based 28-MHz CW transmitter. The power output is purposefully confined to 1 W, adding sport to an already exciting band. A single crystal provides a transmitter tuning range of over 60 kHz.

The Transmitter

The transmitter shown in Fig 12.37 begins with a VXO operating at 18.7 MHz. This free running oscillator is eventually frequency divided by 2, creating a square wave. The third harmonic of that signal, at 28 MHz, is selected with a bandpass filter, amplified, and keyed to form the transmitter. The VXO circuit with oscillator Q1 was originally like others shown in Chapter 4, providing about a 40-kHz tuning range at 28 MHz.



Inside view of the 10-meter module with the VXO and triple tuned bandpass filter in the center. The receiver RF amplifier board is at the bottom of the photo.



Inside view of the 10-meter module. The VXO board is below the board containing the rest of the transmitter. The output low pass filter and T/R relay are on the small board at the upper right. The delay control is on the side panel.

The circuit was modified to use two ranges and now tunes from 28.000 to 28.062 MHz with the available components. The low end of the band is tuned when S1 inserts a series inductance in the circuit. Experiments showed an even larger upward range was available if a separate tuning capacitor was used for

each range. This variation is shown in Fig 12.38. Experimentation is almost always useful with VXO circuits. (We measured our crystal as having $L_m = 3.01 \text{ mH}$ and $C_0 = 6 \text{ pF}$.)

The transmitter continues in Fig 12.39 with a driver using a parallel pair of 2N3904 transistors. The power amplifier

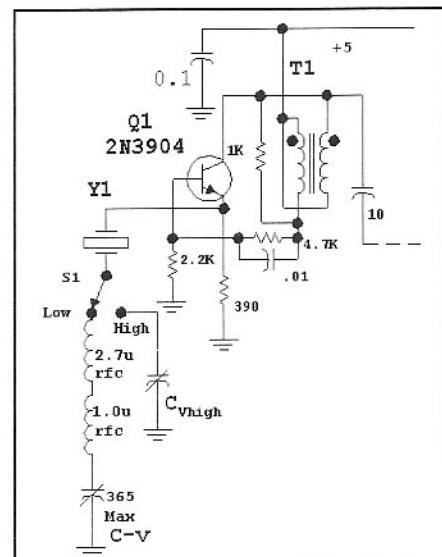
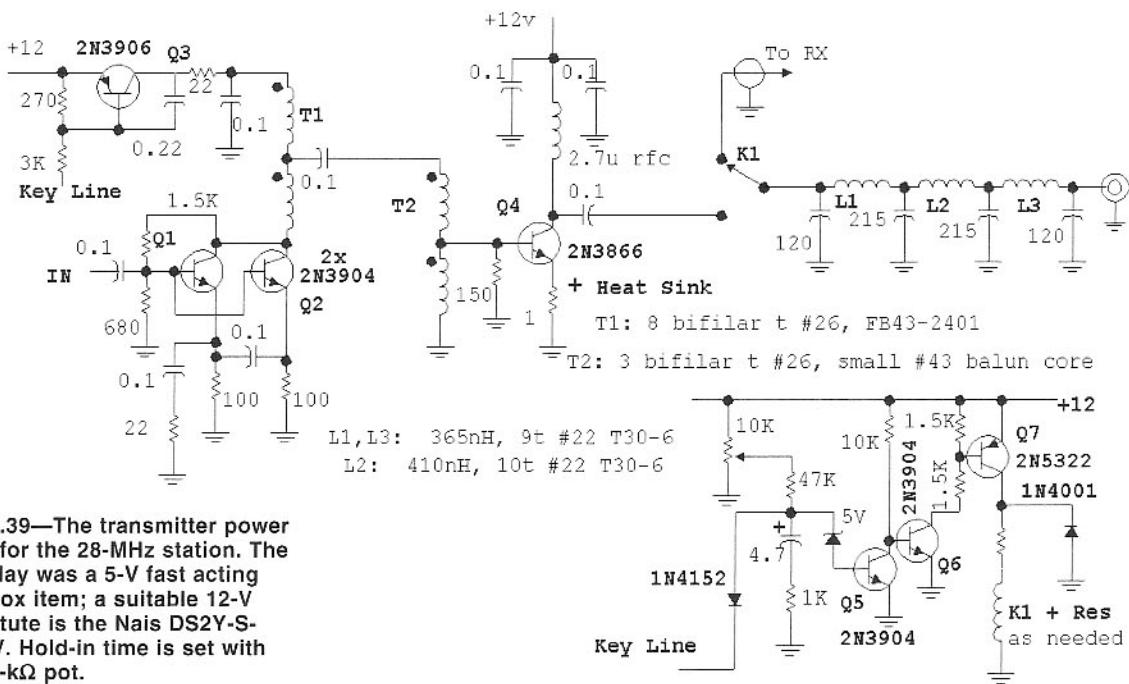


Fig 12.38—An even larger tuning range is available with a separate tuning control for each range. C_{VHigh} is selected from the junk box to have a low minimum capacitance.

is a 2N3866 with a 1- Ω emitter degeneration resistance. A 7-element low pass filter follows the transmitter, suppressing harmonics and other spurious responses. The only harmonic observed was the second at -69 dBc. The 18-MHz output is present in the output, but at the -73 dBc level.



Front panel view of the 10-meter module.

Receiving Converter

A diode ring mixer is the basis of the receiving converter, driven from a crystal-controlled oscillator using a 32-MHz third-overtone oscillator. The post mixer amplifier is a common gate JFET with a drain current of about 13 mA. A narrow bandwidth 4-MHz output feeds a wide bandwidth bandpass

filter. The mixer is preselected with a double tuned circuit.

An RF amplifier is included in the receiver. We used a circuit left from an earlier effort employing a dual gate MOSFET. A common gate JFET, described in Chapter 6, would be ideal, offering low noise figure with less gain.

12.7 A GENERAL PURPOSE RECEIVER MODULE

This module is essentially the heart of a direct conversion receiver. A TUF-3 diode ring was chosen for improved performance at lower frequency, although the TUF-1 will fit the board. The mixer is followed by an LC low pass filter and an audio amplifier chain using a mixture of bipolar transistors and op-amps. Muting circuitry, an RC active low pass filter, an audio attenuator, and a sidetone oscillator are included on the single board.

The module works very well as a direct conversion receiver. Careful attention to grounding in the early audio stages has eliminated many of the traditional problems encountered, which were described in Chapter 8. The board is sized to fit in a Hammond 1590B box with feed through

capacitors and coax connectors, effectively reducing spurious responses from local VHF signals.

The schematic is shown in Fig 12.40. A low pass filter using a ferrite toroid inductor follows the ring mixer. The one we used was a pre-wound 55-μH part from the junk box, but would ideally use higher inductance with a larger core. An increase in the value of C2 would then improve the low pass filtering. The toroid form is preferred, for it is less susceptible to hum pickup than the other inductors often used. A resistor, R1, provides a termination for sum products exiting the ring mixer.

The audio amplifier begins with a common base stage offering a 50-Ω impedance to the mixer. A degenerated common emit-

ter amplifier, Q3, follows this. At this point the user could exit the board to drive a volume control and/or LC filter. This option is shown in Fig 12.41. The filter is a three element high pass configured to suppress frequencies below 300 Hz. A low pass could be cascaded if desired. We have used the board without this filter. Ideally, the signal after the high pass filter, if used, would exit the enclosure on a feedthrough capacitor. The rest of the circuitry (described below) would then be built on a separate board without shielding.

The first op-amp stage includes a FET switch for receiver muting. An RC active low pass filter, U1b, follows this. This circuit is programmable by the designer/builder. The response of the filter alone

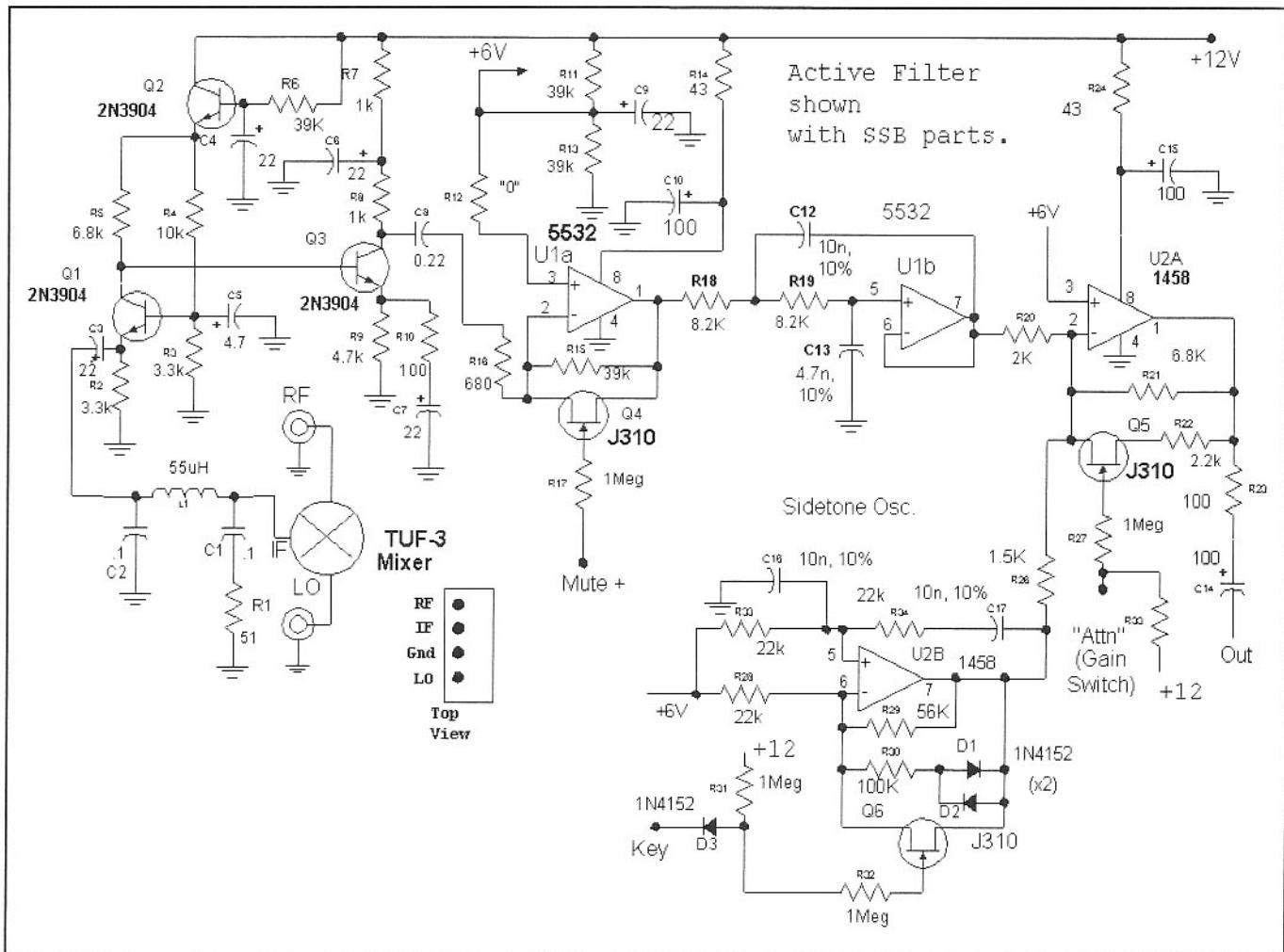


Fig 12.40—General-purpose direct-conversion receiver.

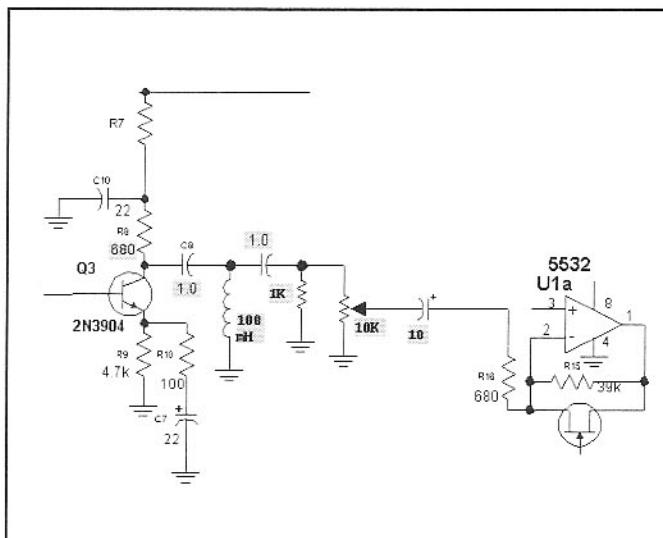


Fig 12.41—Option with an added audio gain control. Also shown is an LC high pass filter. The altered or added components are highlighted.

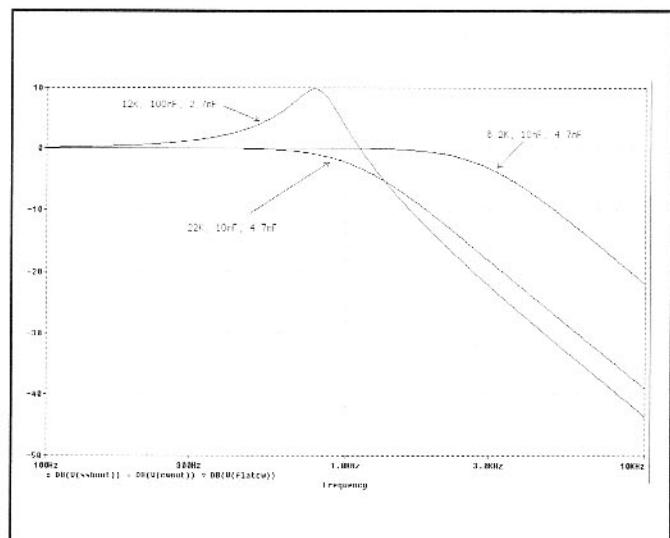
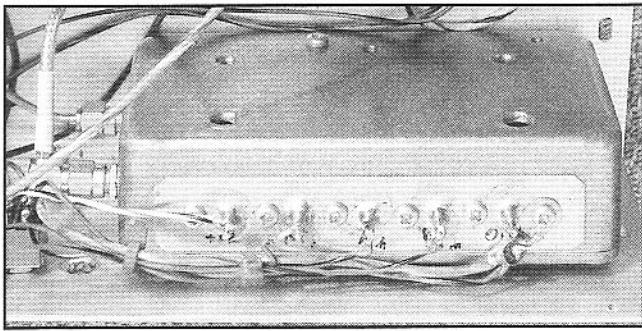
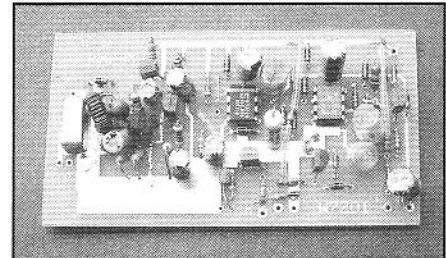


Fig 12.42—Calculated response for low pass filter with three different component value sets.



A shot of the module installed in shielded enclosure. A box built from circuit board would also work well.



General purpose direct conversion module contains a diode ring mixer, audio amplifier, active audio filter, gain programmable active filter, and sidetone oscillator. This board is normally mounted inside a shielded box with coax connectors and feed-through capacitors for all interfaces. Two boards can be used for a binaural receiver.

Table 12.1

General-Purpose Receiver Module—Components for the Low Pass Filter

Bandwidth and Shape	R18 and R19	C12	C13
3 kHz flat	8.2 kΩ	10 nF	4.7 nF
1 kHz flat	22 kΩ	10 nF	4.7 nF
Peak at 700, Q=3	12 kΩ	100 nF	2.7 nF

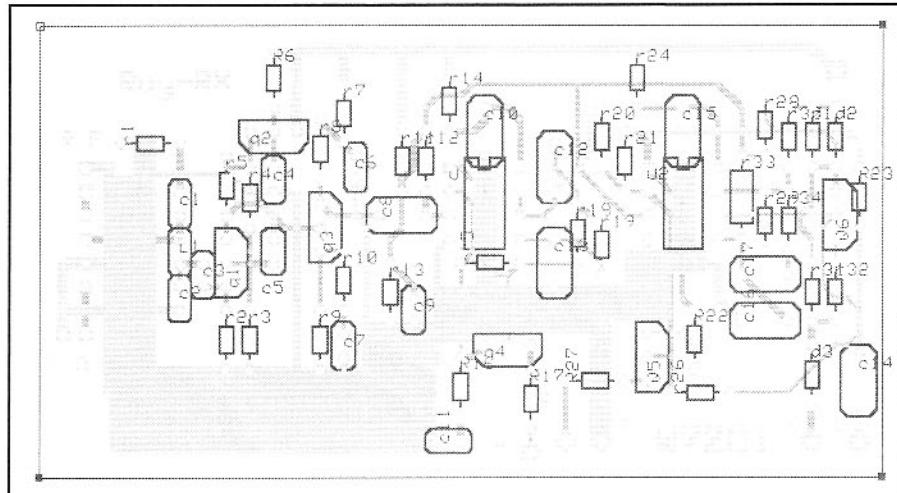


Fig 12.43—View of the component side of the circuit board. Copper runs on both sides of the circuit board are shown. The board layout is double sided, through-hole plated, and was done with the program *Express PCB Version 2.1.1* found at www.expresspcb.com.

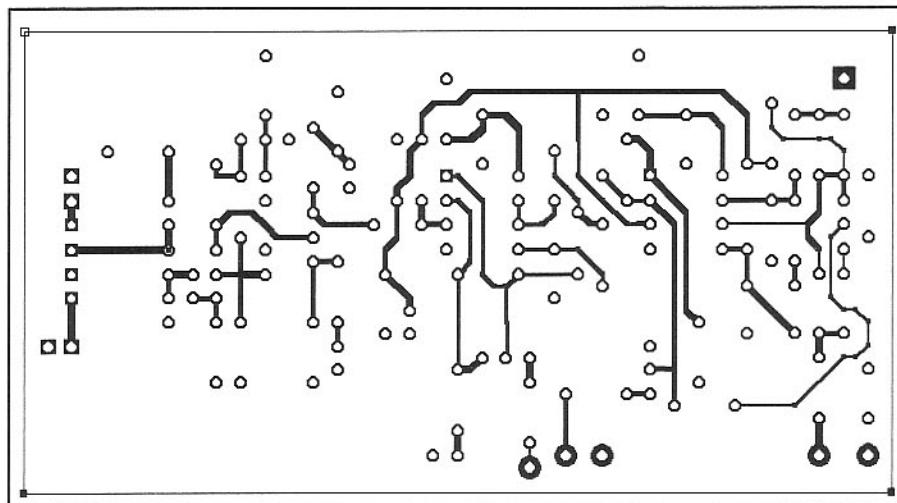


Fig 12.44—This view is identical to that of Fig 12.43, but shows only the runs on the opposite side of the board.

(without the rest of the receiver) is shown in Fig 12.42 for three component value sets summarized in Table 12.1.

An inverting amplifier, U2A, with a gain that can be switched with an external signal, follows the active low pass filter. A 12-dB gain step is available with the components shown. This op-amp has enough output to drive low impedance headphones.

The remaining half of U2 serves as a sidetone oscillator. This Weinbridge topology was used in the “Unfinished” transceiver discussed elsewhere.

There is considerable flexibility available in this design. If a simpler receiver is needed, U1b is capable of driving headphones, allowing U2 to be eliminated. Gain can be programmed in the second audio stage with changes in R10, in U1A through R15 and R16, and in U2A.

We have used these modules in three different receiver types. The first is a simple direct conversion receiver where the circuitry and performance are very much like that of the W7EL classic so long as the board is well shielded and used with a well isolated LO. Second, we have used a pair of these as a binaural receiver.¹⁷ Finally, the board has been a handy “tail end” for several superhet rigs. A pair of the boards could be used to build a phasing receiver, although there is probably too much selective circuitry in the version shown, encouraging a redesign using the guidelines of Chapter 9. The PC board layout used is shown in Figs 12.43 and 12.44. Repeated building of the same design justifies a printed board. The name on the board, “Roy-Rx,” indicates that this is a variation of the Roy Lewallen design from *QST*, August, 1980.¹⁸

12.8 DIRECT CONVERSION TRANSCEIVERS FOR 144-MHZ SSB AND CW

These transceivers were built using prototype circuit boards during the development of the line of products sold by Kanga US. They illustrate different packaging techniques, and also some of the effort that goes into moving from prototype or ugly construction to a commercially available production circuit board. Both transceivers use identical circuitry, and the basic design is intended as a tunable IF for microwave transverters. A wooden box was chosen to investigate the problems that result from having no shielding at all around the circuit boards. The radio works well as a tunable IF, but is subject to hum and noise pickup when directly connected to a nearby, non-directional 2-meter antenna. It works fine on the 2-meter band, however, with a small Yagi 10 meters away, and pointed away from the transceiver. The version built in the gray steel chassis has no shielding between PC boards, but is well shielded from the outside world. It works with a whip antenna, but has some microphonics that are not present in direct conversion rigs with more extensive shielding.

The circuitry is all on three printed circuit boards. The block diagram is shown in Fig 12.45. The miniR2 and T2 PC

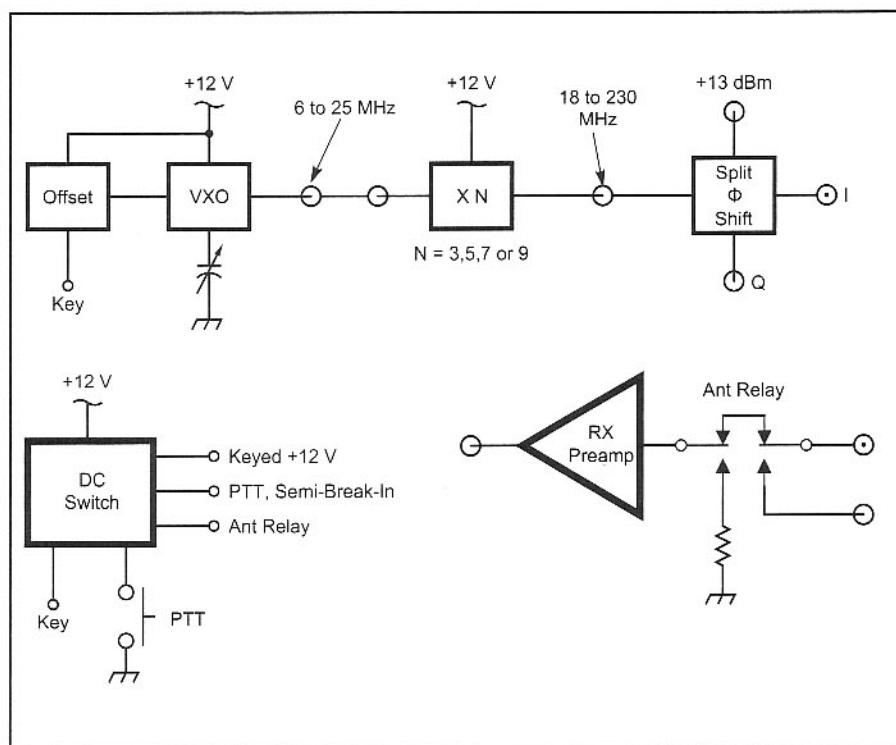


Fig 12.46—Block diagram of LM2 PC board, which contains the VXO, LNA and TR switching circuits.

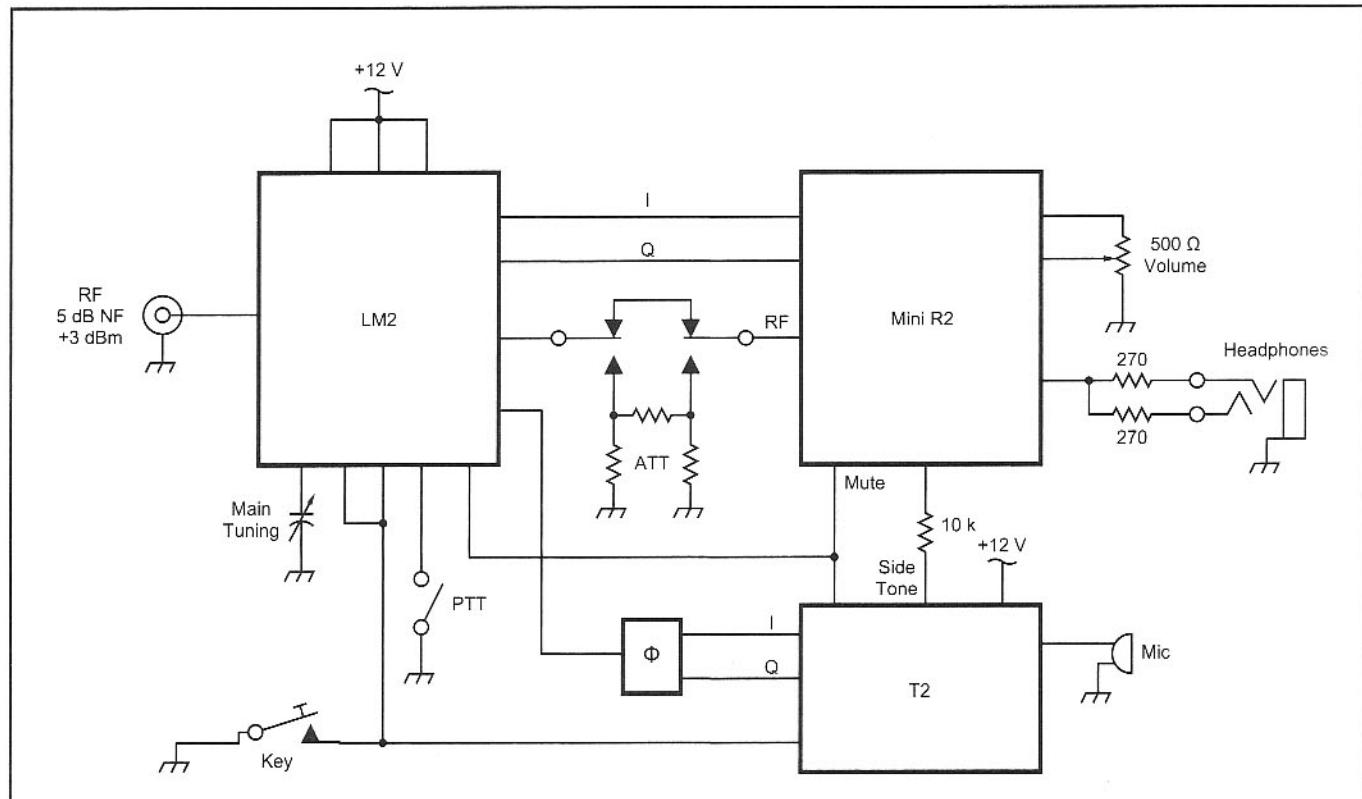


Fig 12.45—Block diagram of direct-conversion 144-MHz SSB/CW transceiver.

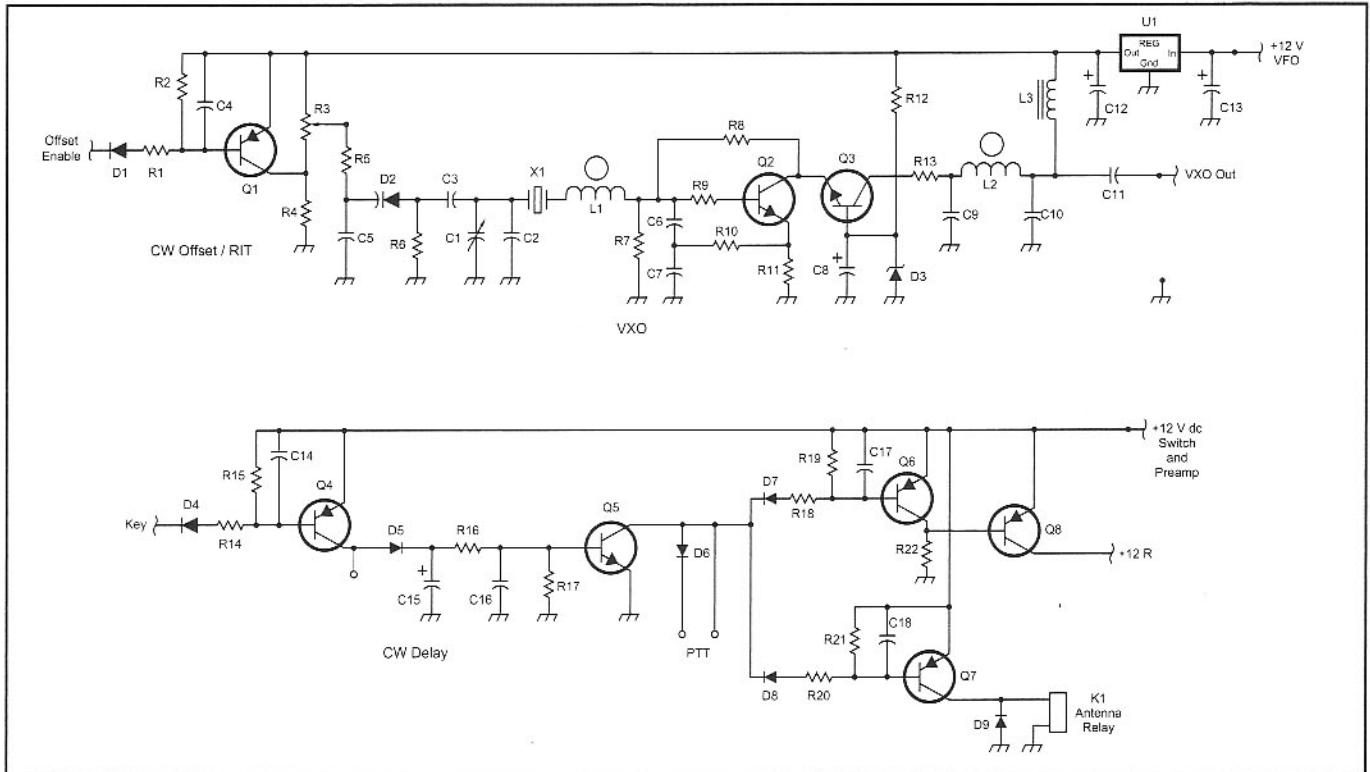


Fig 12.47—LM2 schematic 1.

Fig 12.48—LM2 schematic #2 and parts list.

R1 4.7 kΩ
 R2 10 kΩ
 R3 50 kΩ Trimpot Panasonic 36C series
 R4 47 kΩ
 R5 100 kΩ
 R6 1 MΩ
 R7 10 kΩ
 R8 10 kΩ
 R9 33 Ω
 R10 22 Ω
 R11 510 Ω
 R12 3.9 kΩ
 R13 51 Ω
 R14 4.7 kΩ
 R15 10 kΩ
 R16 4.7 kΩ
 R17 10 kΩ
 R18 4.7 kΩ
 R19 10 kΩ
 R20 4.7 kΩ
 R21 10 kΩ
 R22 10 kΩ
 R23 1 MΩ chip
 R24 120 Ω 1/2 W
 R25 100 Ω chip
 R26 100 Ω chip
 R27 51 Ω chip
 R28 510 Ω
 C1 Approx 40 pF variable Main Tuning. See Text.
 C2 Upper frequency limit or temperature comp. See Text.
 C3 RIT range set. See Text.
 C4 0.1 μF Panasonic V series
 C5 0.01 μF disk ceramic
 C6 See Table 12.3
 C7 See Table 12.3
 C8 10 μF electrolytic

C9 See Table 12.3
 C10 See Table 12.3
 C11 0.01 μF disk ceramic
 C12 4.7 μF tantalum
 C13 10 μF electrolytic
 C14 0.1 μF Panasonic V series
 C15 22 μF tantalum CW semi-break-in delay
 C16 0.1 μF Panasonic V series
 C17 0.1 μF Panasonic V series
 C18 0.1 μF Panasonic V series
 C19 22 pF chip
 C20 0.01 μF chip
 C21 10 μF electrolytic
 C22 See Table 12.2
 C23 See Table 12.2
 C24 See Table 12.2
 C25 See Table 12.2
 C26 See Table 12.2
 C27 See Table 12.2
 C28 See Table 12.2
 C29 0.01 μF chip
 C30 0.01 μF chip
 C31 See Table 12.2
 C32 See Table 12.2
 C33 See Table 12.2
 C34 See Table 12.2
 C35 See Table 12.2
 C36 See Table 12.2
 C37 See Table 12.2
 C38 See Table 12.2
 C39 See Table 12.2
 C40 See Table 12.2
 C41 See Table 12.2
 C42 See Table 12.2
 C43 0.01 μF chip
 C44 See Table 12.2
 C45 See Table 12.2
 C46 See Table 12.2
 C47 See Table 12.2
 C48 See Table 12.2
 L1 VFO range inductor, 33t T37-2 toroid. See Text.
 L2 See Table 12.3
 L3 See Table 12.3
 L4 See Table 12.2
 L5 See Table 12.2
 L6 See Table 12.2
 L7 6 turns FT 25-43 ferrite toroid
 L8 See Table 12.2
 L9 See Table 12.2
 L10 See Table 12.2
 L11 See Table 12.2
 L12 See Table 12.2
 L13 See Table 12.2
 L14 See Table 12.2
 D1 1N4148
 D2 MV2107 or similar tuning diode
 D3 4.7-V Zener
 D4 1N4148
 D5 1N4148
 D6 1N4148
 D7 1N4148
 D8 1N4148
 D9 1N4148
 Q1 2N3906
 Q2 2N3904 or PN5179
 Q3 2N3904 or PN5179
 Q4 2N3906
 Q5 2N3904
 Q6 2N3906
 Q7 2N3906
 Q8 2N3906
 U1 78L09
 U2 78L06
 U3 74AC04
 U4 MAV-11 or MAB-4. See Text.
 U5 Toko splitter
 U6 Toko splitter
 U7 MAR-6
 K1 OMRON 65V-2-H
 X1 Crystal See Text

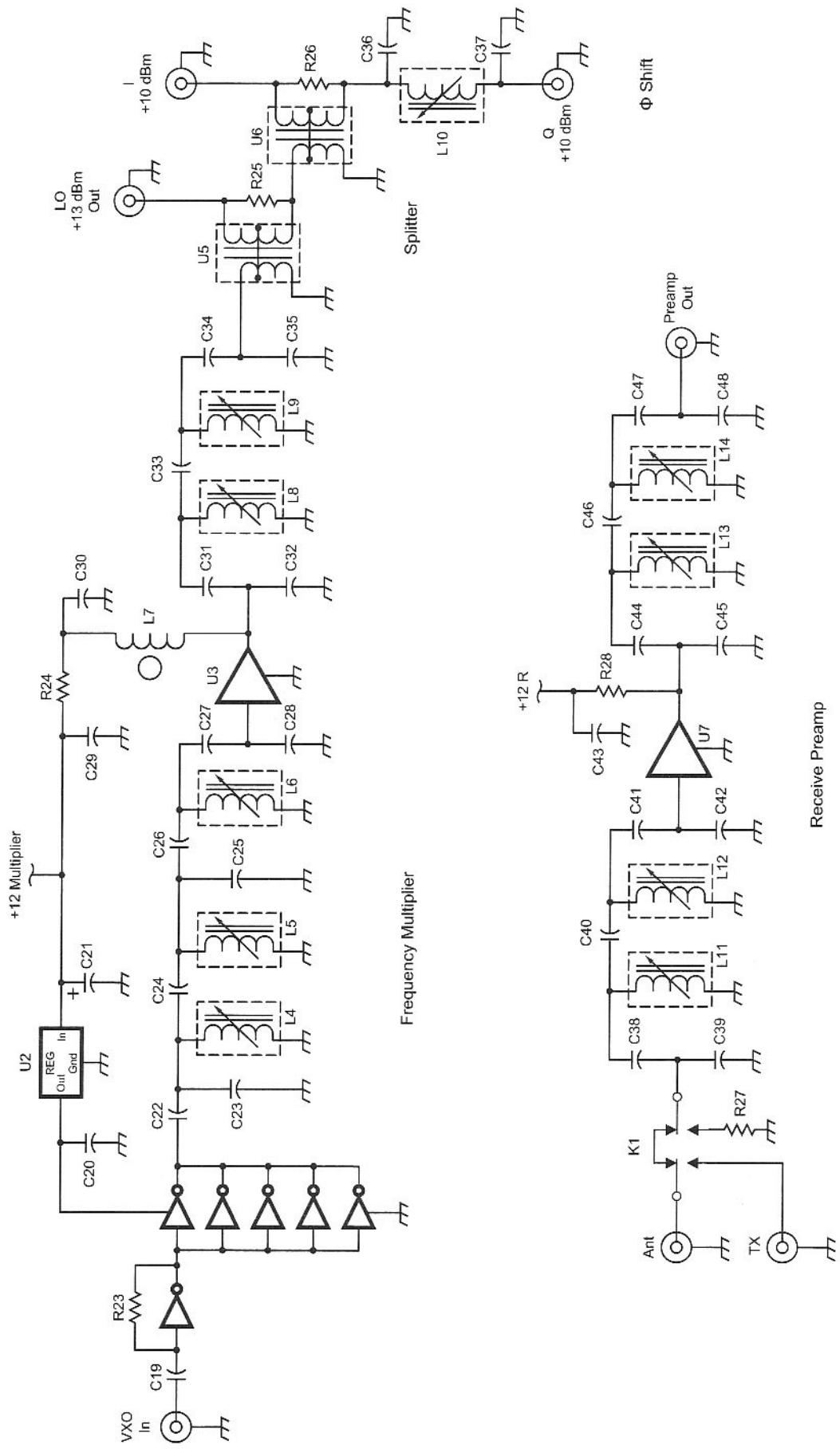


Table 12.2**Filter and Phase Shift Components**

All chip capacitor values are in pF, 1206- or 0805-series Panasonic. All inductor values in nH, MC122- or MC134-series Toko with case.

Component	Frequency (MHz)						
	18	21	24	28	50	144	222
C22	56	56	39	33	20	3.9	3.9
C23	68	68	47	47	22	5.6	3.9
C24, C26, C33, C40, C46	10	10	10	10	5	1	1
C25	120	120	76	68	39	9.1	6.8
C27, C31, C34, C38, C41, C44, C47	180	180	120	120	56	12	8.2
C28, C32, C35, C39, C42, C45							
C48	390	390	270	270	150	47	27
C36, C37	180	150	120	120	68	22	15
L4, L5, L6, L8, L9, L11, L12, L13, L14	422	422	422	350	226	108	53
L10	422	383	350	291	159	53	32

boards have been previously described in *QST*.^{19,20} The LM2 PC board contains the V XO, LNA and TR switching circuits. The

LM2 block diagram is shown in Fig 12.46. Figs 12.47 and 12.48 are the LM2 schematics. In Figs 12.49 and 12.50 you'll see

the wood-boxed transceiver, and Figs 12.51 and 12.52 are the version in the metal chassis.

Table 12.3**V XO Components**

All capacitor values are in pF, Panasonic 100 V C0G, monolithic ceramic. L2 values represent the suggested number of turns on a T37-2 toroid core. Adjust for maximum output across 50Ω. L3 values are in μH using a JW Miller epoxy conformal coated iron core.

Component	Frequency Range (MHz)				
	6-8	8-10	10-15	15-20	20-26
C6, C7	220	220	150	100	82
C9	150	120	82	68	56
C10	680	560	390	330	220
L2	24	21	19	17	16
L3	18	15	12	8.2	6.8

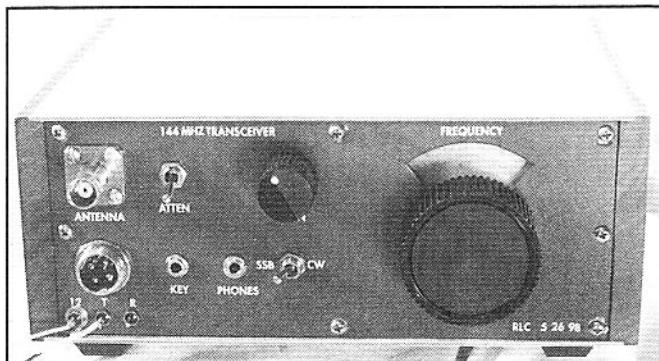


Fig 12.49—Wood Box 144-MHz transceiver.

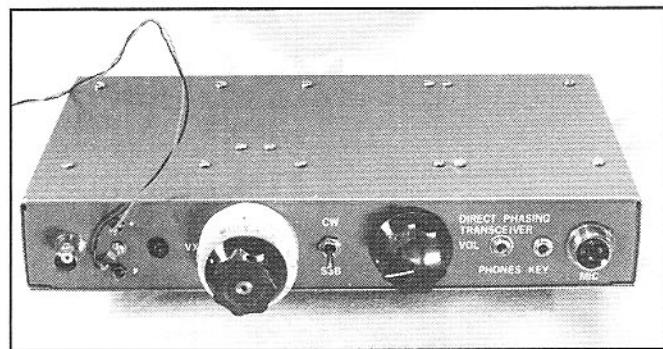


Fig 12.51—The Metal Box 144-MHz transceiver.

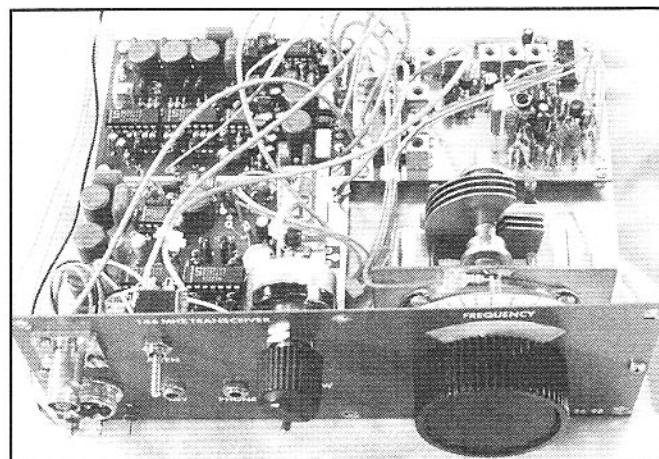


Fig 12.50—An interior view of the Wood Box 144-MHz transceiver.

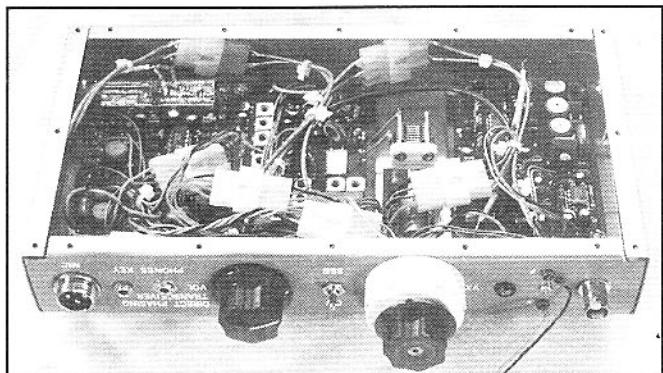


Fig 12.52—An inside look at the Metal Box 144-MHz transceiver.

12.9 A 52-MHz TUNABLE IF FOR VHF AND UHF TRANSVERTERS

This transceiver was designed and built to serve as the base station tunable IF for weak signal SSB and CW DXing on the bands from 222 through 2304 MHz. It is mounted in a large rack-mount box, and is connected to a set of rack mount transverters. A front-panel switch selects the desired transverter. The transverters provide 100-W output on 222 and 432 MHz, 10 W on 903 MHz, 15 W on 1296 MHz and 4 W on 2304 MHz, with less than 2-dB noise figure on each band. 52 MHz was chosen for the IF because it is not harmonically related to any of the desired band segments, and there is no CW or SSB activity near 52 MHz to cause IF breakthrough problems.

Fig 12.53 is a photograph of the IF transceiver in operation, and the block diagram is shown in **Fig 12.54**. Modular construction is used, and each module is mounted in a shield box. The T2 exciter and LO modules are build in boxes soldered up from PC board material; the R2 receiver is

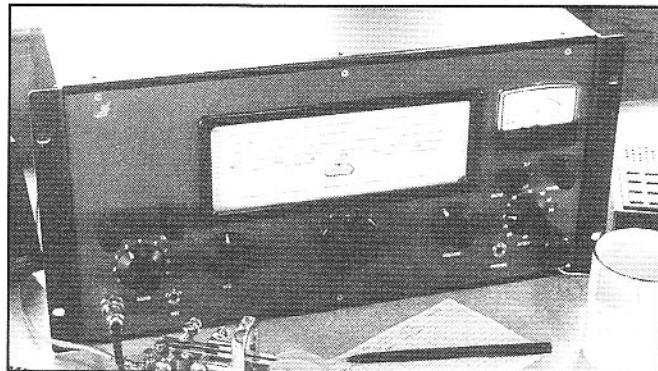


Fig 12.53—The 52-MHz IF transceiver in operation.

in a steel chassis. The filters and preamp are in aluminum boxes with screw-on covers. The receiver and exciter each has its own independent phase-shift network with an air-variable phase trim capacitor, hard-wired directly to the receiver or exciter circuit board.

The LO phase shift adjustments and amplitude trimmer adjustments are accessible on top of the shielded enclosures, but after initial alignment they have remained untouched during the 6 years (and a move half-way across the country) that the rig has been in service. Detailed schematics

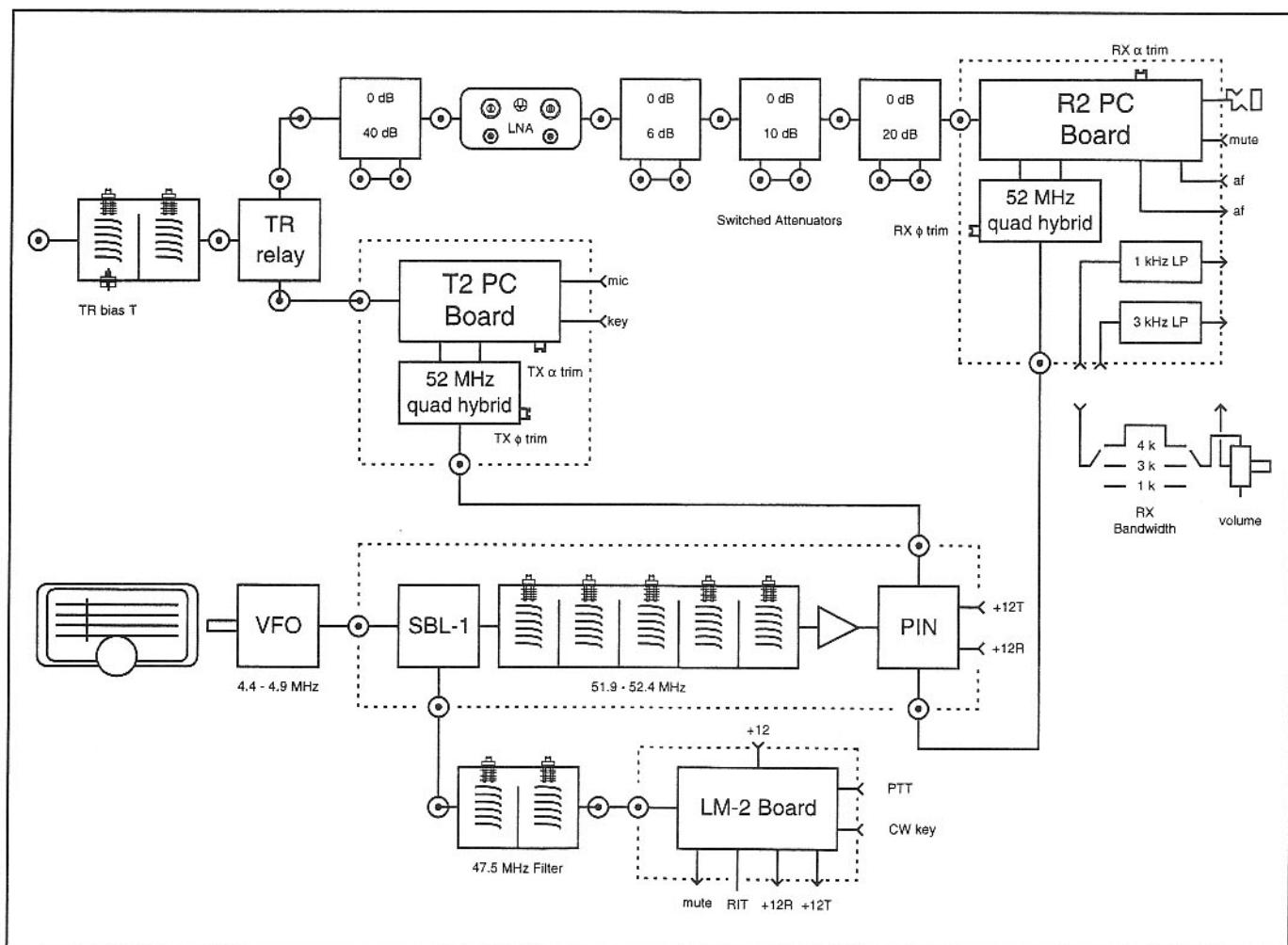


Fig 12.54—52-MHz IF transceiver block diagram.

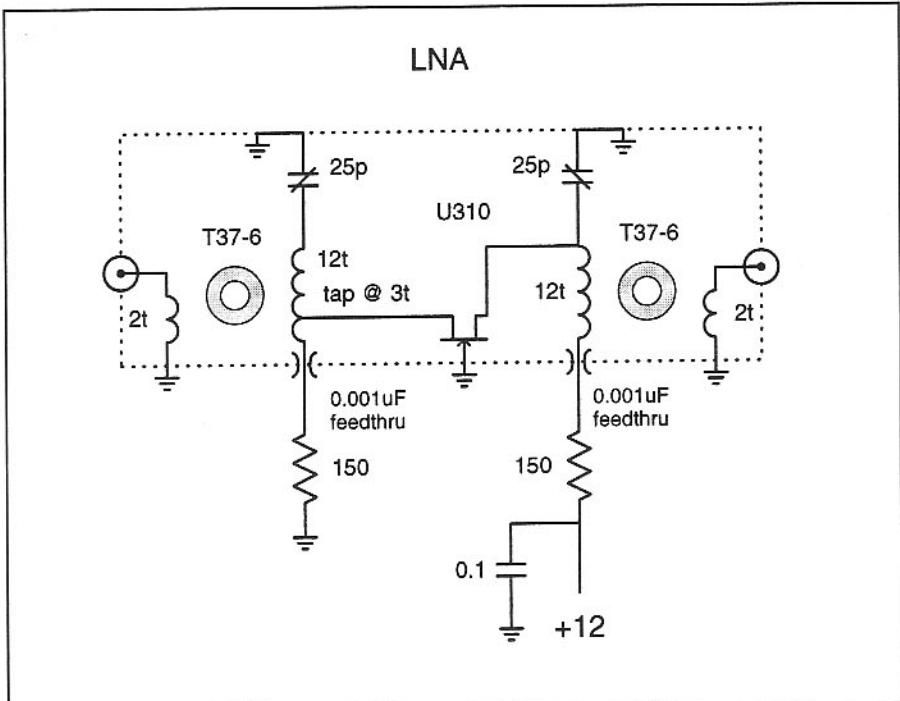


Fig 12.55—LNA schematic.

of each of the circuit blocks are shown in Figs 12.55 through 12.61. Figure 12.62 is a close-up of one of the LO phase-shift networks, illustrating the mechanical and electrical symmetry and connection of the phase-trim capacitor. Figure 12.63 is a view of the 52-MHz filter. Figure 12.64 is a look under the hood, and Fig 12.65 is a bottom view, showing much of the circuitry.

The Local Oscillator system is pre-mixed from the 4-MHz range up to 52 MHz. A 5-section helical resonator filter selects the 52-MHz product, rejects the 44-MHz image, and provides additional attenuation of the 48-MHz premix oscillator. The output tunes from 51.9 MHz to 52.4 MHz, and the vintage Eddystone Dial provides a smooth, slow tuning rate and may be reset to within 1 kHz.

This IF transceiver was built to replace a commercial 6-meter rig being used as a tunable IF in a competitive VHF contest station. The commercial rig had a few spurs and birdies, and synthesizer noise burbles that sounded like weak signals

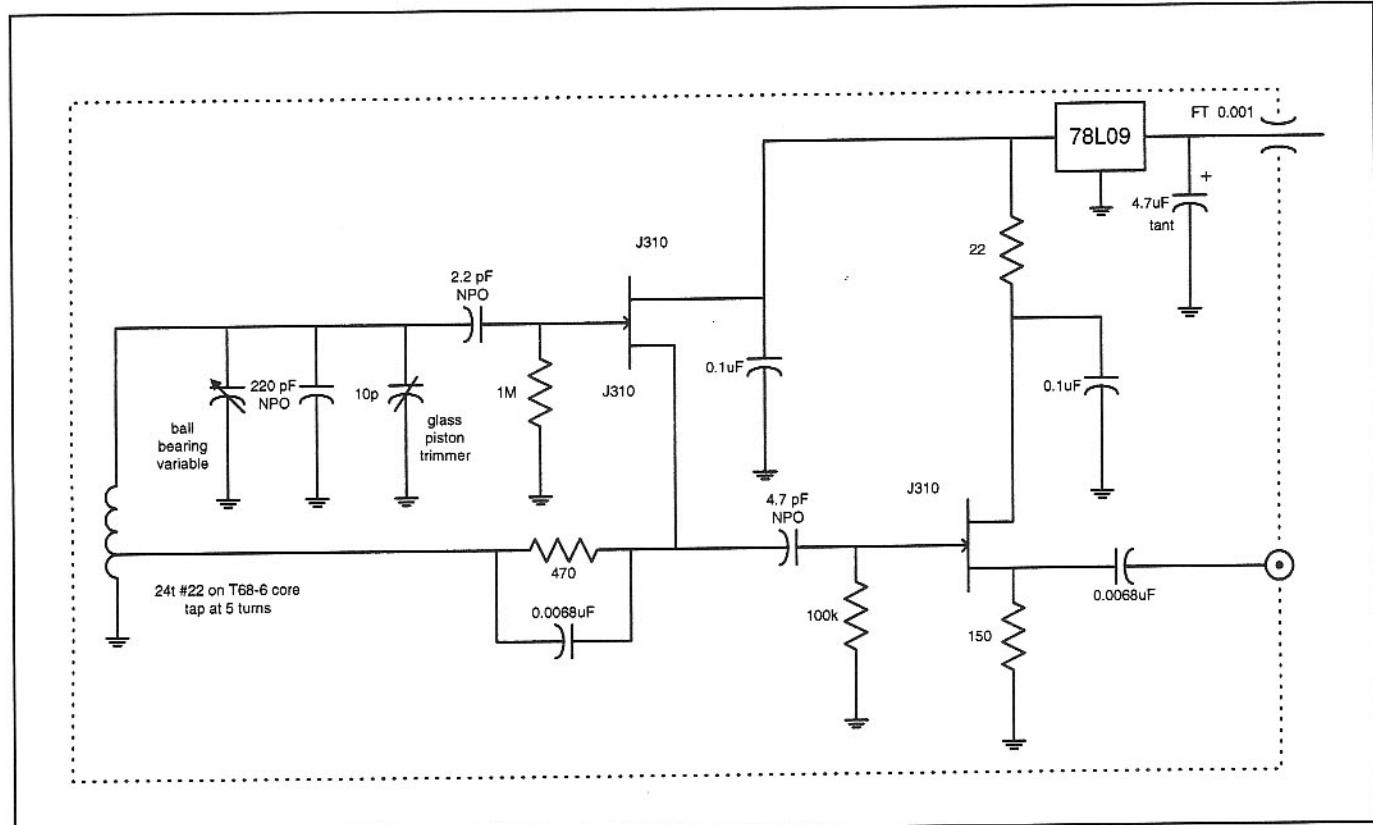
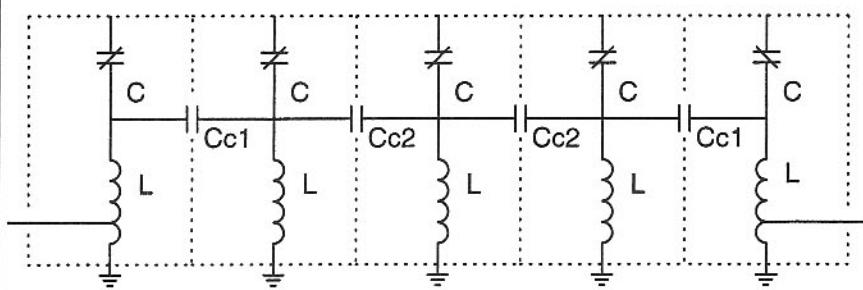


Fig 12.56—The 4.4-4.9 MHz VFO schematic

52-MHz center freq. 2 MHz Bandwidth 1 dB loss LO Premix filter



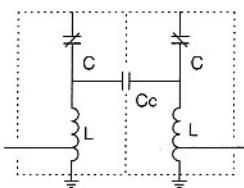
All L 10T 0.50" i.d. 1.00" long bare number 18 copper
in and out taps 1 full turn from ground end
C 50 pF air variable
Cc1 0.32" gimmick twisted #22 Teflon Covered
Cc2 0.25" gimmick twisted #22 Teflon Covered

Fig 12.57—Schematic of the 52-MHz premix filter.

when tuning for UHF DX. In addition, the audio distortion of the commercial radio contributed to operator fatigue over the course of a weekend contest. The home-

Brew 52-MHz transceiver has no spurious responses or birdies, and all undesired outputs are more than 70 dB below the desired output.

47.5-MHz center freq. filter



L 10T 0.50" i.d. 0.75" long bare number 18 copper
in and out taps 1 full turn from ground end
C 50 pF air variable
Cc 0.25" gimmick twisted #22 Teflon Covered

Fig 12.58—The 47.5-MHz premodulator filter.

Modular construction with individual shielded modules, and a spacious cabinet, contributes to a very large piece of radio equipment with fine performance.

This 52-MHz tunable IF is a "work in progress," with unfinished audio gain control, metering, and mode selection functions. It has been in service for 6 years, and every year or so a function will be added. There is ample room inside for additional circuit modules, and room on the front panel for additional controls.

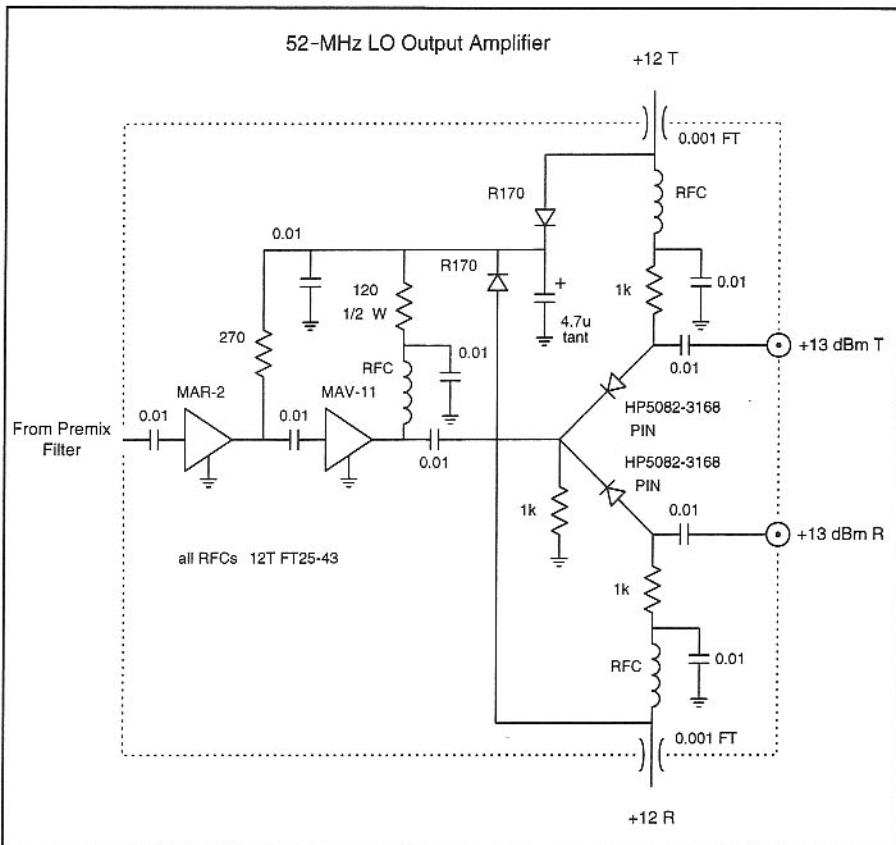


Fig 12.59—The 52-MHz premix LO output amplifier.

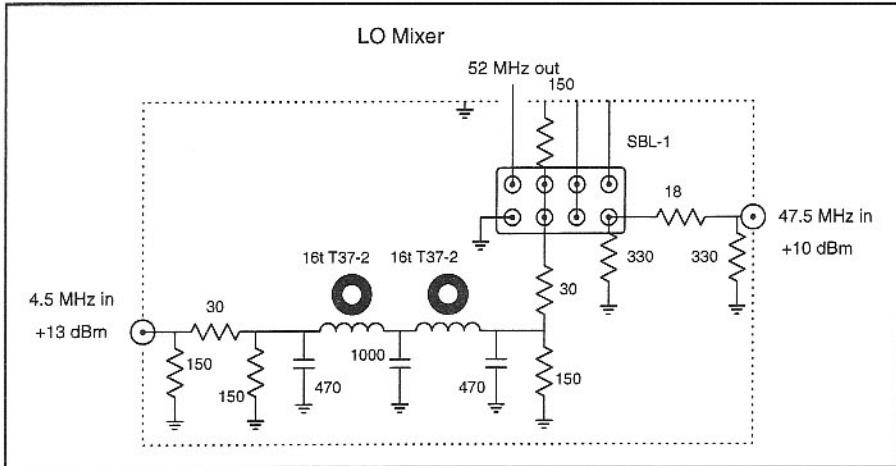


Fig 12.60—Schematic of the premix LO mixer.

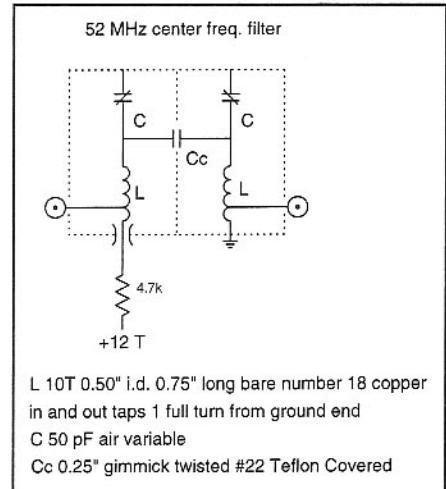


Fig 12.63—The 52-MHz filter.

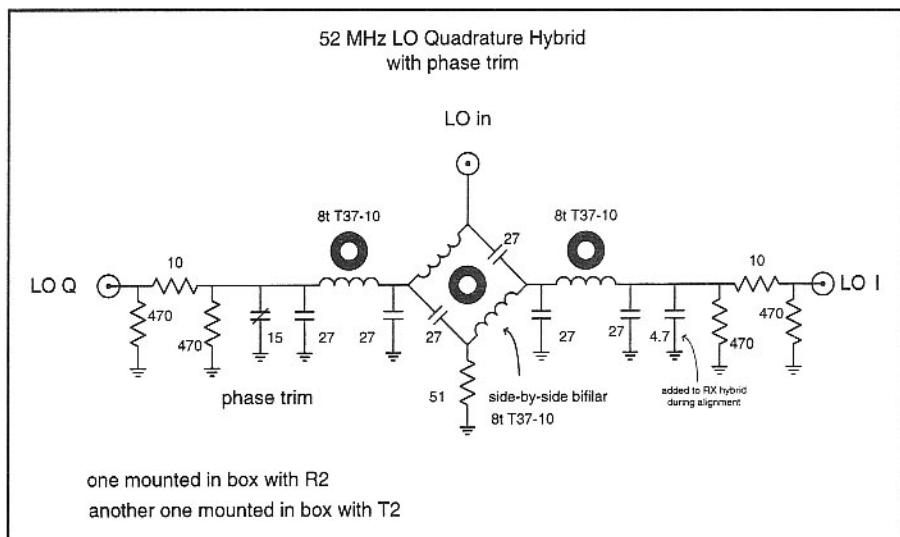


Fig 12.61—Schematic of the 52-MHz LO quadrature hybrid.

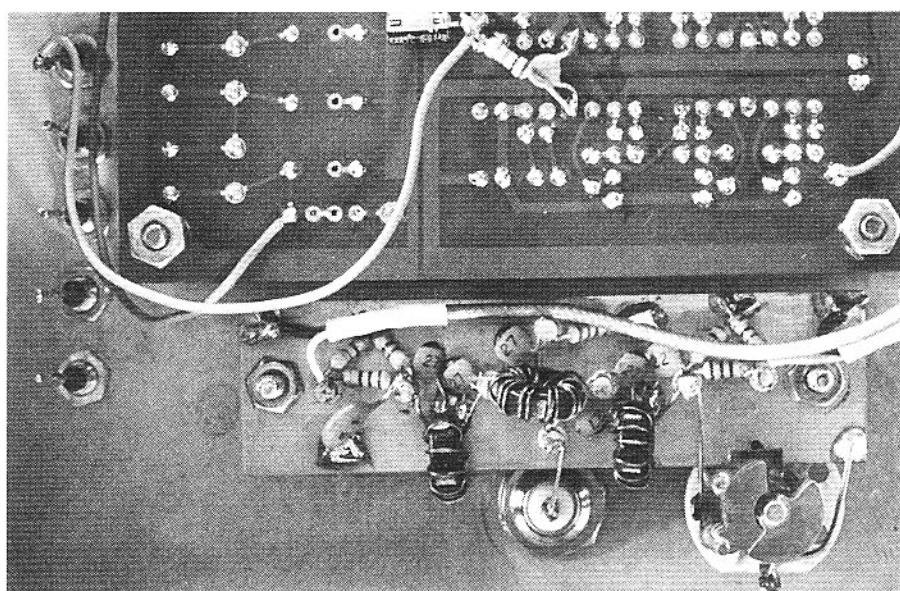


Fig 12.62—Close-up of LO quad-rature hybrid.

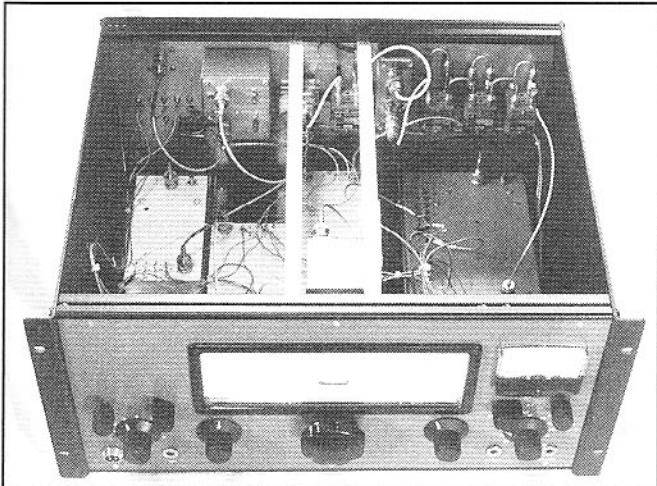


Fig 12.64—A peek at the inside top of the 52-MHz transceiver.

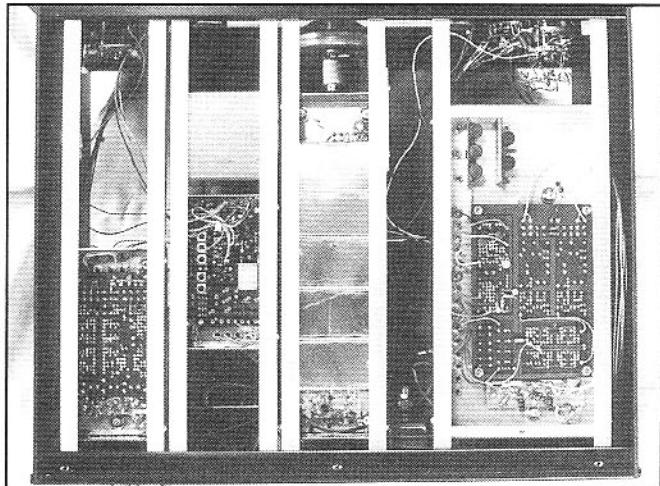


Fig 12.65—The inside bottom of the 52-MHz transceiver.

12.10 SLEEPING BAG RADIO

On winter camping trips in the Northwest and Michigan's Upper Peninsula, radio operation typically occurs at night, while snuggled deep inside a warm sleeping bag. This is a different environment that

completely changes the usual ergonomics of a radio. This 40-meter CW transceiver is designed to sit on either its back or bottom, with all connections and controls on the front/top. It is stable in either position. The controls are kept to a minimum, with a large, stiff tuning knob, a volume control, and RIT. CW is full break-in, and the use of a keyed receiver LNA along with conventional receiver muting eliminates any receiver thumps during keying. The radio is built in two die-cast boxes screwed together, with feedthrough capacitors to carry the signals and power into the back compartment. The back compartment contains an interchangeable receiver circuit board, which may be either an R1 direct conversion receiver, a mini-R2 receiver, or a binaural receiver. This radio has a solid

feel to it, and is heavy enough that it is unwelcome on a weeklong summer trek through the backcountry—but for a short overnight jaunt on snowshoes it is ideal. The tuning knob is large enough to tune with mittens, and stiff enough that it doesn't move when bumped.

The four photographs in Figs 12.66 through 12.69 illustrate the construction. **Figure 12.70** illustrates how the receiver compartment is double shielded from the outside world. All connections into the receiver compartment are made using $0.001 \mu\text{F}$ feedthrough capacitors into the VFO/PA compartment. **Figure 12.71** is a block diagram. The VFO/frequency doubler is shown in **Fig 12.72**, the PA, using a high-gain differential amplifier driving a 5-W CB power transistor is

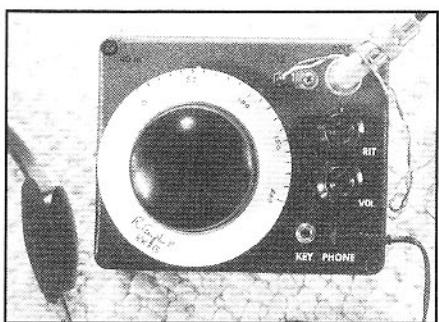


Fig 12.66—The Sleeping Bag Radio.

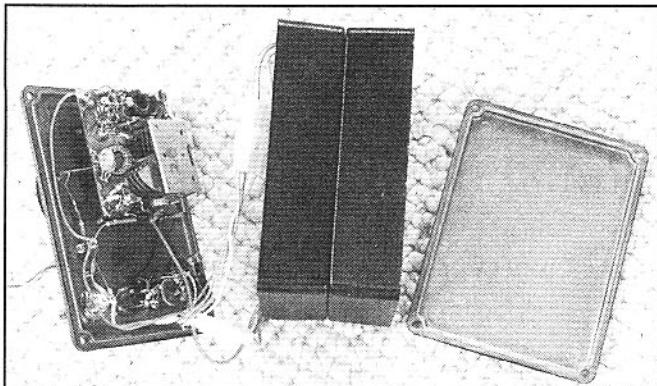


Fig 12.67—Sleeping Bag Radio VFO.

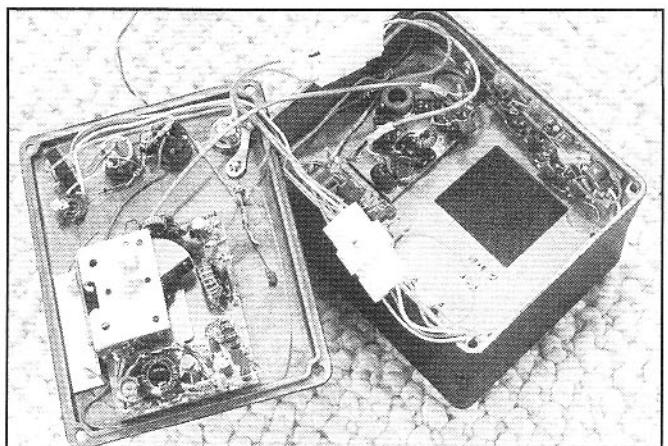


Fig 12.68—The PA compartment.

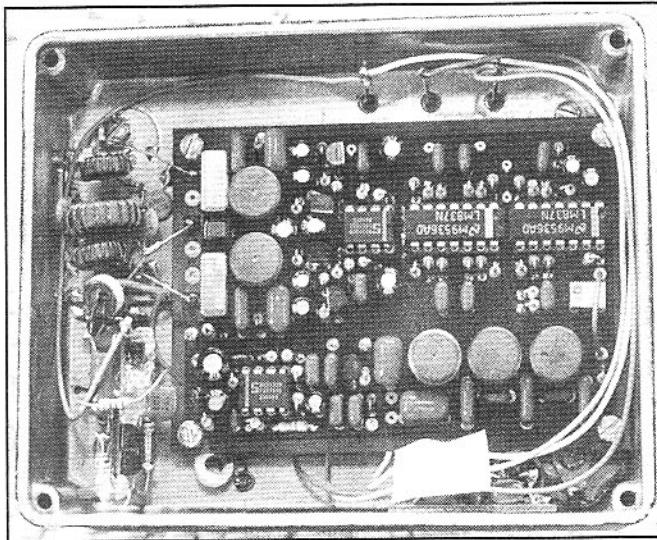


Fig 12.69—The
Sleeping Bag
Radio receiver
compartment.

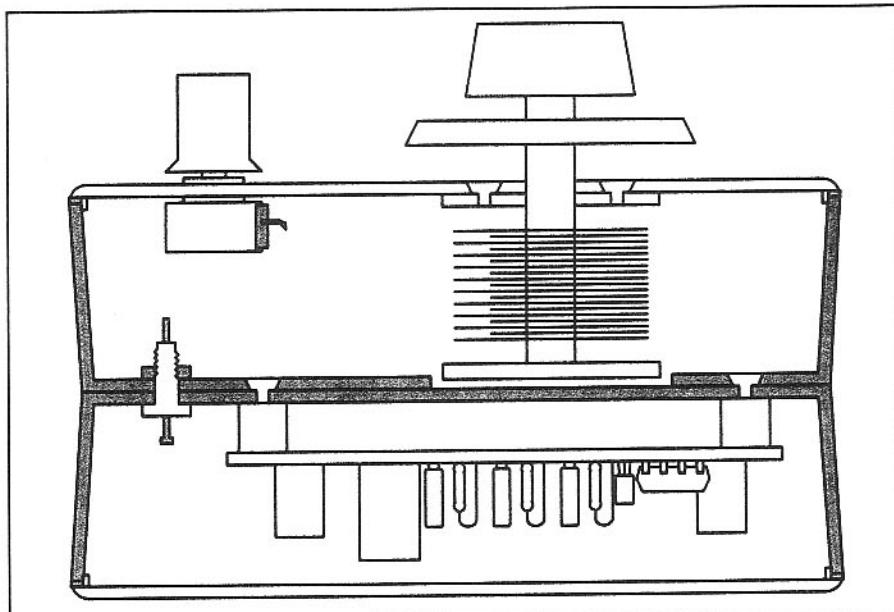


Fig 12.70—A Sleeping Bag Radio construction sketch.

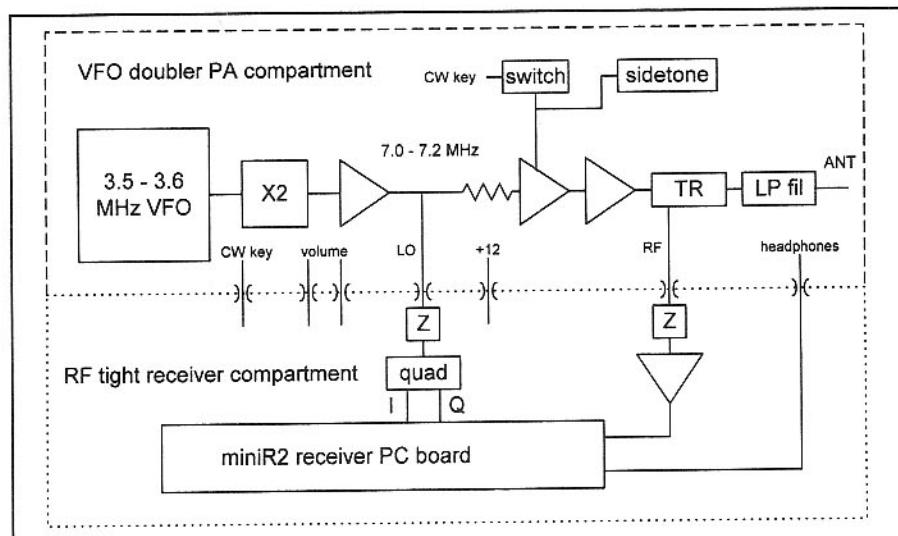


Fig 12.71—Block diagram of the
Sleeping Bag Radio.

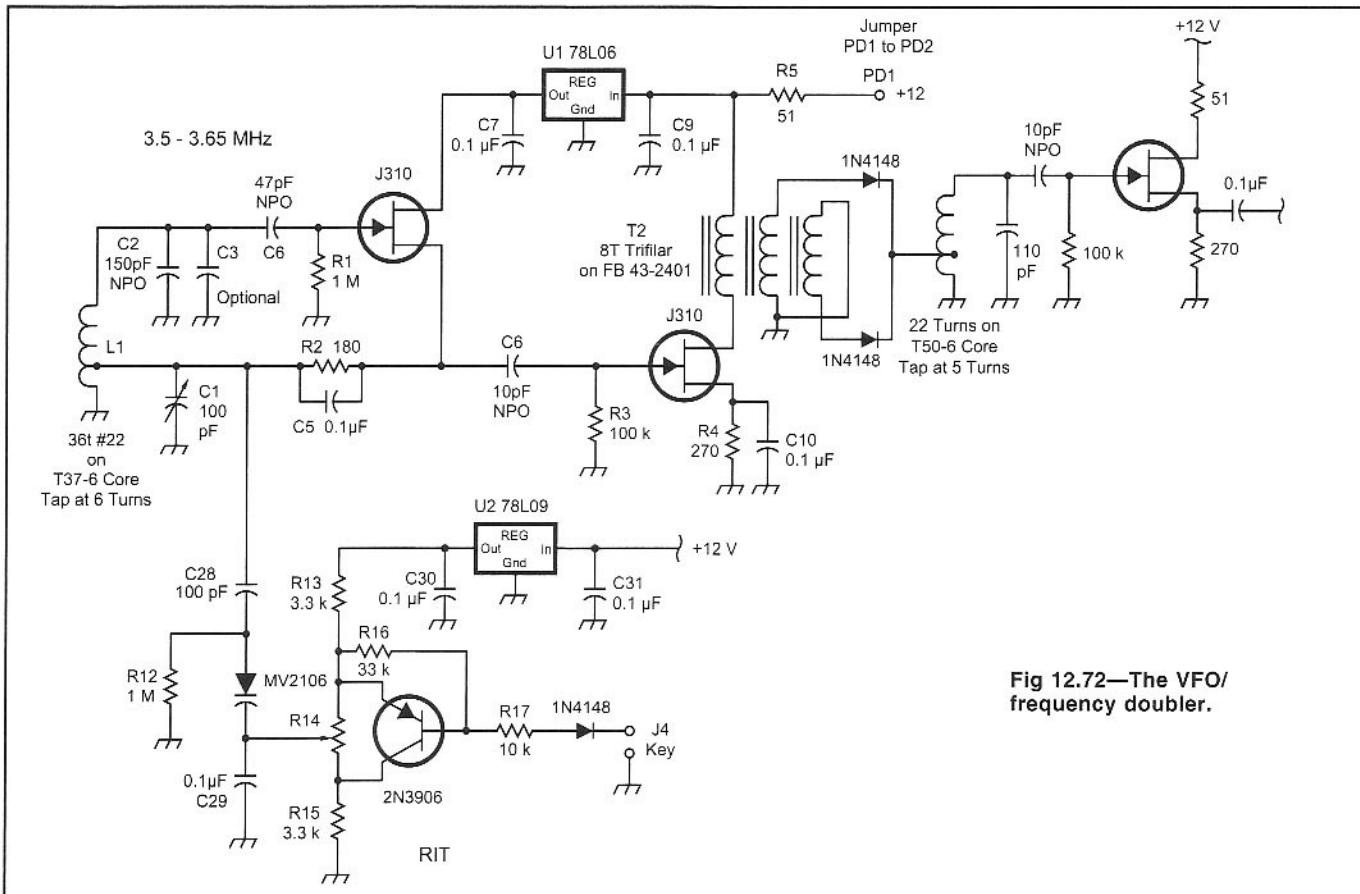


Fig 12.72—The VFO/
frequency doubler.

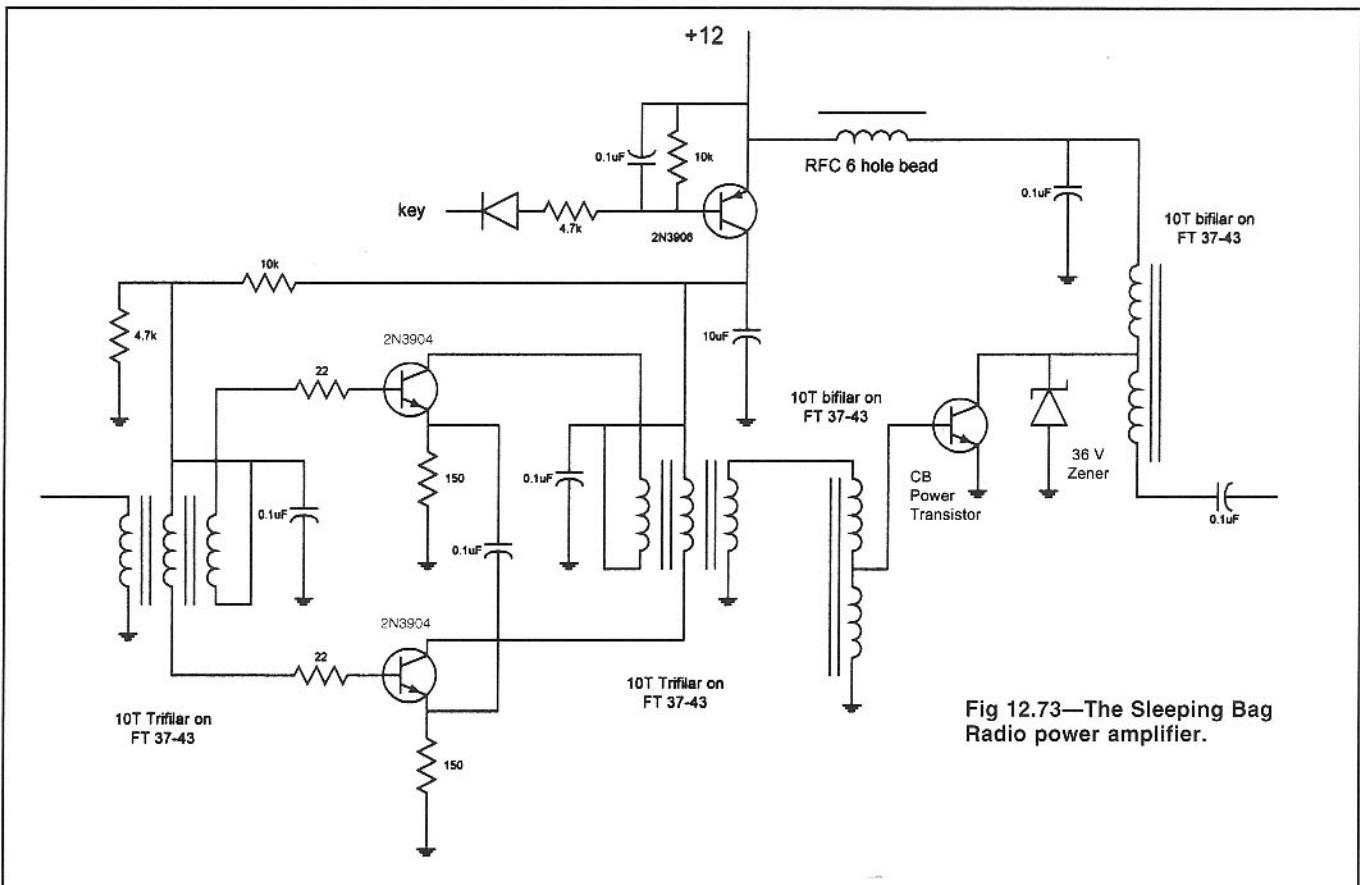


Fig 12.73—The Sleeping Bag
Radio power amplifier.

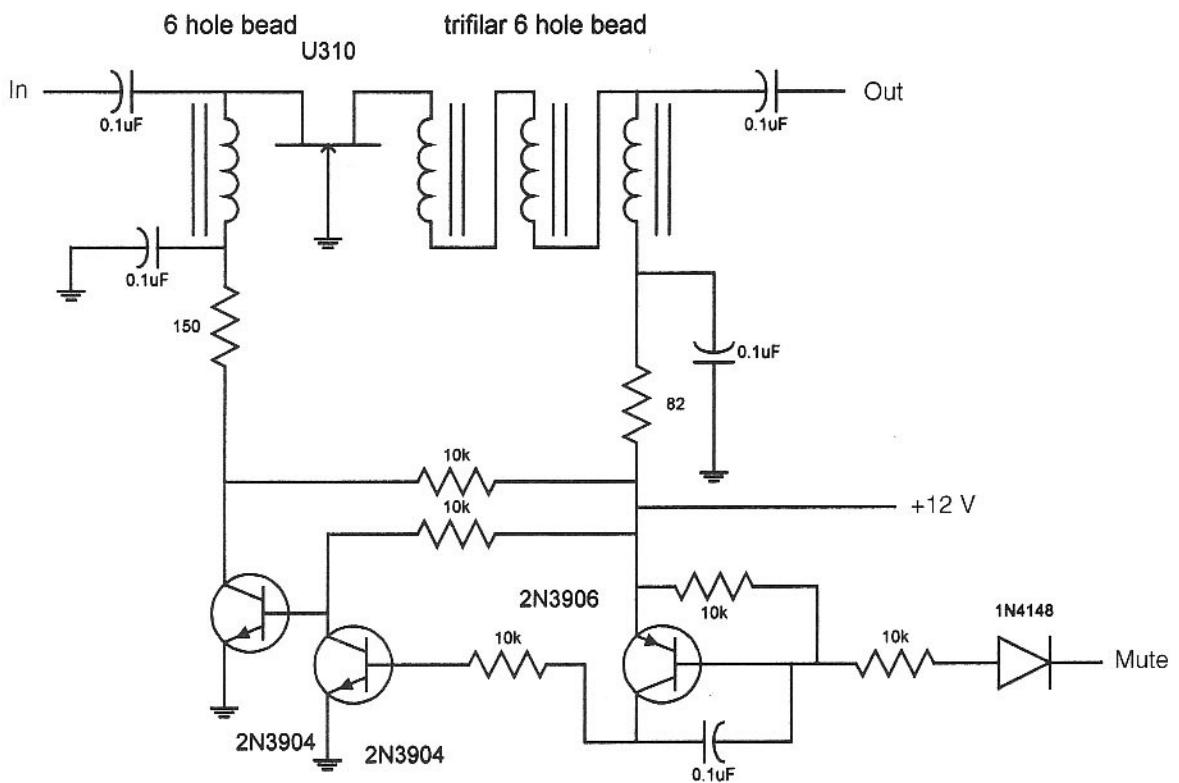
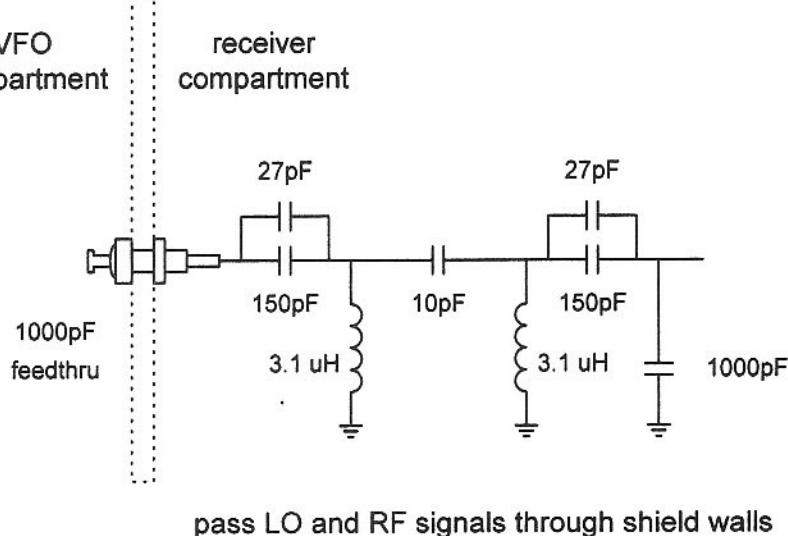


Fig 12.74—The LNA/attenuator.

shown in Fig 12.73, and the LNA/attenuator is shown in Fig 12.74. The 7-MHz RF and LO signals are routed through the shield walls on the feedthrough capacitors using the bandpass networks shown in Fig 12.75. This is the best CW transceiver I have ever used.



High attenuation to FM and AM Broadcast Signals and Harmonics

Fig 12.75—The 7-MHz bandpass feedthrough filter used in the Sleeping Bag Radio.

12.11 A 14-MHZ CW RECEIVER

This is a simple home station receiver for the CW portion of the 20-meter band. It uses R2pro circuit boards and a Kanga UVFO universal VFO board, along with lightweight aluminum chassis construction. **Fig 12.76** is a construction sketch, and **Fig 12.77** is a block diagram. The R2pro receiver circuit boards are described in detail in Chapter 9. **Fig 12.78** is a schematic of the UVFO board. **Figs 12.79, 12.80** and **12.81** illustrate the con-

struction. There are two selectable bandwidths and front-panel muting for use with a small QRP transmitter or vintage 40-W tube transmitter. Appearance and controls are basic. Performance is uncompromising, with over 50 dB of opposite sideband

suppression, 9-dB noise figure, a slow tuning rate, 80 dB between the receiver noise floor and onset of audio clipping, 92-dB SSB bandwidth two-tone third-order dynamic range, and absolutely no spurious responses or synthesizer noise.

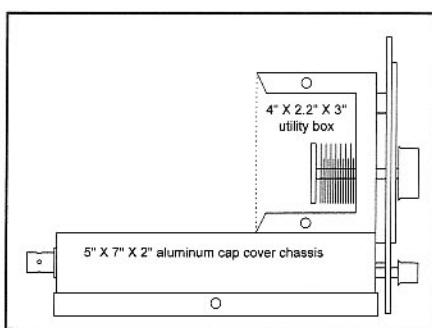


Fig 12.76—A construction sketch of the 14-MHz R2pro.

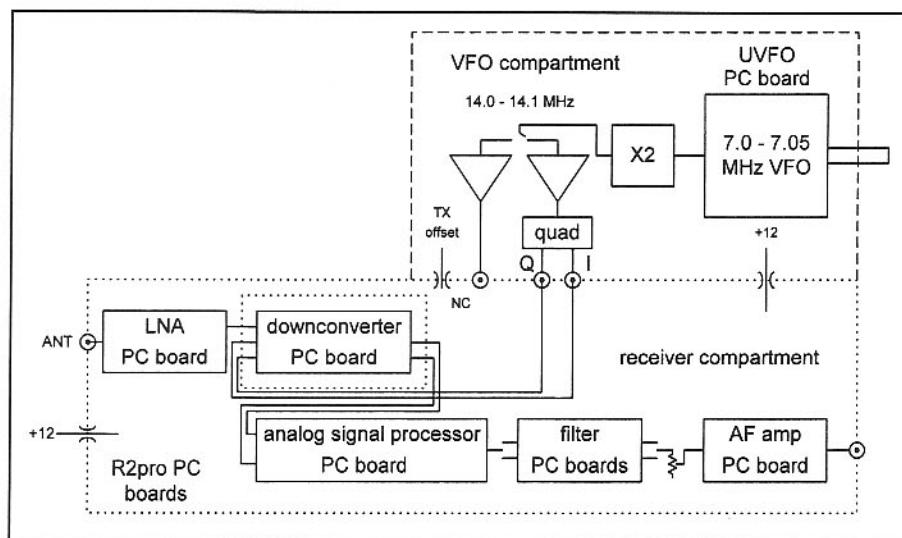


Fig 12.77—The 14-MHz R2pro block diagram.

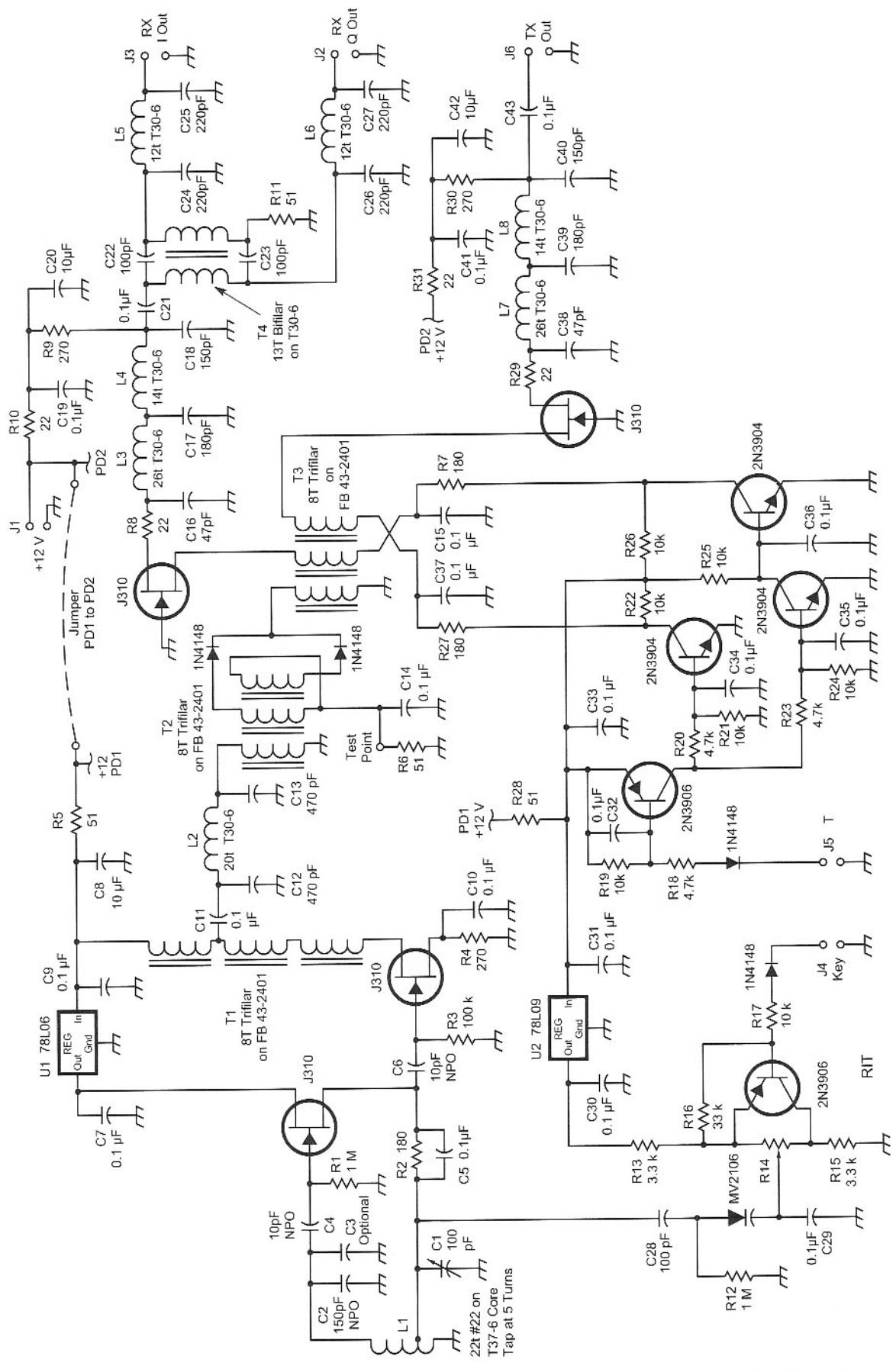


Fig 12.78—14 MHz UVFO schematic.

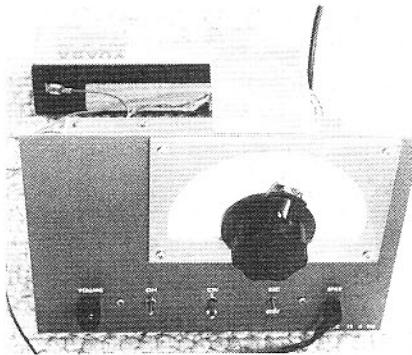


Fig 12.79—14 MHz R2pro front view.

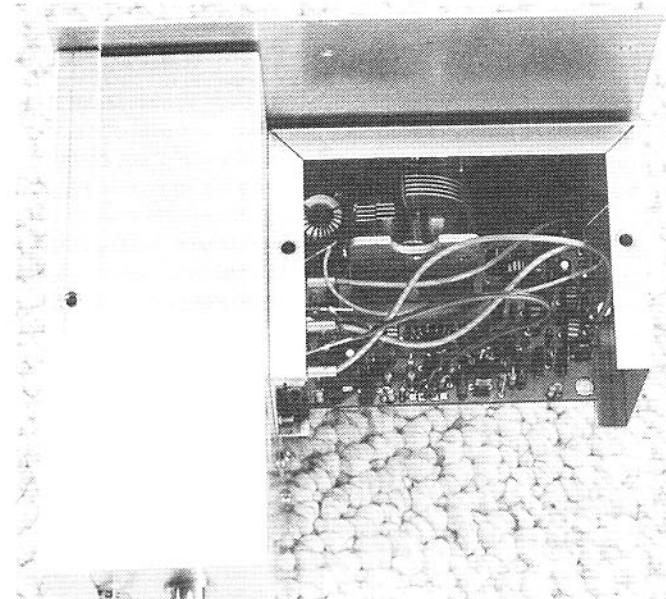


Fig 12.80—
The UVFO.

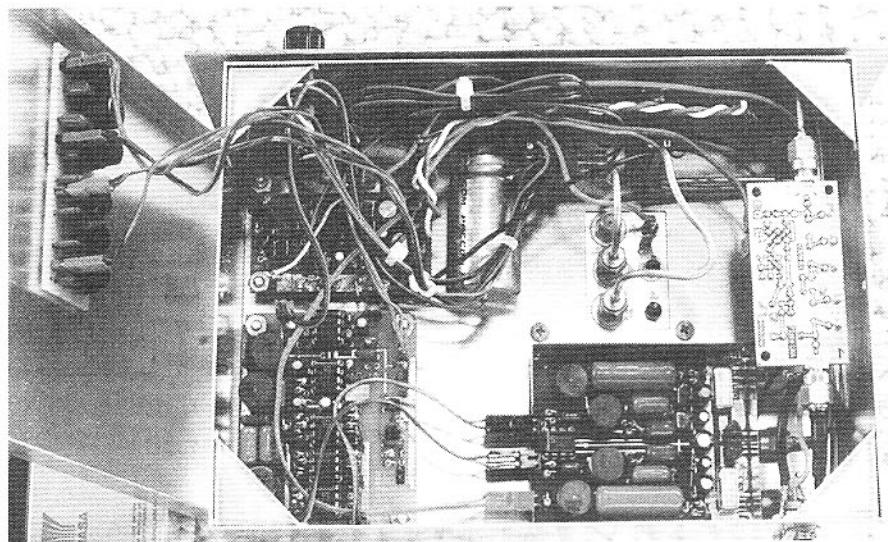


Fig 12.81—The R2pro circuit boards.

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5. W. Hayward, "Measuring and Compensating Oscillator Frequency Drift," *QST*, Dec, 1993, pp 37-41.
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8. Detailed operation of the various weak-signal modes is described in the file README20.TXT. The source code, in 'C', for these modes is primarily in the files U_CODE.C, UMATRIX.C and MOONSUN.C. The specification for the 'PUA43' code is in the file PUA43_02.ZIP. All of these files are included on the CD-ROM.
9. Different countries have different restrictions on the amateur use of data modes. For US amateurs, a short summary of the interpretation of FCC regulations on these matters is the sidebar by Paul Rinaldo, "Is Hellschreiber Permissible Under Part 97?", *QST*, Jan, 2000, p 54. Before using any mode on the air, it is important to determine the legality of its usage and the frequencies that are allowable.
10. V. Poor, "R9/S1," *QST*, Oct, 1965, pp 33-37. This was not the introduction of these ideas, but it is a good summary of the amateur experimenter art of the time.
11. The advantages of multi-tone keying, along with historic background is in the article by M. Greenman, "MFSK for the

- New Millennium," *QST*, Jan, 2001, pp 33-36.
12. Interested readers might start their exploration for further information with the "Matched Filter" topic in books such as D. K. Barton, *Radar System Analysis*, Prentice-Hall, Englewood Cliffs, NJ, 1964.
13. D. Turrin, and A. Katz, "Earth-Moon-Earth (EME) Communications," *The ARRL UHF/Microwave Experimenters Manual*, ARRL, 1990, Chapter 10.
14. Urban dwellers might quarrel with this statement, since coherent "birdies" coming from the all pervasive electronic gadgetry in people's houses will make extended integration times frustrating! EME-2 includes provisions for randomizing the transmitting frequency effectively to shift the interfering signals around, making them noise-like. This prevents the interference from adding in any particular bin but does not remove the equivalent noise power that is added.
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CD-ROM Contents

The material contained on the CD-ROM packaged on the inside back cover of this book contains articles, reference material, and software. This material is organized in the following directories:

\software
\articles
\dsp

The \dsp directory contains specific lists of material for the DSP programs in Chapters 10 and 11 and the DSP-10 2-meter transceiver project.

ARTICLES AND REFERENCES

All of the following articles and references are on the CD-ROM in Adobe Acrobat PDF format. Double-click **articles.pdf** to access a summary of these materials. Alternatively, open any PDF document in the \articles directory to access that specific article. The article filename on the CD-ROM is shown after each reference listing.

While the Adobe Acrobat Reader program used to view the articles and references is normally run directly from the CD, there is a copy included on the CD-ROM that you may optionally choose to install on your hard disk for viewing other PDF files.

To Install Acrobat Reader for Windows:

- 1) Close any open applications and insert the CD-ROM into your CD-ROM drive.
- 2) Select **Run** from the **Windows Start** menu.
- 3) Type **d:\Acrobat\setup** (where **d:** is the drive letter of your CD-ROM drive; if the CD-ROM is a different drive on your system, type the appropriate letter) and press **Enter**.
- 4) Follow the instructions that appear on your screen.

To Install Acrobat Reader for the Macintosh:

- 1) Close any open applications and insert the CD-ROM into your CD-ROM drive.
- 2) Open the "Experimental Methods in RF Design CD" icon on the desktop, then double-click the "Acrobat Reader" icon.
- 3) Double-click the "Acrobat Reader Installer" icon.
- 4) Follow the instructions that appear on your screen.

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SOFTWARE

- LAPDAC-2002, Design programs for Windows. Run **setup.exe** and follow the on-screen directions to install the software.
- Analysis of mixing with a JFET (Mathcad file **mixer_jfet1.mcd**, Adobe Acrobat file **mixer_jfet1.pdf**). See Chapter 5, section 1. Using **mixer_jfet1.mcd** requires Mathsoft *Mathcad* version x.x or higher. **Mixer_jfet1.pdf** is compiled from screenshots showing the equations used in the *Mathcad* file, useful for those who don't have *Mathcad*.

DSP (DIGITAL SIGNAL PROCESSING) Programs for Chapters 10 and 11

The programs for Chapters 10 and 11 are in the directories CHAP10 and CHAP11. For each **c1xxx.dsp** file there is also a **c1xxx.exe** file created by the **ld21** linker as described in **read.txt**. The contents of the two directories are:

CHAPTER 10

- c1shell.dsp** Basic DSP structure for EZKIT- Lite
c1shell.exe
c1sin.dsp Generates single sine wave at 1000 Hz
c1sin.exe
c1sin2.dsp Generates 2 sine waves at 700 and 1900 Hz
c1sin2.exe
c1spn.dsp Generates 1000 Hz sine wave plus Gaussian noise
c1spn.exe
c1fir.dsp FIR filter coefficients
c1fir.exe
fir200bp.dat Part of **c1fir.dsp** - Band pass FIR filter coefficients
firdsn3.bas A QBASIC program for calculating FIR filters using the Kaiser window method.

CHAPTER 11

- c1knob.dsp** Interaction with a rotary knob, switches, LCD display
c1knob.exe

c1tbox.dsp Uses the c1knob to generate 2 sine waves plus noise
c1tbox.exe

c18.dsp An 18 MHz I-Q transceiver for CW and USB

c18.exe

lp2_8.dat Part of **C18.dsp** - Low pass FIR filter coefficients

lp_5_48.dat Part of **C18.dsp** - Low pass FIR filter coefficients

bpcw1.dat Part of **C18.dsp** - CW audio FIR filter coefficients

hil_3_48.dat Part of **C18.dsp** - Hilbert transform for 90 degree phase shift. These are coefficients for a specialized FIR filter.

All of the **c1xxx.exe** programs can be put into EPROM for loading when the EZKIT-Lite starts operation. See the Analog Devices PROM Splitter for details.

Documentation for the DSP-10 2-Meter Transceiver

Included in five directories is a complete set of documentation for the DSP-10 2-meter transceiver. All **.TXT** files are simple ASCII text with embedded end-of-lines. All **.HTM** files can be read on a Web browser.

This documentation is up-to-date as of March 2002. Further data may be available on the internet. The URL currently is <http://www.proaxis.com/~boblark/dsp10.htm>. If the Web page location is changed it will still include the word **ABCDSP10ABCD** that may be helpful for locating it with a search engine! See the **.txt** files listed below for more information.

Here is a quick summary of the contents to help in finding files.

ARTICLES

Contains the three *QST* articles from Sept-Nov 1999 in **.PDF** format.

1. R. Larkin, "The DSP-10: An All-Mode 2-Meter Transceiver Using a DSP IF and PC-Controlled Front Panel," *QST*, Sep, 1999, pp 33-41; Oct, 1999, pp 34-40; Nov, 1999, pp 42-45.

HARDWARE

dsp10hdw.txt - General notes, corrections and improvements.

dsp10n45.txt - Assembly notes for the project

dsp10pd2.txt - Assembly part-by-part list, with locations on the PCB

dsp10ph5.htm - Part list for purchasing parts

u15_mod.htm - Improvement information referenced by **dsp10hdw.txt**

u15mod1.gif - A sketch required for **u15_mod.htm**.

f10.gif - A corrected figure 10 for the *QST* articles.

f11.gif - A corrected figure 11 for the *QST* articles.

EXECUTABLE

Uhfa.exe - DOS Executable front panel program

Uhf3.exe - Machine language program (NOT A DOS .EXE file)

Egavga.bgi - Borland graphics drivers for PC

Gnugpl.txt - User license (Please Read)

Uhfa_43a.rnd - Random number list for several of the weak signal modes.

Readme16.txt - Software user information for basic modes

Readme20.txt - Additional user information, including weak-signal modes.

Wat_exe.txt - A reminder that **UHF3.EXE** is NOT a DOS .exe file.

SOURCE CODE AND MISCELLANEOUS

CSRC - Source code for the PC program, in Borland C: 28 files.

DSPSRC - Source code for the EZKit program: 33 files.

Included in the last two directories are two batch files, **U.BAT**, that assembles and links the program from the various modules. The file, **U3.BAT**, serves the same function for the DSP program.

The file **Pc_dsp2.txt** in the directory **CSRC** has the details of the communication between the PC and the DSP.

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Editor's Note: Except for commonly used phrases and abbreviations, topics are indexed by their noun names. Many topics are also cross-indexed, especially when noun modifiers appear

(such as "Modulator, Balanced" and "Balanced, Modulator"). The letters "ff" after a page number indicate coverage of the indexed topic on succeeding pages.

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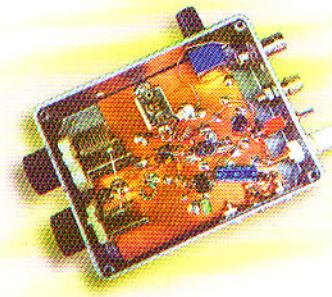
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EMRFD brings professional RF design experience to the radio amateur. It's written for anyone with a driving curiosity about state-of-the-art equipment.

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Published by:

ARRL The national association for
AMATEUR RADIO

225 Main Street • Newington, CT 06111-1494 USA

ARRLWeb: www.arrl.org/

ISBN 0-87259-879-9

54995 >
EAN
9 780872 598799

ISBN: 0-87259-879-9 ARRL Order No. 8799