On the Analysis of Low Output Impedance Characteristic of Flipped Voltage Follower (FVF) and FVF LDOs

(Invited Paper)

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***Abstract*—The flipped voltage follower (FVF), a variant of the common-drain transistor amplifier, comprising local feedback, finds application in circuits such as voltage buffers, current mirrors, class AB amplifiers, frequency compensation circuits and low dropout voltage regulators (LDOs). One of the most important characteristics of the FVF, is its low output impedance. In this tutorial-flavored paper, we perform a theoretical analysis of the transfer function, poles and zeros of the output impedance of the FVF and correlate it with transistor-level simulation results. Utilization of the FVF and its variants has wide application in the analog, mixed-signal and power management circuit design space.**

***Index Terms*—Flipped voltage follower (FVF), common drain circuit, CMOS class-AB op-amps, voltage buffers, output impedance.**

I. Introduction

The flipped voltage follower (FVF) can be viewed as a variant of the common-drain (CD) circuit with local feedback [1]. The FVF has characteristics that are similar to a CD transistor amplifier, such as high input impedance, unity gain, low output impedance, good linearity, and a level shift of approximately one threshold voltage, which makes the circuit desirable to operate as a voltage buffer. The FVF has been utilized in several applications, such as voltage buffers [2], [3], low input impedance current mirrors [4], class AB amplifiers [5], [6], frequency compensation networks [7] and low dropout voltage regulators (LDOs) [8]–[17].

In the design of LDOs, it is particularly important to achieve low output impedance when driving small resistive loads, so that the LDO achieves good steady-state load regulation. Low output impedance pushes the pole at the output node to a higher frequency, improving the LDOs transient response [18]–[20]. When driving large capacitive loads, low output impedance allows the LDO to respond quickly to changes in load current. Indeed, the fastest LDOs which drive large output capacitors require a low output impedance output stage [21].

In this tutorial-flavored paper, we explore one of the most important characteristics of the FVF, which is its low output impedance behavior as a function of frequency. We compare and contrast this characteristic with that of a CD amplifier for the purposes of developing intuition.

Fig. 1(a) shows the conventional PMOS CD transistor amplifier topology. In this topology, notice that the bias current

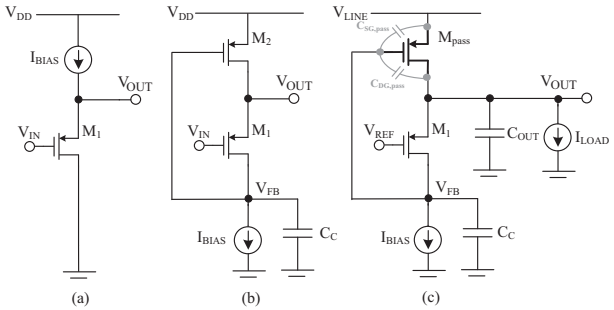

Fig. 1: (a). PMOS common-drain amplifier, (b) PMOS FVF, (c) typical implementation of an FVF in the output stage of an LDO.

I_{BIAS} sources current from the positive supply. Fig. 1(b) illustrates a PMOS FVF circuit. The input to the FVF, V_{IN}, is applied at the gate terminal of PMOS transistor M_1. Transistor M_2 is configured as a common-source amplifier, the gate of which is connected to feedback terminal V_{FB}, forming a local feedback loop. V_{FB} is also the drain terminal of M_1 and is connected to the "flipped" bias current I_{BIAS}, as illustrated in Fig. 1(b). This use of a "flipped" bias relative to the traditional CD circuit explains the name, "flipped voltage follower". Compensation capacitor C_C is connected to the feedback node V_{FB}. The output, V_{OUT}, is at the source of M_1 and the drain of M_2. In the case of a PMOS FVF, the output voltage range is given by

$$\begin{aligned} V_{out,max} &= V_{DD} - V_{SD2,sat} \\ V_{out,min} &= V_{DD} - V_{SG2} + V_{SD1,sat} \end{aligned} \tag{1}$$

where V_{SG} and $V_{SD,sat}$ represent source-to-gate and overdrive voltages, respectively.

Fig. 1(c) illustrates the typical implementation of an FVF in the output stage of an LDO. M_{pass} is the huge pass transistor of the LDO. The input reference voltage, V_{REF}, is applied to the gate of M_1. Parasitic capacitances $C_{SG,pass}$ and $C_{DG,pass}$ associated with M_{pass} are large and are often comparable to the output capacitor. As such, they cannot be neglected when performing the small-signal analysis.

The paper is organized as follows: in Section II we present the small-signal analysis of the FVF output impedance. Section III contains transistor-level simulation results verifying the work in Section II. We conclude in Section IV.

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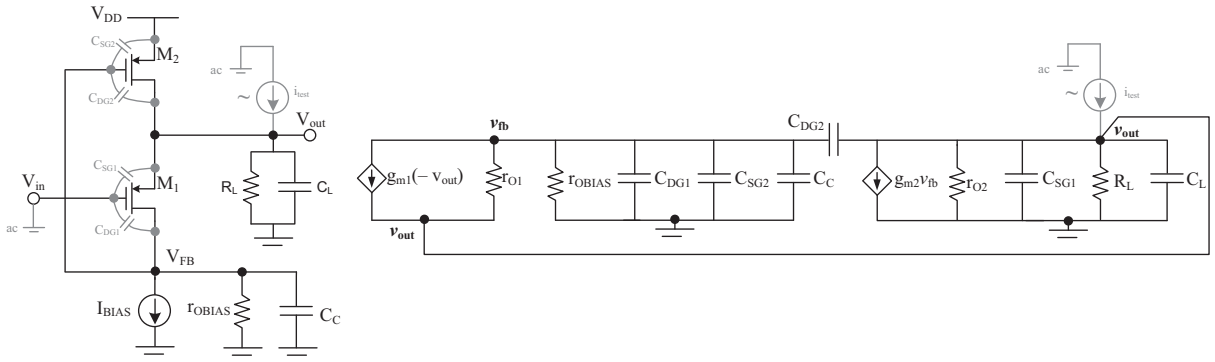

Fig. 2: (a) PMOS FVF with ac signal i_{test} injected at output node V_{out}. Input V_{in} is ac grounded. The parasitic capacitances associated with M_1 and M_2 are shown. (b) Equivalent small-signal circuit used to find the output impedance of the FVF.

$$Z_{out,FVF}(s) \cong \frac{\big(1+s\big(r_{O1}\|r_{OBIAS}\big)\big(C_{FB}+C_{GD2}\big)\big)}{g_{m1}\ r_{O1}\ g_{m2}\left(1+\left(\frac{C_{FB}}{g_{m2}}+\frac{C_L}{g_{m1}g_{m2}\big(r_{O1}\|r_{OBIAS}\big)}\right)s+\left(\frac{C_{FB}C_L}{g_{m1}g_{m2}}\right)s^2\right)} \tag{2}$$

II. Analysis of FVF Output Impedance

Fig. 2(a) is the schematic used to find the output impedance of the FVF circuit shown in Fig. 1(b). To find the output impedance, test current i_{test} is injected into the output node, V_{out}, and input V_{in} is connected to ac ground.

Also shown in the figure are the dominant parasitic elements associated with FVF transistors M_1 and M_2. Fig. 2(b) shows the small-signal equivalent model of the circuit in Fig. 2(a).

Parameters g_{mi}, r_{Oi}, C_{SGi} and C_{DGi} represent the transconductance, output resistance, source-to-gate capacitance and drain-to-gate capacitance associated with transistor M_i. Transistor M_1 is modeled as voltage-controlled current source (VCCS) $-g_{m1}v_{out}$, as small-signal input v_{in} is connected to ac ground. Transistor M_2 is represented by a VCCS $g_{m2}v_{fb}$.

Grounded compensation capacitor C_C, often used to stabilize the FVF, is connected to node V_{FB}. The equivalent capacitance C_{FB} associated with node V_{FB} is given by

$$C_{FB} = C_{DG1} + C_{SG2} + C_C. \tag{3}$$

The capacitance associated with node V_{out} can be approximated as C_L, assuming $C_L >> C_{SG1}$.

The output impedance of current source I_{BIAS} is r_{OBIAS}, which cannot be assumed to be infinite.

A. Output Impedance Transfer Function

Applying KCL equations at each node, we solve to obtain the output impedance transfer function, defined as

$$Z_{OUT}(s) \equiv V_{out}(s)/i_{test}(s). \tag{4}$$

The complete FVF output impedance transfer function is shown near the top of the page in equation (2).

B. Output Resistance at DC

In order to obtain the output resistance at DC, we substitute s = 0 in the impedance transfer function (2). The output resistance of the FVF at DC is given by

$$R_{OUT} \approx \frac{1}{g_{m1}r_{O1}g_{m2}}. \tag{5}$$

Equation (5) is an important result, which implies a very-low-valued DC output impedance for the FVF. We note that the DC output resistance of the CD voltage buffer of Fig. 1(a) is given by

$$R_{OUT,CD} = \frac{1}{g_{m1}}\| \ r_{O1} \approx \frac{1}{g_{m1}}, \tag{6}$$

where g_{m1} represents the transconductance of the input CD transistor M_1 . Comparing (5) and (6), we observe that the DC output impedance of the FVF is lower than the CD voltage buffer output impedance by a factor of $g_{m2}r_{O1}$, i.e.,

$$R_{OUT,FVF} = \left(\frac{1}{g_{m2}r_{O1}}\right)R_{OUT,CD}. \tag{7}$$

In modern CMOS processes, one can expect the output resistance of the FVF to be lower than that of the CD amplifier by a factor generally ranging from 10 to 25.

C. Output Impedance Characteristic at Higher Frequencies

1) Case 1: In case the FVF application is that of a voltage buffer, where $g_{m1} \approx g_{m2}$ and C_C is similar in magnitude to C_L , poles ω_{P1} and ω_{P2} are given by

$$\begin{aligned} \omega_{P1} &\approx -\frac{g_{m2}}{C_{FB}}, \\ \omega_{P2} &\approx -\frac{g_{m1}}{C_L}, \end{aligned} \tag{8}$$

where poles ω_{P1} and ω_{P2} are situated very close to one another. The numerator of the impedance transfer function in (2) indicates the presence of a left-half-plane (LHP) zero, which is given by

$$\omega_{Z1} = -\frac{1}{(r_{O1} \| r_{OBIAS})(C_{FB} + C_{GD2})}. \quad (9)$$

As $r_{OBIAS} >> (1/g_{m2})$, LHP zero ω_{Z1} occurs before both poles ω_{P1} and ω_{P2}.

Fig. 3 illustrates the output impedance behavior of the FVF pertaining to this case. Note that ω_{Z1} occurs prior to ω_{P1} and ω_{P2}. As such, the output impedance will begin to increase near ω_{Z1}, which is generally undesirable in a voltage buffer application. The proximity of ω_{P1} and ω_{P2} results in impedance peaking.

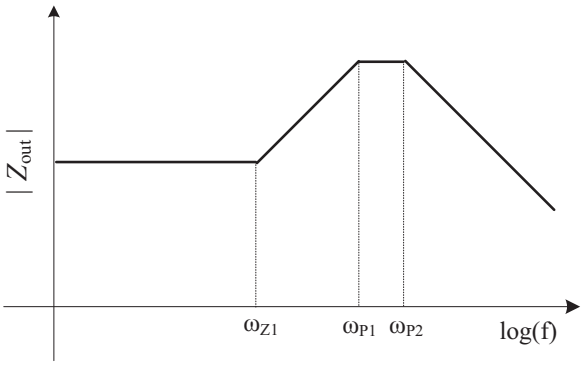

Fig. 3: Typical output impedance characterictic of FVF circuit.

2) Case 2: In the case of an FVF application where $g_{m1} \approx g_{m2}$ and $C_L >> C_C$, poles ω_{P1} and ω_{P2} are given by

$$\omega_{P1} \approx -\frac{g_{m1} g_{m2} (r_{O1} \| r_{OIBIAS})}{C_L}, \qquad \omega_{P2} \approx -\frac{1}{(r_{O1} \| r_{OIBIAS}) C_{FB}}. \quad (10)$$

Again, poles ω_{P1} and ω_{P2} are situated very close to each other. No change occurs in the equation for ω_{Z1}.

The major difference in this application is that LHP zero ω_{Z1} is now at a frequency somewhat close to ω_{P2}. As such, the LHP zero will be approximately canceled and the output impedance will begin to decrease at frequencies close to ω_{P1}. Decreasing output impedance is a desirable effect.

From this case, we observe an inherent trade-off in the implementation of FVF circuits. If C_C is small, or omitted altogether, the magnitude of the output impedance will monotonically decrease with frequency. On the other hand, the purpose of C_C is to ensure that the local feedback loop in the FVF circuit is stable, meaning, remains negative. Thus, a tradeoff exists between stability and low output impedance.

3) Case 3: FVF LDO topology: In the case of the FVF as the output stage of an LDO, transistor M_2 is a huge pass transistor. In this scenario, transconductance $g_{m2} >> g_{m1}$ and $C_C << C_L$ and a complex-pole pair is formed, given by

$$\omega_{P1,2} \approx \sqrt{\frac{g_{m1} g_{m2}}{C_{FB} C_L}}. \quad (11)$$

Complex pole pairs generally give rise to peaking in the magnitude response of the output impedance function, as well as sharp transitions in the phase response. No change occurs in the equation for ω_{Z1}.

Assuming $r_{O1} > 1/g_{m2}$, which is the goal in most practical applications of the FVF, then LHP zero ω_{Z1} occurs prior to the complex pole pair. This creates an even higher peak in the magnitude of the output impedance. Proper choice of design parameters will help to reduce the impedance peaking and achieve low output impedance over a broad frequency range.

III. Simulation Results

The PMOS CD amplifier of Fig. 1(a) and the PMOS FVF of Fig. 1(b) are designed and simulated in a 180-nm CMOS process, with a supply voltage of 1.8V and a quiescent current of 5μA. Fig. 4 shows the output impedance vs. frequency plot of the CD and FVF topologies.

As can be seen in Fig. 4, at DC, the CD topology has an output resistance of 4.86 kΩ, whereas the FVF demonstrates a much lower output impedance of 294Ω. The reduction in output resistance for the FVF is approximately 16 times that of the CD amplifier.

Fig. 4 also demonstrates the undesirable effect of output impedance peaking, which occurs in the FVF, but not in the common-drain amplifier. The frequency at which it occurs is relatively high and, therefore, may or may not negatively impact the application for which it is intended.

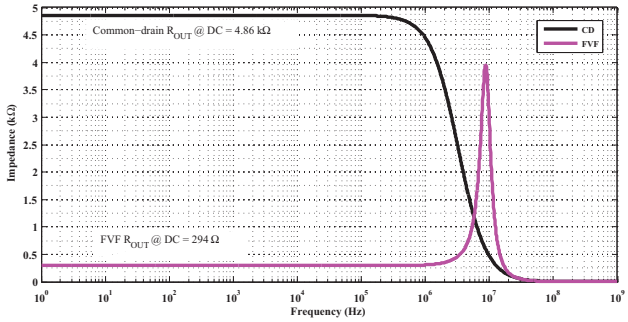

Fig. 4: Output impedance characteristic of CD and FVF topologies.

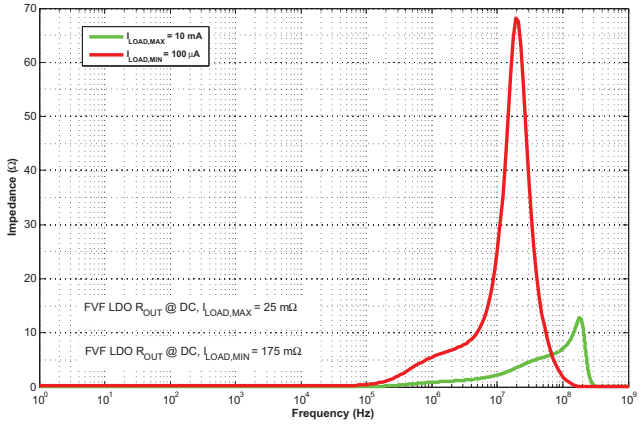

Fig. 5: Output impedance characteristic of FVF LDO.

Fig. 5 shows the simulated output impedance characteristic of a typical FVF LDO implementation. Note that as load current I_{LOAD} varies from a light load of $I_{LOAD,MIN}$ = 100μA to a heavy load of $I_{LOAD,MAX}$ = 10mA, the transconductance of the pass transistor increases, whereas its output resistance decreases. The result is markedly different output impedance transfer functions. At DC, the output impedance magnitude at light load is 175mΩ, whereas at heavy load it is 25mΩ . More importantly, at light load the output impedance magnitude shows a large peak at 20 MHz, whereas at heavy load the peak value is much lower and occurs near 200 MHz.

IV. Discussion and Conclusion

The CD transistor amplifier is a commonly-used voltage buffer because of its low output impedance characteristic. The FVF circuit demonstrates much lower output impedance characteristic at DC compared to CD topology, making it a desirable choice. At higher frequencies, frequency peaking is seen in most cases of FVF topologies, as analyzed in this paper. Choosing appropriate design parameters, including transistor dimensions and compensation capacitance, can help reduce impedance peaking.

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