1. Extract the source codes from the zip file to folder xxxx.

Make sure NOT to change the folder structure of the source codes.

All source codes stay in src folder, sim folder contains all simulation related tcl scripts and assemble code. syn folder is for synthesis results.

1. Download SoCEDSSetup-17.0.0.595-windows.exe from Altera/Intel website. This SW is also needed for HPS development.
2. run SoC EDS command shell -> this shall be available after you install SoC EDS software. This starts a Cygwin shell. All following commands are executed in the shell.
3. Compile the design

cd xxxxx -> goto the folder where you copy the source code to

cd sim -> in the folder you could find .tcl file which is TCL scripts, which does not work

vlib work -> this creats a folder named work if it does not exists

vcom -87 ../src/risc\_i\_16\_pack.vhd

vcom -87 ../src/alu.vhd

vcom -87 ../src/reg\_file.vhd

vcom -87 ../src/datapath.vhd

vcom -87 ../src/control.vhd

vcom -87 ../src/sync\_reset.vhd

vcom -87 ../src/cpu.vhd

vcom -93 ../src/memory.vhd

vcom -87 ../src/cpu\_tb.vhd -> this is the top-level testbench

1. run ModelSim for functional simulation

vsim -gfile\_base\_g=gcd cpu\_tb -> this starts ModelSIM GUI, using gcd.ass. In ModelSim you shall see all the hierarchy of CPU and TB. Try to modify the gcd.ass, or use differnt option to start ModelSim.

Vsim is the command to call ModelSim.

-g is the option to give file\_base\_g, a parameter defined in cpu\_tb.vhd a value besides default value. gcd.ass is in folder xxxx/sim for your reference, which is the assemble code to be parsed/compiled and executed.