ECSE 222 – DIGITAL LOGIC
VHDL ASSIGNMENT 1
LAB REPORT

Group:

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SUMMARY

For the first VHDL assignment, we were introduced to Quartus Prime and ModelSim for programming VHDL and designing logic circuits. We spent most of the time understanding the user interface of these programmes, the syntax of VHDL, and the procedure of writing scripts and test benchmarks. In the end, we had created an ‘OR-gate’ and tested it properly to ensure its functionality.

FIGURES

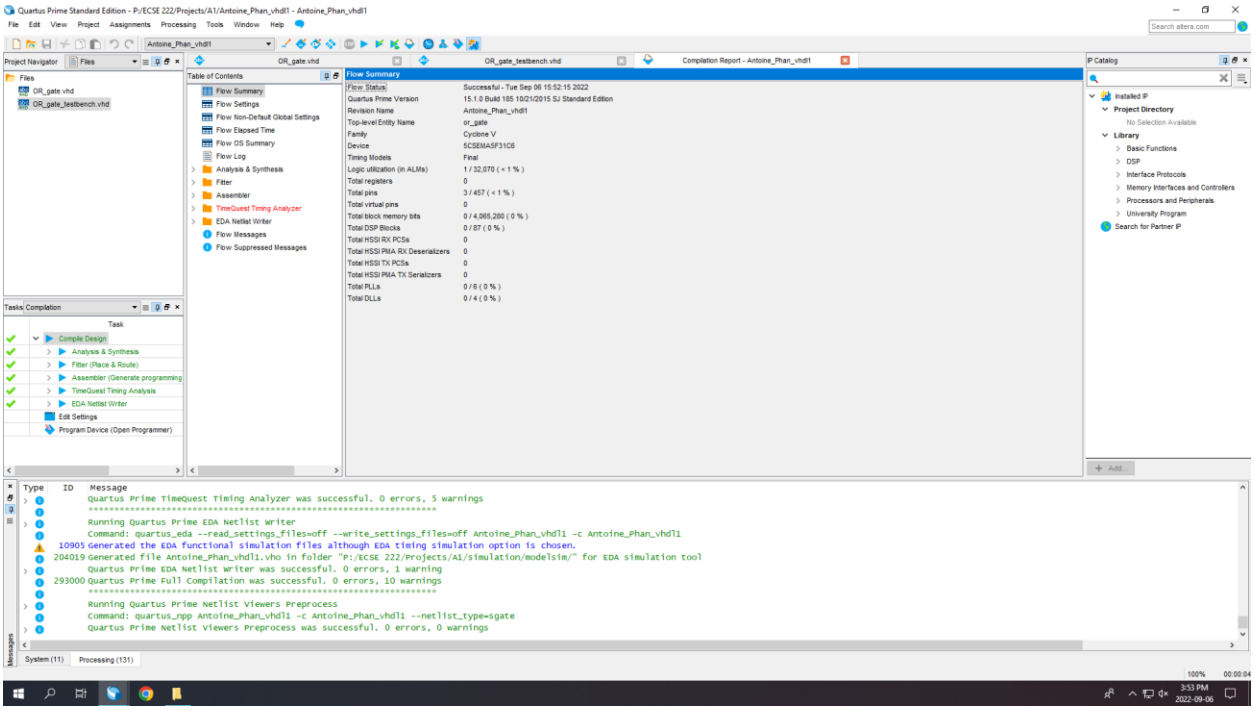

Image 1: Screenshot of **Quartus Prime** after successfully compiling the VHDL scripts

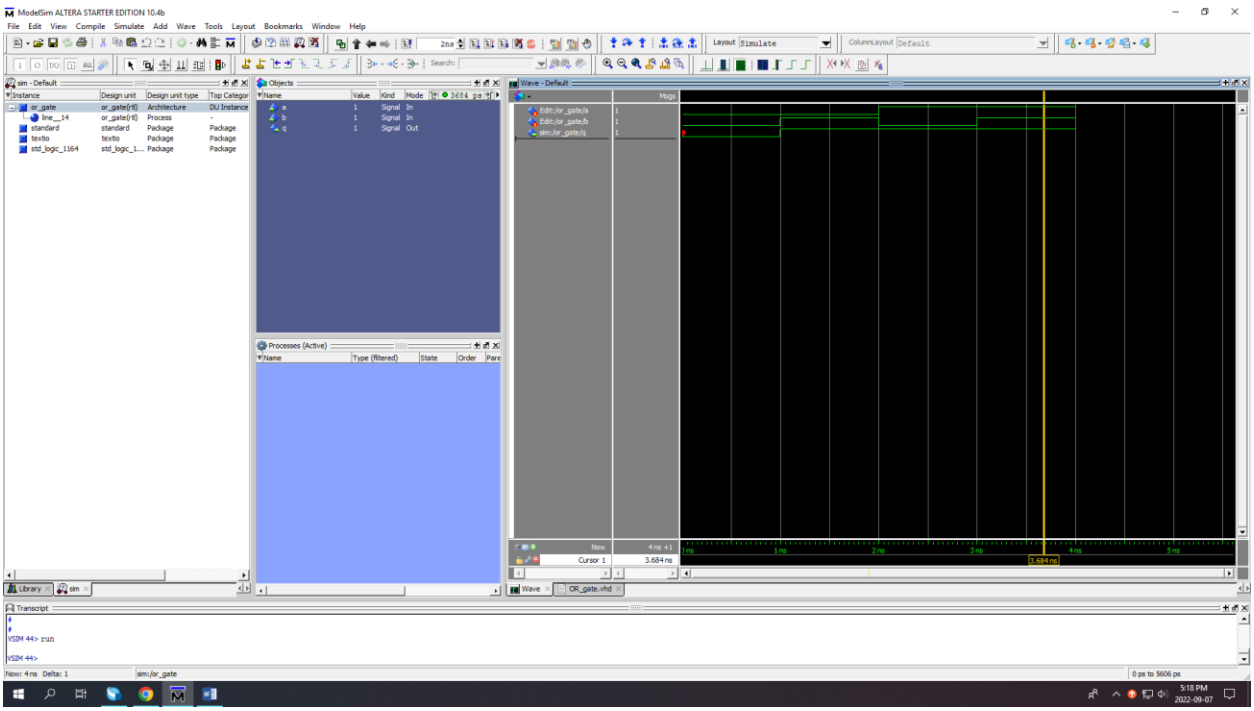

Image 2.1: Screenshot of **ModelSim** after running “EDA RTL Simulation”

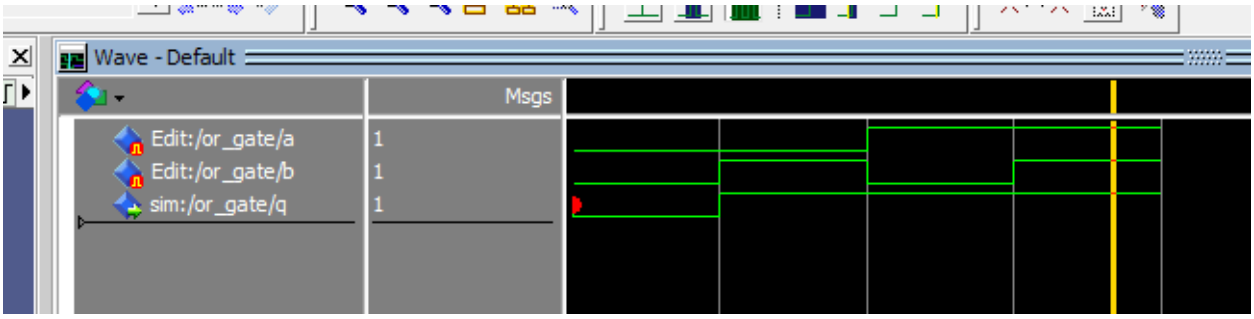

Image 2.2: Close-up screenshot of **ModelSim**, simulating the truth table of logical OR
(Note: low wave = 0, high wave = 1)

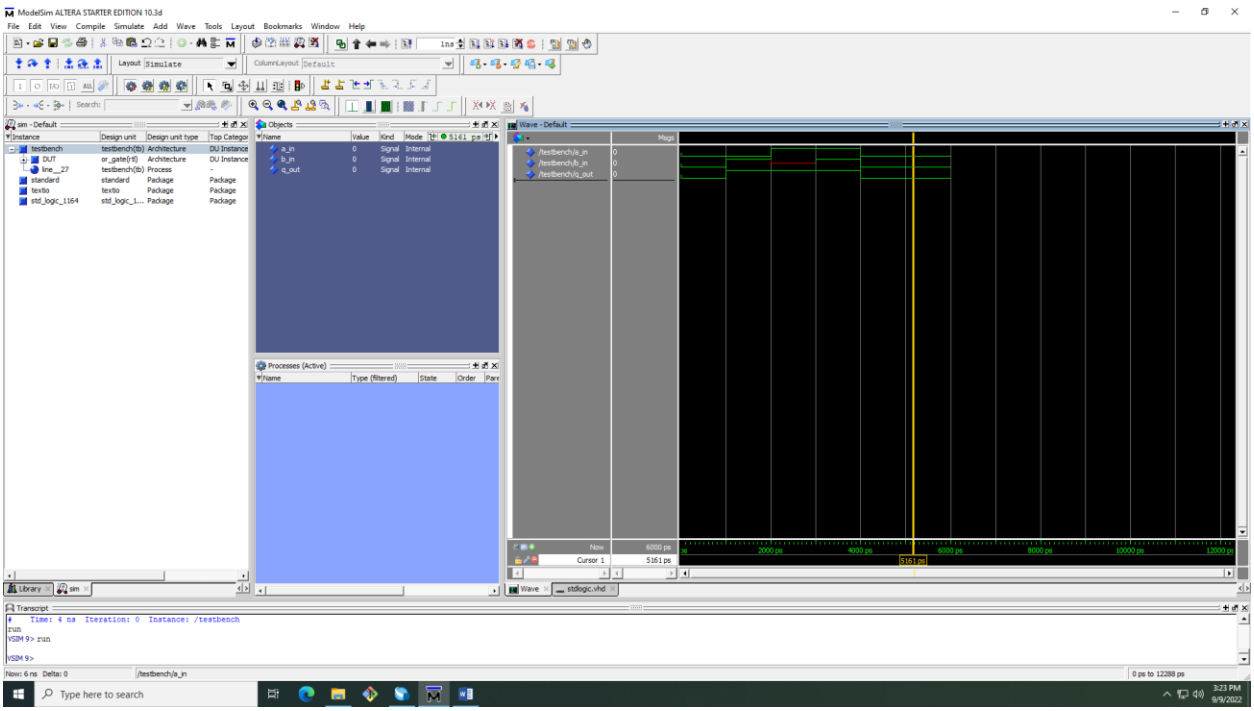

Image 3.1: Screenshot of **ModelSim** after running “EDA RTL Simulation”, showing test bench of the programme with its simulation.

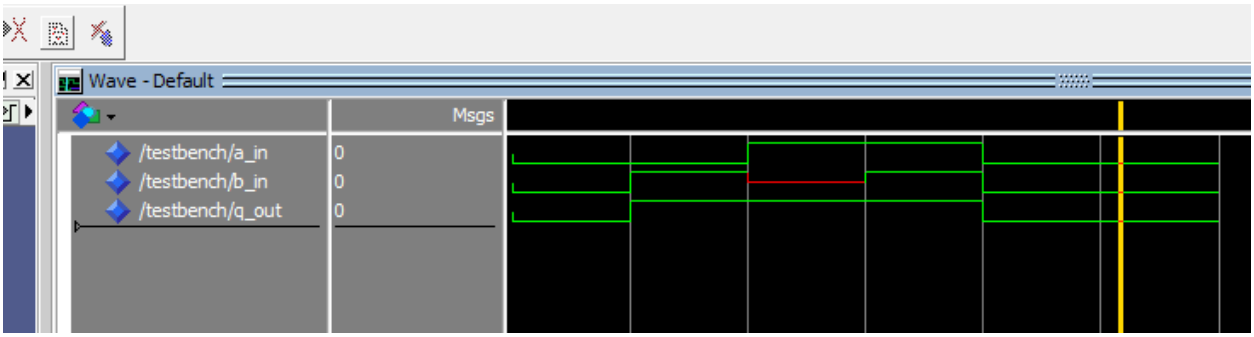

Image 3.2: Close-up screenshot of **ModelSim**, simulating the testbench scripts (Note: low green wave = 0, high green wave = 1, red wave = ‘X’)

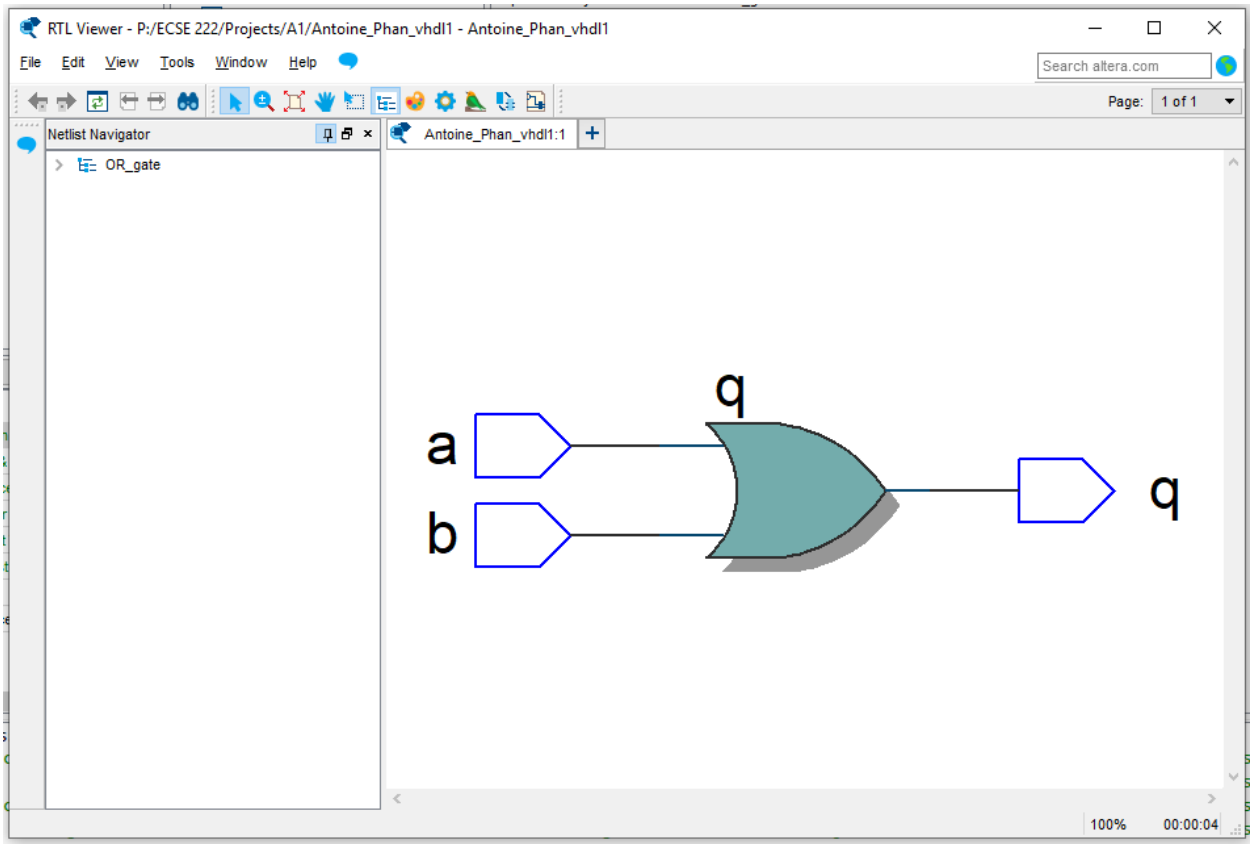

Image 4: Screenshot of the generated **OR gate** from *"Netlist Viewers"* → *"RTL Viewer"*

CONCLUSION

Although much of the scripts were written for us and the procedure was explained in detail, we learned the basics of Quartus and ModelSim programmes for the design of digital logic circuits and VHDL as a description hardware language.