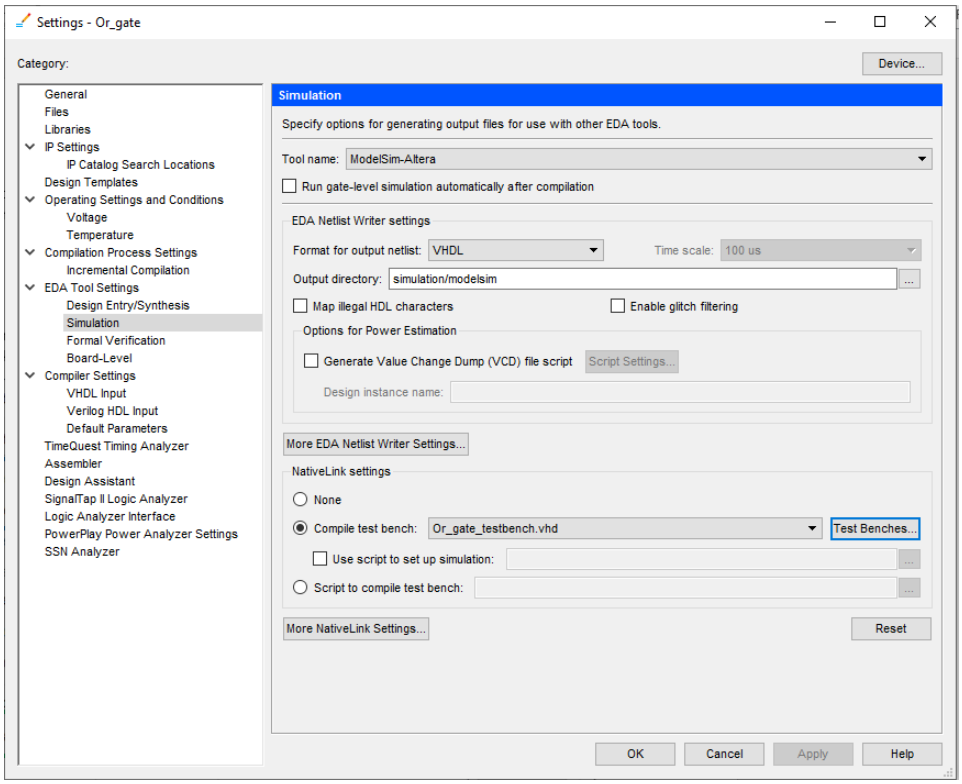
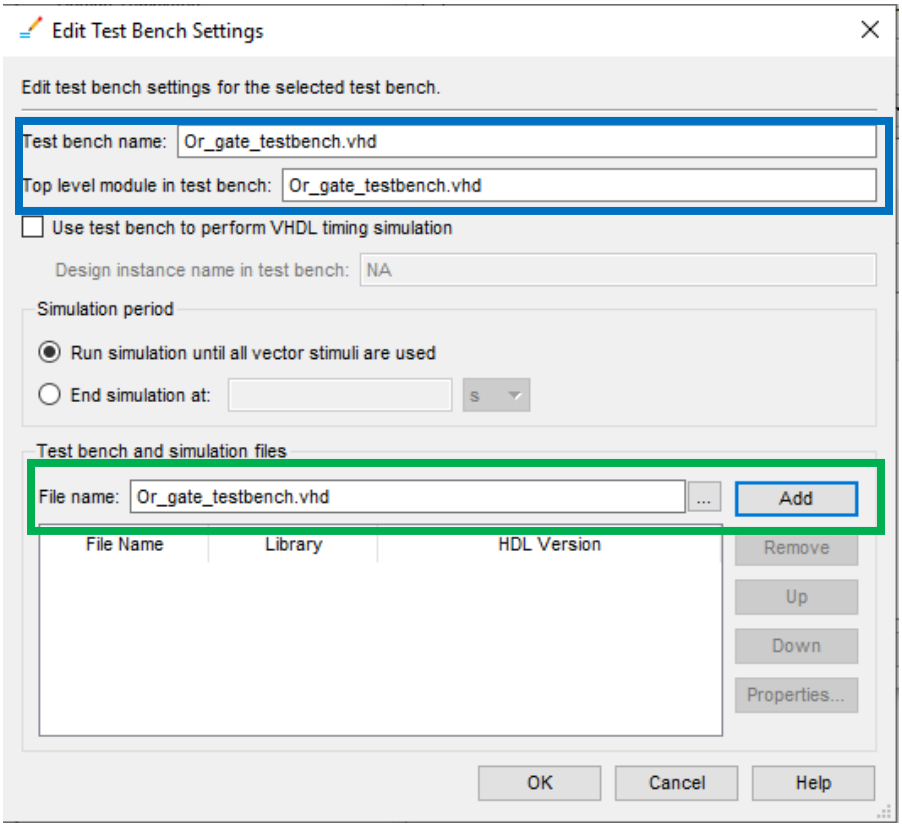
Additional Instruction for Lab 1

For Testbench setting, if you don't see the test bench name already in the dropdown box, click on the "Test Benches.." button (marked in blue)

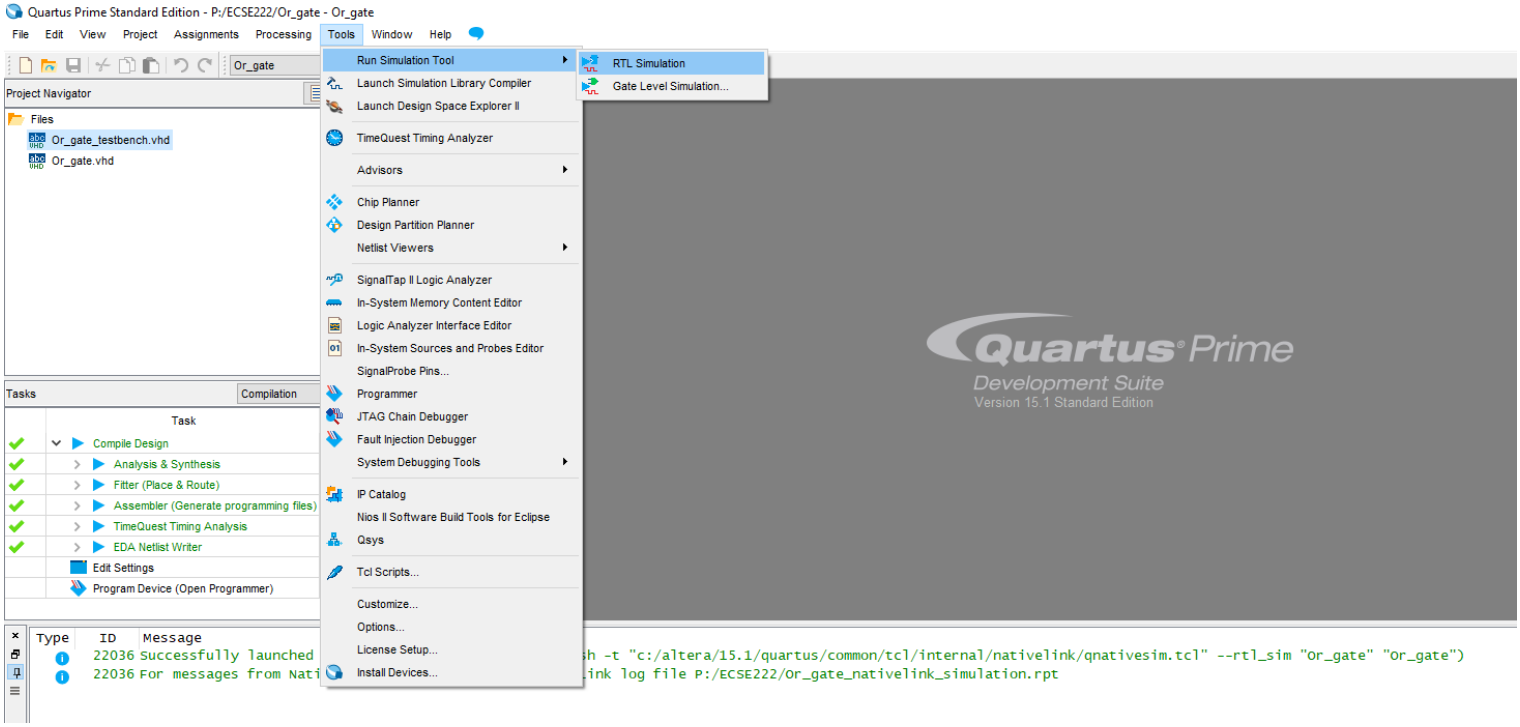


The click on "New.." , and it will open the following window. Add the name of your test bench (with extension) in the first two fields (marked in blue). Then click the "…" button to add the test bench vhdl file (marked in green)

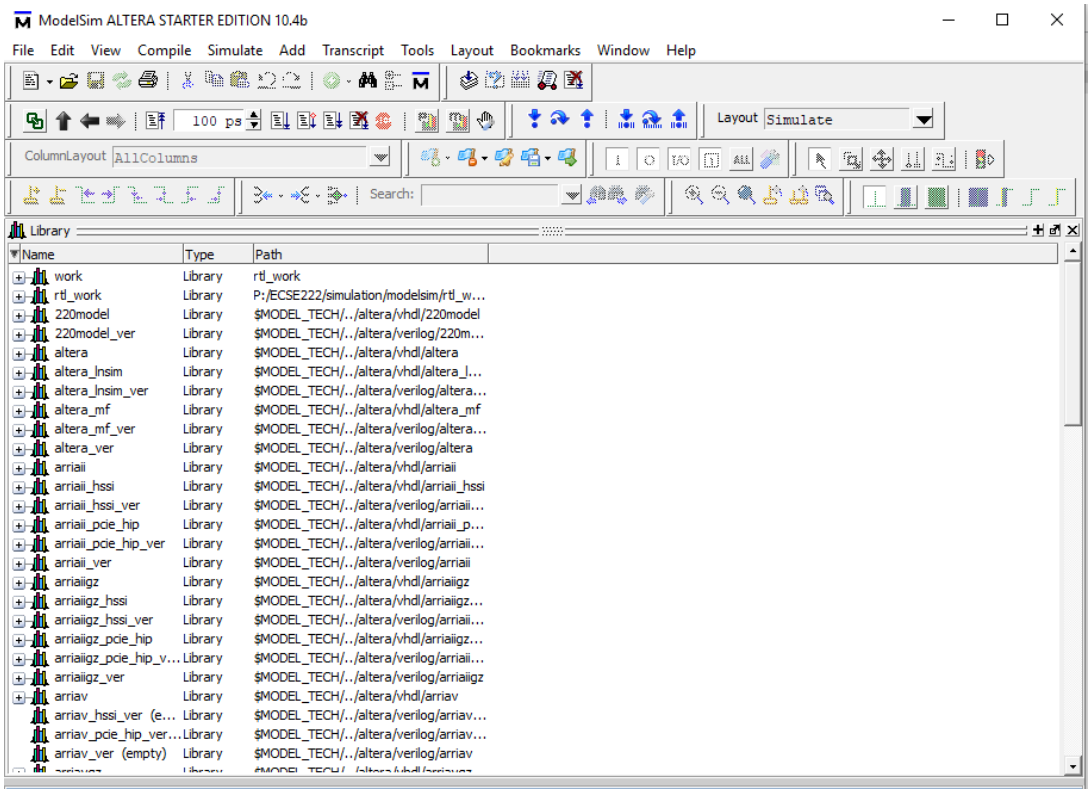


For RTL Simulation

Follow all the steps in the original lab manual to create and compile the code till the following step

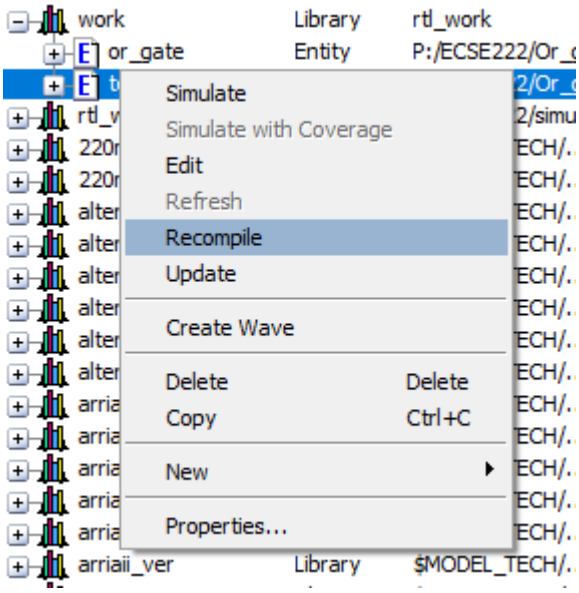


After you click the “RTL Simulations”, the ModelSim_Altera should launch, and show you the required simulation graphs. However, for some of the people the following screen would appear

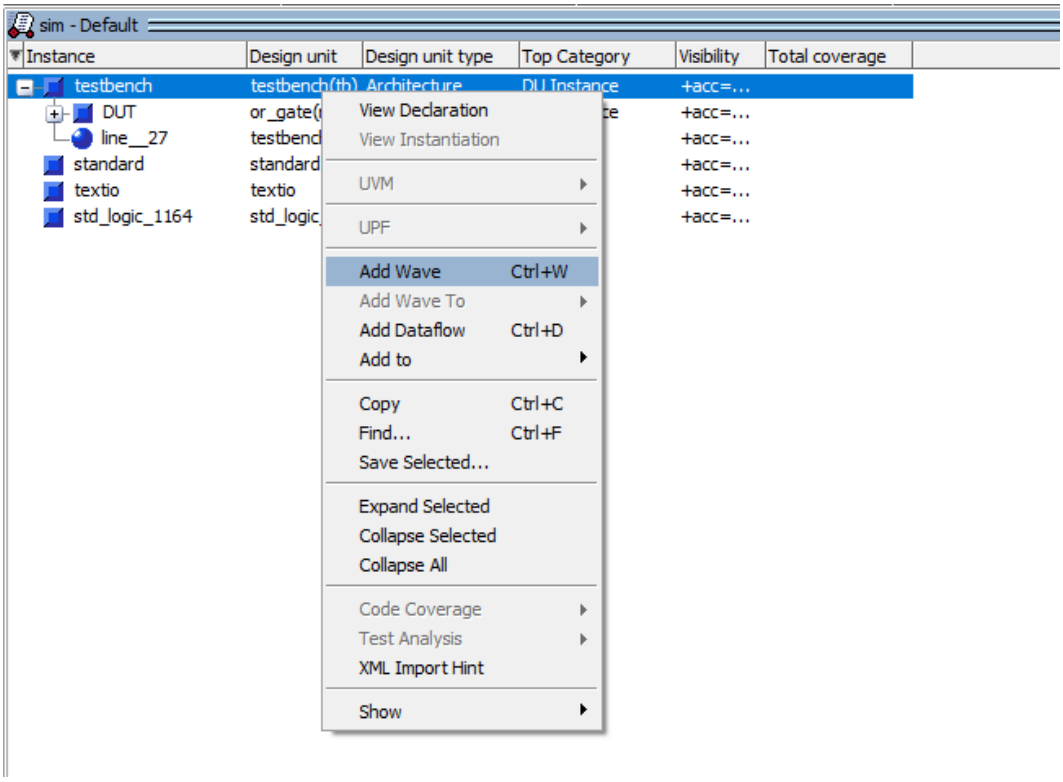


Follow the following instruction to get the simulation plots,

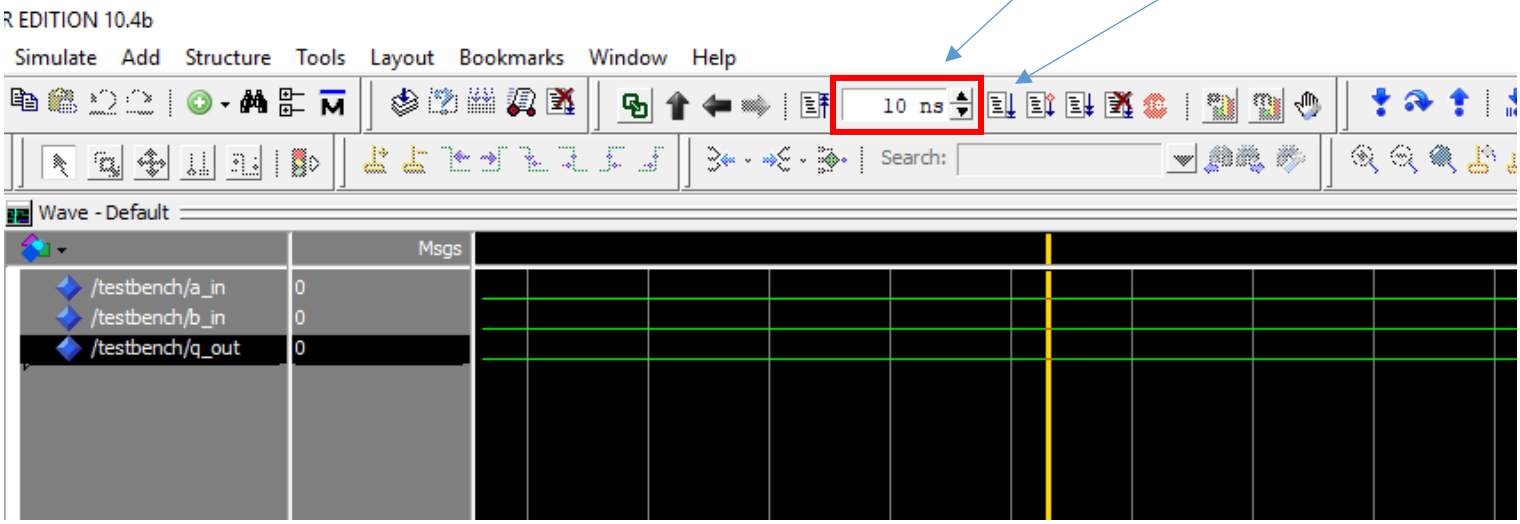
Step 1: Under the “Work” name you will see you both VHDL files, right-click and **“Recompile”** them both as shown



Step 2: Right-click on the test bench file and select **“Simulate”** , a new window will appear . Right-click on test bench name and select “Add Wave” as shown



Step 3: Once the simulation screen appears change the simulation time to 10ns and click “Run” button as marked below, you will be able to see plots for all three pins



To view the complete plot you can right-click on the screen and select “zoom full” to get the following simulation results