4-Bit Comparator Using Four 1-Bit Comparators

Digital Logic Design Report

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2025

Contents

Design and Analysis of a 4-Bit Comparator Using Four 1-Bit Comparator Modules

1 Introduction

A digital comparator is a combinational logic circuit that compares binary numbers and determines their magnitude relationship. This report presents the design of a 4-bit comparator using four cascaded 1-bit comparator modules. Each 1-bit comparator determines the relationship between a pair of bits (A_i and B_i), and the final 4-bit result is determined by prioritizing comparison from the Most Significant Bit (MSB) down to the Least Significant Bit (LSB).

The goal of this documentation is to clearly explain the theoretical design, Boolean expressions, truth tables, and cascading mechanism that allow four simple 1-bit comparators to function as a complete 4-bit comparator.

2 Theoretical Background

2.1 Logic Gates Used

- **AND Gate:** Output is 1 only when all inputs are 1.
- **OR Gate:** Output is 1 when at least one input is 1.
- **NOT Gate:** Inverts the input.
- **XOR Gate:** Output is 1 when the inputs differ. Used for detecting inequality.
- **XNOR Gate:** Output is 1 when the inputs are equal. Used for equality detection.

2.2 Boolean Algebra Used

- $A \oplus B = \overline{A}B + A\overline{B}$ (Inequality)
- $A \odot B = AB + \overline{AB}$ (Equality)
- $A > B$ when $A\overline{B} = 1$
- $A < B$ when $\overline{A}B = 1$
- Cascading uses AND to propagate "Equal so far"

3 1-Bit Comparator Design

A single comparator compares A_i and B_i. It generates three outputs:

$$E_i = A_i \odot B_i$$
$$G_i = A_i \cdot \overline{B_i}$$
$$L_i = \overline{A_i} \cdot B_i$$

Where:

- $E_i = 1$ means $A_i = B_i$
- $G_i = 1$ means $A_i > B_i$
- $L_i = 1$ means $A_i < B_i$

3.1 Truth Table for 1-Bit Comparator

A_i	B_i	Equal (E_i)	Greater (G_i)	Less (L_i)
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

4 4-Bit Comparator Architecture

Let the two 4-bit numbers be:

$$A = A_3A_2A_1A_0, \quad B = B_3B_2B_1B_0$$

Comparison starts from A_3 and B_3 (MSB). If they are equal, comparison moves to the next bit. If they differ, the result is immediately decided.

This is implemented by **cascading** the 1-bit comparators using "Equal so far" signals.

4.1 Boolean Equations for the Full Comparator

4.1.1 Equality Output

$$EQ = E_3E_2E_1E_0$$

4.1.2 Greater Output

$$G = G_3 + E_3G_2 + E_3E_2G_1 + E_3E_2E_1G_0$$

4.1.3 Less Output

$$L = L_3 + E_3L_2 + E_3E_2L_1 + E_3E_2E_1L_0$$

These equations enforce MSB priority.

5 Cascading Logic Explanation

- The MSB comparator decides first.
- If $A_3 > B_3$ or $A_3 < B_3$, the lower bits do not matter.
- Only when $E_3 = 1$ (meaning $A_3 = B_3$), the system checks A_2 vs. B_2.
- This continues until a difference is found, or all bits match.

This ensures correct multi-bit comparison.

6 Truth Table for 4-Bit Comparator

Instead of listing all 256 combinations, a structured table is provided showing how the result depends on comparisons:

$A_3A_2A_1A_0$	$B_3B_2B_1B_0$	Greater	Equal	Less
$A > B$	any	1	0	0
$A = B$	identical bits	0	1	0
$A < B$	any	0	0	1

6.1 Expanded MSB-Priority Interpretation

- If $A_3 > B_3 \rightarrow$ A ¿ B (ignore lower bits)
- If $A_3 < B_3 \rightarrow$ A ¡ B (ignore lower bits)
- If $A_3 = B_3 \rightarrow$ compare A_2 and B_2
- Continue until a difference is found
- If all bits equal $\rightarrow$ A = B

7 Summary

This documentation presents the complete theoretical structure of a 4-bit comparator built from four 1-bit comparator modules. Using basic logic gates, Boolean algebra, and cascading MSB-priority logic, the circuit produces three outputs indicating whether $A > B$, $A = B$, or $A < B$. The design is fully modular, beginner-friendly, and demonstrates the fundamentals of digital comparison circuits.

A Final Schematic

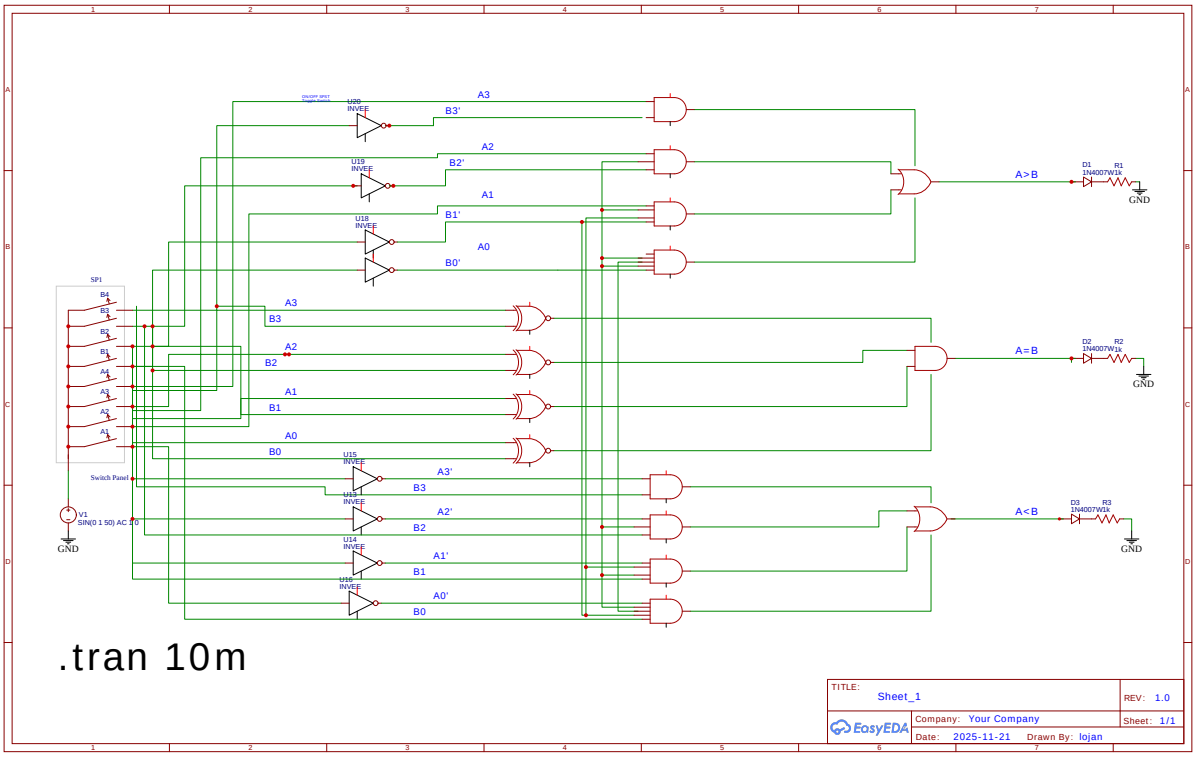

Figure 1: Final EasyEDA Schematic of the 4-bit Comparator