MODEL NO. : TM035NDH07

MODEL VERSION: 00

ISSUED DATE: 2017-07-05

VERSION : Ver 2.1

□**Preliminary Specification**

■**Final Product Specification**

Customer : Leelab

Approved by	Notes

TIANMA Confirmed :

Prepared by	Checked by	Approved by
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This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2016-9-13	Preliminary Specification Release	Dongliang xie
2.0	2017-5-24	Final Specification Release	Dongliang Xie
2.1	2017-7-05	Update drawing changing printing code to paper label in page 20	Dongliang Xie

1 General Specifications

Feature		Spec
Display Spec.	Size	3.5 inch
	Resolution	272(RGB) x 480
	Technology Type	a-si TFT
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(mm)	0.16125 x 0.16125
	Display Mode	TM,NW
	Surface Treatment	AG
	Viewing Direction	9 o'clock
	Gray Scale Inversion Direction	3 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	50.86x87.98x2.50
	Active Area(mm)	43.86x77.40
	With /Without TSP	Without TSP
	LED Numbers	6 LED
	Weight (g)	21.2g
Electrical Characteristics	Interface	RGB 18bits+SPI
	Color Depth	262K
	Driver IC	ILI9488

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

2 Input/Output Terminals

No	Symbol	I/O	Description	Remark
1	MJPJ_N	I/O	Negative polarity of low voltage differential data signal	
2	MJPJ_P	I/O	Positive polarity of low voltage differential data signal	
3	MJPJ_CN	I	Negative polarity of low voltage differential clock signal	
4	MJPJ_CP	I	Positive polarity of low voltage differential clock signal	
5	IM0	I	Select the RGB interface mode.	Note 3
6	IM1	I	Select the RGB interface mode.	Note 3
7	IM2	I	Select the RGB interface mode.	Note 3
8	Reset	I	Reset signal	
9	VSYNC	I	Frame synchronizing signal	
10	HSYNC	I	Line synchronizing signal	
11	DOTCLK	I	Dot clock signal	
12	ENABLE	I	A data ENABLE input signal	
13	DB17	I/O	Data input/output	
14	DB16	I/O	Data input/output	
15	DB15	I/O	Data input/output	
16	DB14	I/O	Data input/output	
17	DB13	I/O	Data input/output	
18	DB12	I/O	Data input/output	
19	DB11	I/O	Data input/output	
20	DB10	I/O	Data input/output	
21	DB9	I/O	Data input/output	
22	DB8	I/O	Data input/output	
23	DB7	I/O	Data input/output	
24	DB6	I/O	Data input/output	
25	DB5	I/O	Data input/output	
26	DB4	I/O	Data input/output	
27	DB3	I/O	Data input/output	
28	DB2	I/O	Data input/output	
29	DB1	I/O	Data input/output	
30	DB0	I/O	Data input/output	
31	SDO	O	Serial data output	
32	SDA	I/O	Serial data input/output bi-direction pin	
33	RD	I	Serve as a read signal	
34	SCL	I	Serial Clock when operates in the serial interface	
35	D/C	I	Data/Command Selection pin	
36	CSX	I	Chip select input signal	
37	GND	P	Ground	

38	IOVCC	P	Digital Power Supply	
39	IOVCC	P	Digital Power Supply	
40	VCC	P	Analog Power Supply	
41	VCC	P	Analog Power Supply	
42	GND	P	Ground	
43	LEDA	P	LED Anode	
44	LED1-	P	LED Cathode	
45	LED2-	P	LED Cathode	
46	LED3-	P	LED Cathode	
47	LED4-	P	LED Cathode	
48	LED5-	P	LED Cathode	
49	LED6-	P	LED Cathode	
50	TE	O	Tearing effect out. If not used, please open this pin.	

Note1: P: Power/GND; I: input pin; O: output

Note2: Unused I/O pin should be fixed to GND level.

Note3: System interface select

IM2	IM1	IM0	RGB-interface Mode	DB pin in use	Colors
0	0	0	DBI Type B 24-bit (DB_EN = 1)	DB[23:0]	16.7M
0	0	0	DBI Type B 18-bit (DB_EN = 0)	DB[17:0]	262K
0	0	1	DBI Type B 9-bit	DB[8:0]	262K
0	1	0	DBI Type B 16-bit	DB[15:0]	65/262K
0	1	1	DBI Type B 8-bit	DB[7:0]	65/262K
1	0	1	DBI Type C Option 1 (3-line SPI)	SDA/SDO	8/262K
1	1	0	DSI	MIPI_DATA_P , MIPI_DATA_N, MIPI_CLOCK_P,MIPI_CLOCK_N	
1	1	1	DBI Type C Option 3 (4-line SPI)	SDA/SDO	8/262K

The interface mode is selected by IM[2:0], as the table above.

3 Absolute Maximum Ratings

3.1 Driving TFT LCD Panel

GND=0V, Ta = 25℃

Item	Symbol	Min	Max	Unit	Remark
Logic Supply Voltage	IOVCC	-0.3	3.3	V	
Analog Supply Voltage	VCC	-0.3	3.3	V	
Input Voltage	VSYNC，HSYNC，DOTCLK，ENABLE，IM0，IM1，IM2，DB[17:0]	-0.3	IOVCC+0.3		
Backlight Forward Current	I_{LED}	--	25	mA	For each LED
Operating Temperature	T_{OPR}	-20	60	℃	
Storage Temperature	T_{STG}	-30	70	℃	

4 Electrical Characteristics

4.1 LCD module

GND=0V, Ta=25℃

Item		Symbol	Min	Typ	Max	Unit	Remark
Logic Supply Voltage		IOVCC	1.65	1.8	3.3	V	
Analog Supply Voltage		VCC	2.5	2.8	3.3	V	
Input Signal Voltage	Low Level	VIL	-0.3	-	0.3*IOVCC	V	VSYNC，HSYNC，DOTCLK，ENABLE，IM0，IM1，IM2，DB[17:0]
	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
Output Signal Voltage	Low Level	VIL	0	-	0.2*IOVCC	V	
	High Level	VIH	0.8*IOVCC	-	IOVCC	V	
(Panel+LSI) Power Consumption		Black Mode	--	--	--	mW	
		Sleeping Mode	--	--	--	mW	
		Standby Mode	--	--	--	uW	

Table 4.1 LCD module electrical characteristics

4.2 Driving Backlight

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	--	20	--	mA	For each LED
Forward Current Voltage	V_F	--	3.2	--	V	For each LED
Backlight Power Consumption	W_{BL}	--	384	--	mW	For 6 LED

Table 4.2 backlight unit electrical characteristics

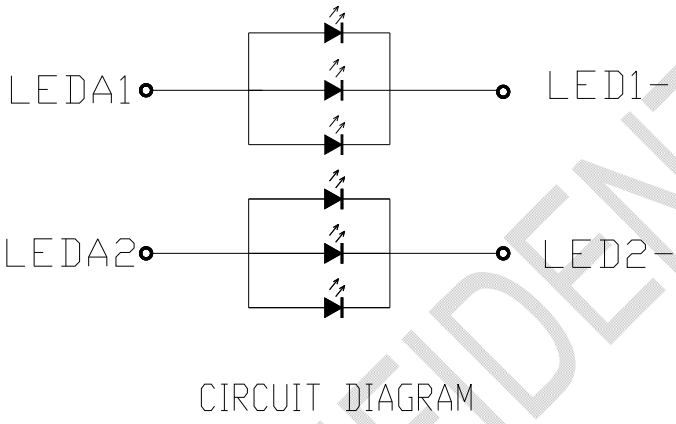
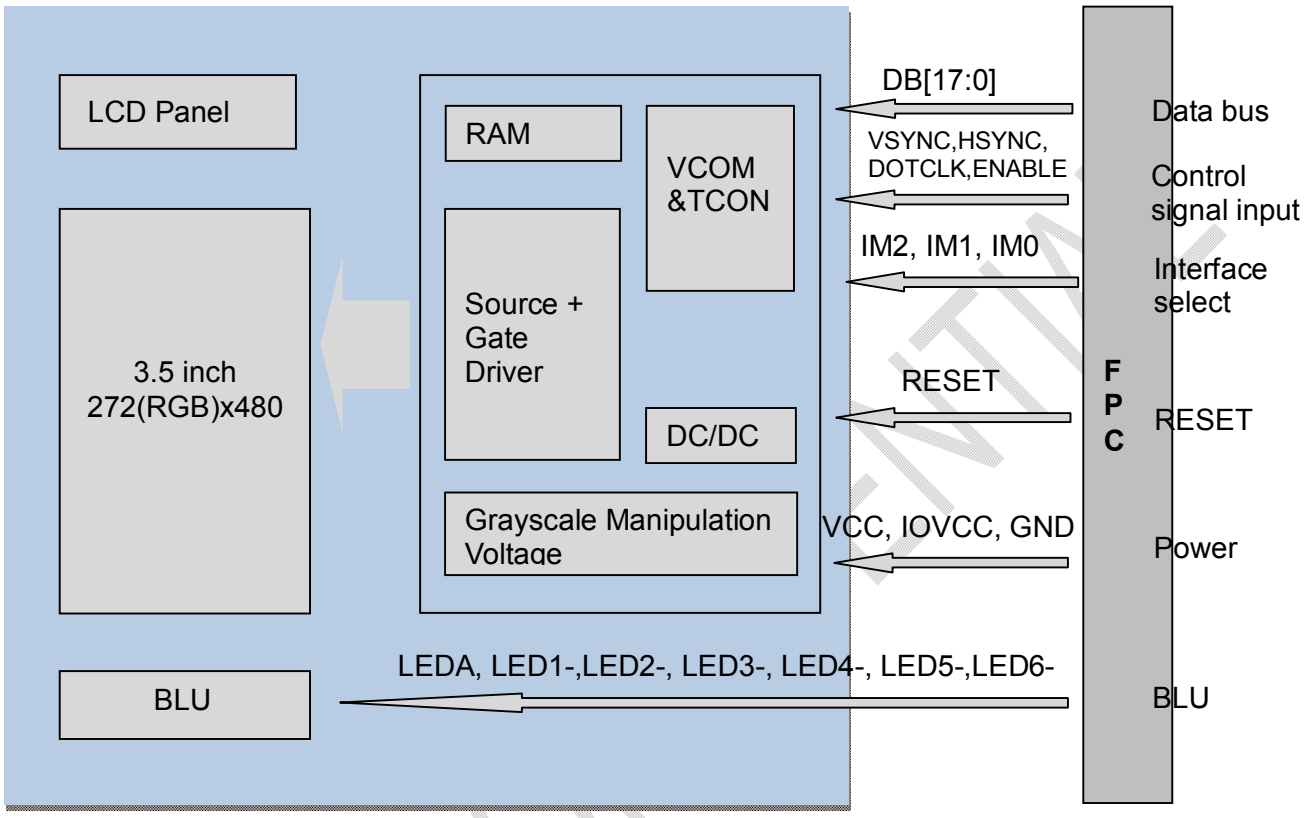


Figure 4.2 LED circuit structure

4.3 Block Diagram

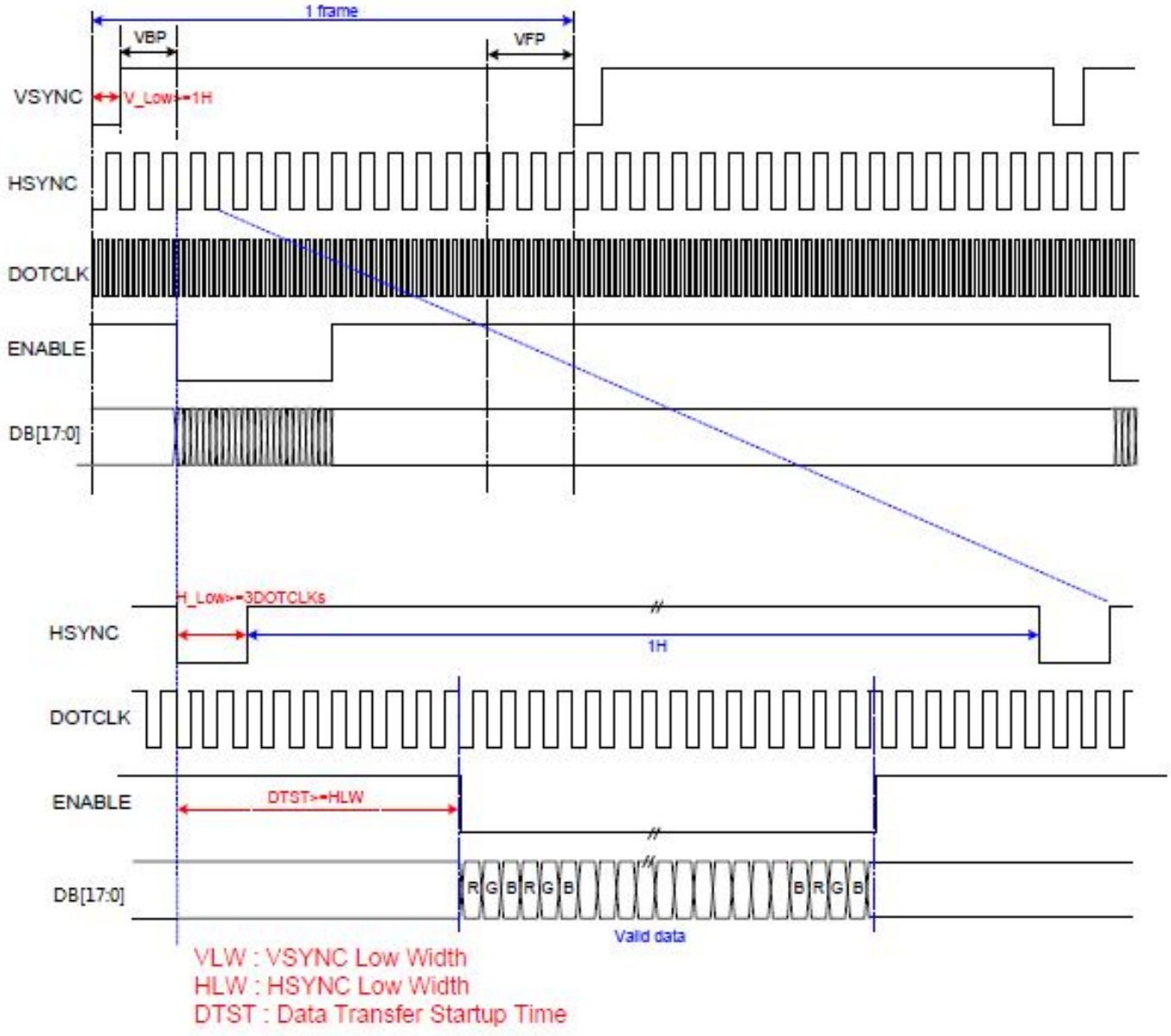
LCD module diagram



5 Data input timing

5.1 DPI type

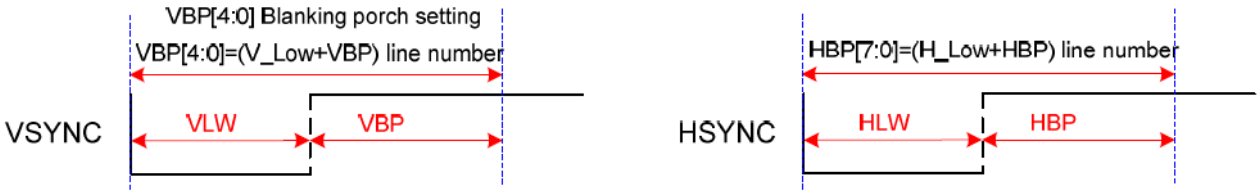
5.1.1 18-bit DPI interface timing chart



5.1.2 Interface Timing Parameters

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low+HBP <192	DOTCLK
Horizontal Back Porch	HBP	3	-		DOTCLK
Horizontal Front Porch	HFP	3	-	255	DOTCLK
Horizontal Address	HACT	-	272	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low+VBP+VFP < 32	Line
Vertical Back Porch	VBP	2	-		Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		100	-	50	ns
DOTCLK Frequency		10	-	20	MHz

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:

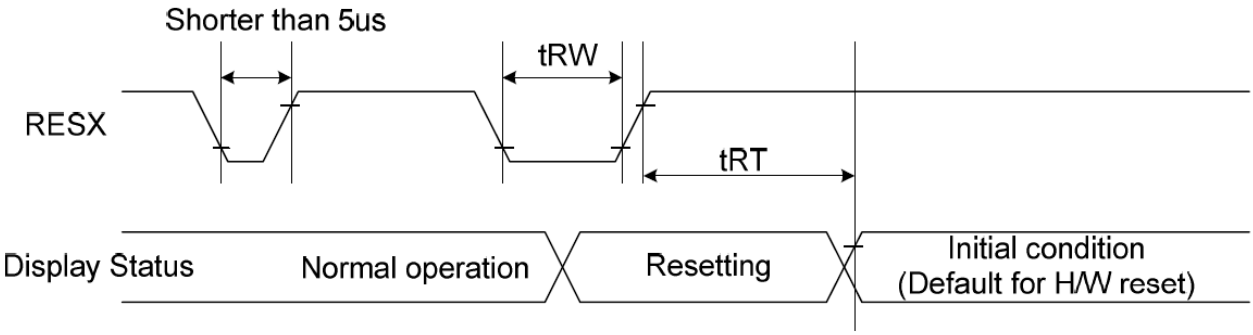


5.1.5 DPI Interface input format

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

5.2 Reset Timing



Reset input timing

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
T_{RW}	Reset pulse duration	10	-	-	us
T_{RT}	Reset cancel	-	-	5	ms
			-	120	ms

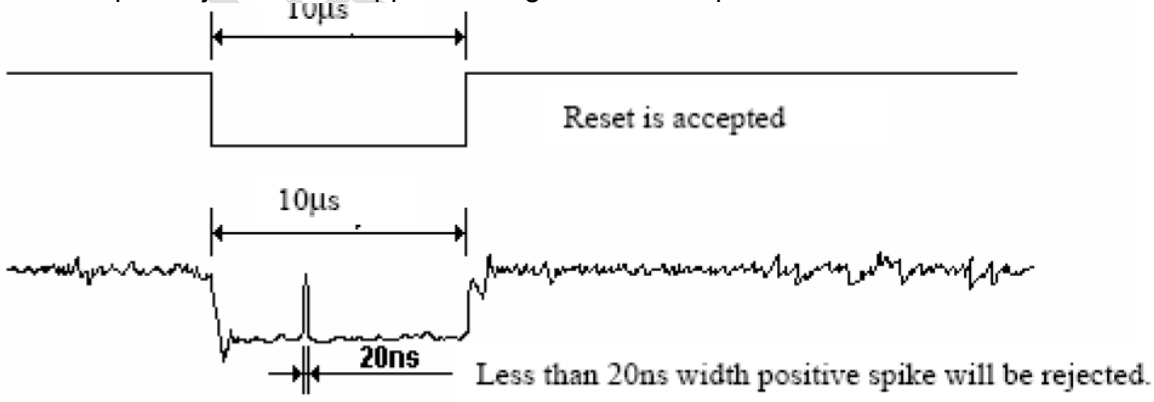
Note 1: The reset cancel include also required time for loading ID bytes, VCOM setting and other setting from EEPROM to registers. This loading is done every time when there is a HW reset cancel time (T_{RT}) within 5 ms after a rising edge of RESX.

Note 2: According to the table below, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Resx Pulse	Action
Shorter than 5 us	Reset Rejected
Longer than 9 us	Reset
Between 5 us and 9 us	Reset starts

Note 3: During the reset period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120 ms, when reset starts in sleep out mode. The display remains the blank state in sleep in mode.) and then return to default condition for Hardware Reset.

Note 4: Spike rejection also applies during a valid reset pulse as shown below:

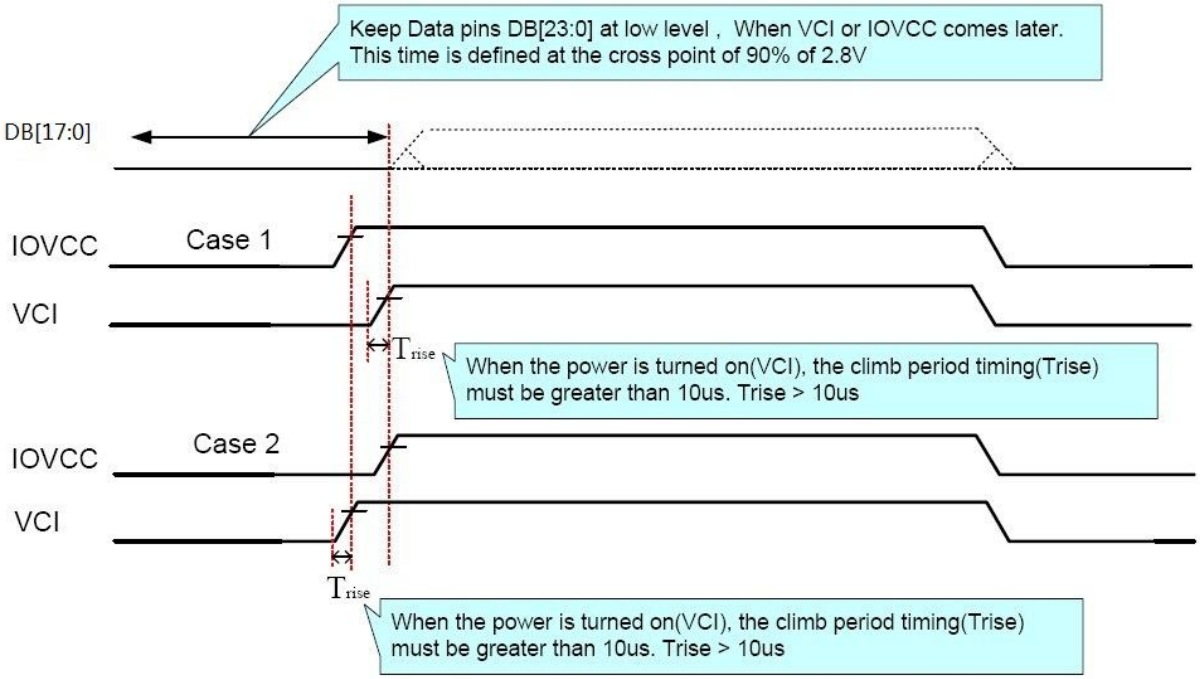


Note 5: when reset is applied during sleep in mode.

Note 6: when reset is applied during sleep out mode.

Note 7: It's necessary to wait 5 ms after releasing RESX before sending commands. Also sleep out command cannot be sent for 120 ms.

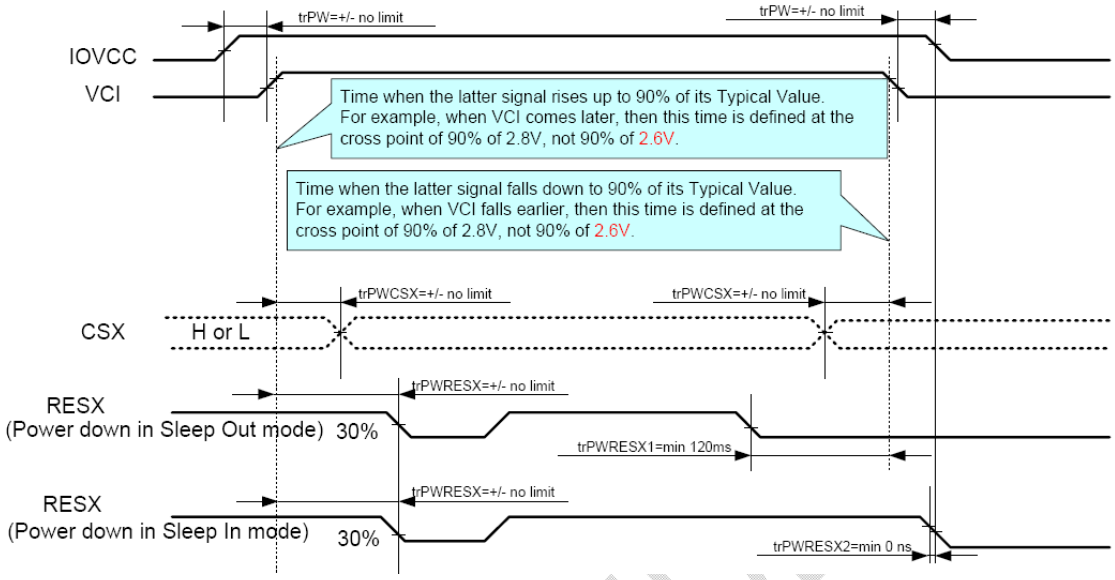
6 Power on/off sequence



Note1: Keep data pins [17:0] at low level, when VCI or IOVCC comes later.
Note2: When the power is turned on, the climb period timing (Trise) must be greater than 10 us.
Note3: If the RESX line is not steadily held by the host during the Power on Sequence, it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power on Sequence to ensure correct operation. Otherwise, all the functions are not guaranteed.

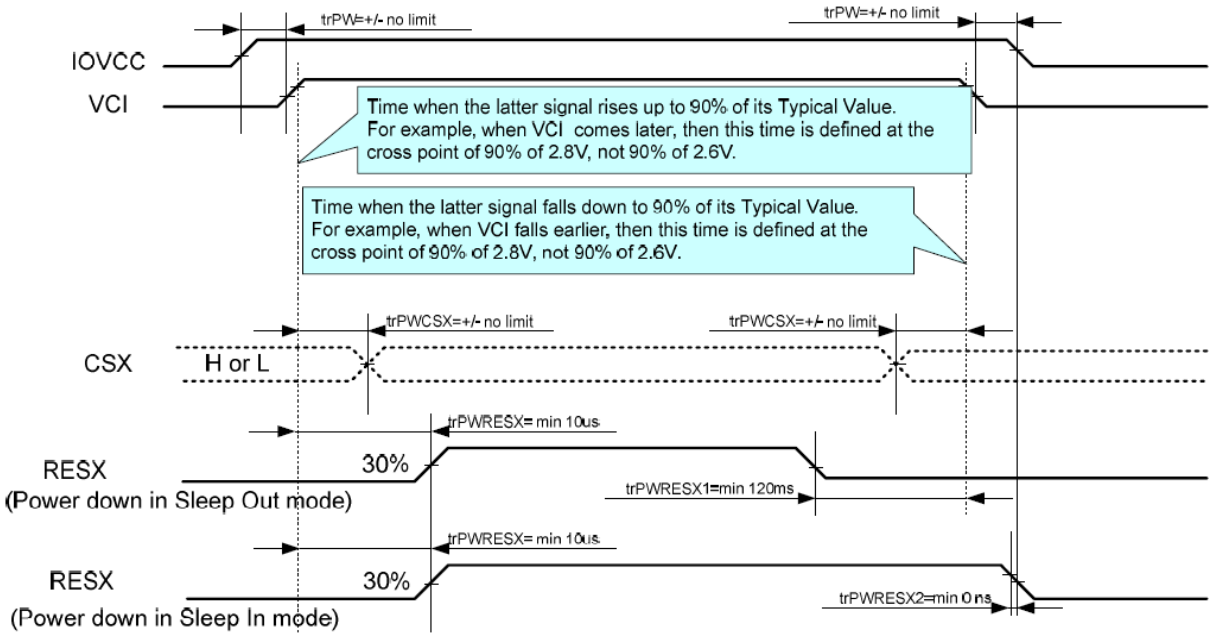
RESX line is held high or unstable by host at Power on

If the RESX line is held high or unstable by the host during Power On, then Hardware Reset must be applied after both VCI and IOVCC have been applied.



RESX line is held low by host at Power on

If the RESX line is held low (and stable) by the host during Power On, then the RESX must be held low for a minimum of 10 us after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the sleep out mode
trPWRESX2 is applied to RESX falling in the sleep in mode

7 Optical Characteristics

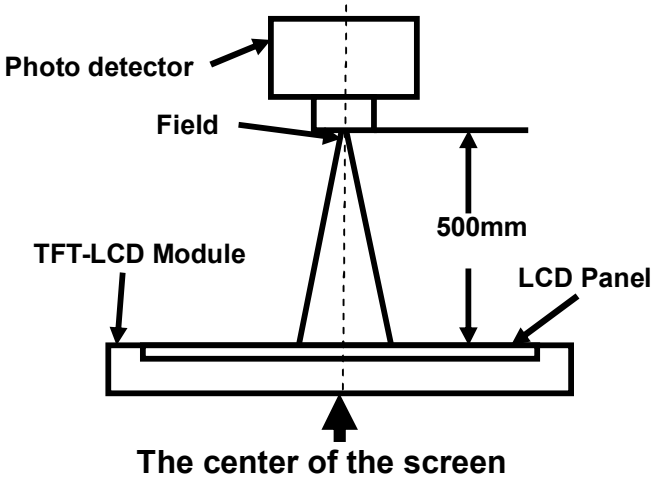
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70	--	Degree	Note2,3
		θB		60	70	--		
		θL		50	60	--		
		θR		60	70	--		
Contrast Ratio		CR	θ=0°	400	500	--		Note 3
Response Time		T_{ON}	25℃	--	20	30	ms	Note 4
		T_{OFF}						
Chromaticity	**White**	x	Backlight is on	0.258	0.308	0.358		Note 1,5
		y		0.280	0.330	0.380		
	Red	x		0.515	0.565	0.615		Note 1,5
		y		0.290	0.340	0.390		
	Green	x		0.290	0.340	0.390		Note 1,5
		y		0.540	0.590	0.640		
	Blue	x		0.100	0.150	0.200		Note 1,5
		y		0.045	0.095	0.145		
Uniformity		U		--	80	--	%	Note 6
NTSC				--	50	--	%	Note 5
Luminance		L		250	300		cd/m^2	Note 7

Test Conditions:

1. I_F= 20 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

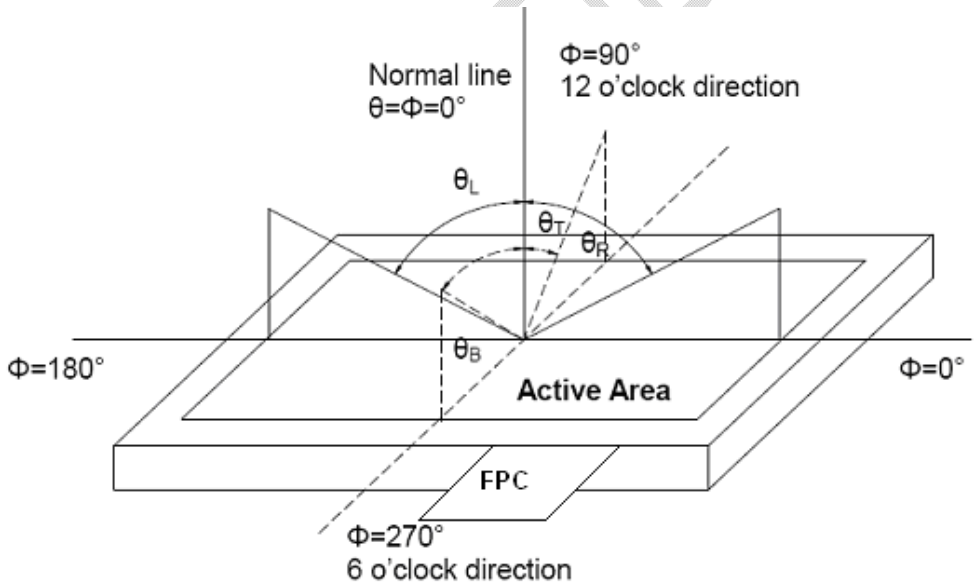
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

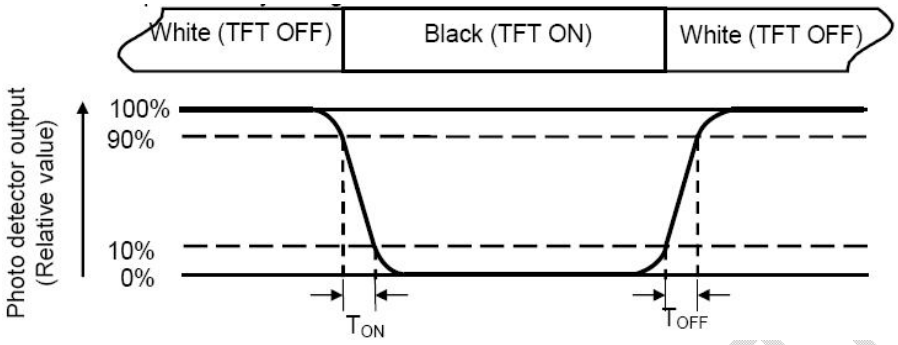
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

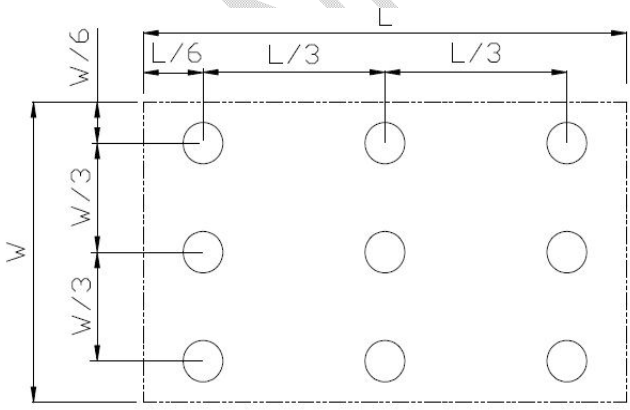
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

8 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts = +60℃, 240 hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta = -20℃, 240 hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta = +70℃, 240 hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta = -30℃, 240 hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	Ta = +60℃, 90% RH max,240hours	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 20 Cycle	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	ESD	C=150pF,R=330Ω,5point/panel Air:±8Kv,5times; Contact:±4Kv,5times (Environment:15℃~35℃, 30%~60%.86Kpa~106Kpa)	IEC61000-4-2:2001 GB/T17626.2-2006
8	Package Vibration Test	2~12~100~300Hz,0.0002~0.01~0.01~0.00001 g2/Hz，30min for each direction of X/Y/Z	GB/T 4857.23-2003
9	Package Drop Test	Height: 60cm 1corner,3edges,6surfaces	IEC60068-2-32:1990 GB/T2423.8—1995

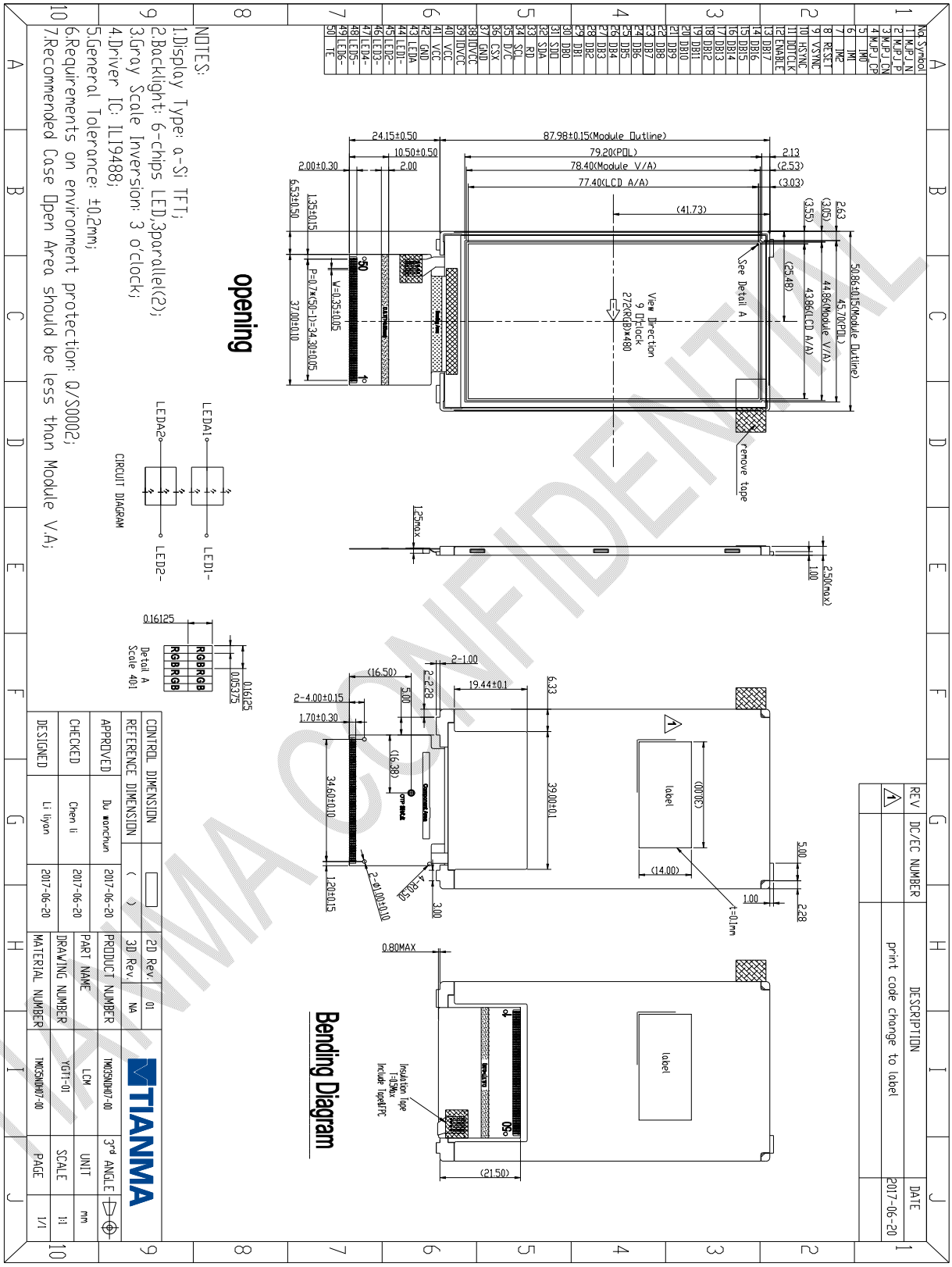
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

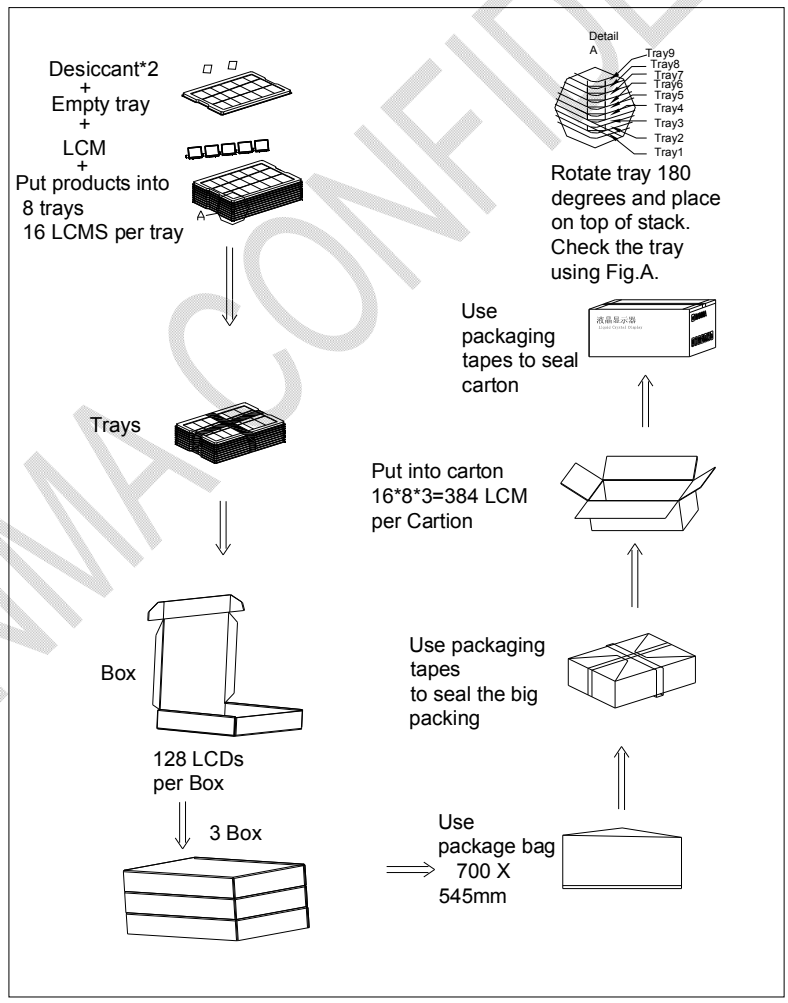
9 Mechanical Drawing



10 Packing Drawing

No	Item	Model(Material)	Dimensions (mm)	Unit weight (Kg)	Quantity	Remark
1	LCM module	TM035NDH07-00	50.86x87.98x2.50	0.0212	384	
2	Desiccant	Desiccant	45x35	0.002	6	
3	Tray	PET	485x330x12.1	0.156	27	Anti-static
4	Dust-Proof Bag	PE	700x545	0.021	1	
5	Box	Corrugate paper	520x345x74	0.227	3	
6	Carton	Corrugate paper	544x365x250	1.01	1	
7	Total weight	14.07±5%				

Note：Packaging specification and quantity.
1. LCD quantity per tray:6 row x 2 column +4=16.
2. Module quantity in a carton: NO. of PS trays 24x quantity per tray 16=384 pcs.



11 Precautions for Use of LCD Modules

1.1 Handling Precautions

1.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

1.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

1.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

1.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

1.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

1.1.6 Do not attempt to disassemble the LCD Module.

1.1.7 If the logic circuit power is off, do not apply the input signals.

1.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

1.1.8.1 Be sure to ground the body when handling the LCD Modules.

1.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

1.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

1.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

1.2 Storage precautions

1.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

1.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

1.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

1.3 Transportation Precautions

1.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.