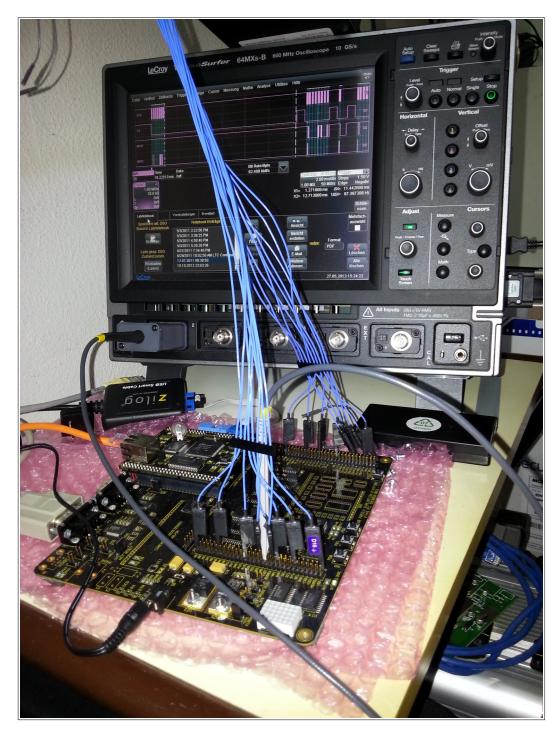
This file is part of the FreeRTOS port for ZiLOG's EZ80F91 Module. Copyright (C) 2016 by Juergen Sievers <JSievers@NadiSoft.de>



The Port was made and rudimentary tested on ZiLOG's EZ80F910300ZCOG Developer Kit using ZDSII Acclaim 5.3.4 Developer

Environment and comes WITHOUT ANY WARRANTY to you!

Developer:

SIE Juergen Sievers <JSievers@NadiSoft.de>

#### Repository directories:

- CPM CP/M 2.2 source and environment.
- doc some documantation.
- FreeRTOS the modified FreeRTOS real time kernel source code.
- FreeRTOSCLI the FreeRTOS-Plus-CLI command line interface source code.
- FreeRTOSTCP the modified FreeRTOS-Plus-TCP TCP/IP source code.
- Inc The Demo's header files.
- monitor Z80 machine monitor. (not usable yet)
- src The Demo's source files.
- uzlib The compress/un-compress library

See http://www.freertos.org.html for full details of the FreeRTOS directory structure and information on locating the files you require.

# My Build- and Test-environment:

I use a Fedora Linux Workstation as host system. On this host a Windows 10 is running as guest under QEMU. On Windows I mount a samba share as drive Z: with at least the following directories.

### 1. Z:\ZDSII\_eZ80Acclaim!\_5.3.4

ZiLOG Developer Studio II—eZ80Acclaim!® installation. Free download from <a href="https://www.zilog.com">www.zilog.com</a>.

#### 2. Z:\workspace

The Target is connected over its Serial and Ethernet port on the Linux-PC

The Debug-output uses target's serial-port 0 115200,8,1,n,RTS/CTS. I use PuTTY on the Linux-PC to display such information.

```
A 11
B 6

UT 0:1:32 332ms
UT 0:1:32 284ms

eZ80 tty
11223344->44332211->3351057p
prvIPTask started
Link ...... ENAC 100MBPS, FULL_DUPLEX, Link up
prvInitialiseDHCP: start after 318767354 ticks
Socket 4040 -> 0.0.0.0:0 State eCLOSED->=TCP_LISTEN
VDHCPProcess: discover
VDHCPProcess: discover
VDHCPProcess: timeout 10000 ticks
VDHCPProcess: timeout 20000 ticks
VDHCPProcess: rimeout 20000 ticks
VDHCPProcess: rimeout 20000 ticks
VDHCPProcess: effer 192.168.77.24
VDHCPProcess: effer 192.168.77.24
VDHCPProcess: acked 192.168.77.24
VDHCPProcess: acked 192.168.77.24
NETWORKEVentHook eNetworkEvent:0
IP Address: 192.168.77.24
Subnet Mask: 255.255.55.0
Gateway IP Address: 192.168.77.1
DNS server IP Address: 192.168.77.1
DNS server IP Address: 192.168.77.1
DNS server iP Tybrime1.ptb.de' @ 192.53.103.108
DNS[0x00000]: The answer to 'ptbtime1.ptb.de' (192.53.103.108) will be stored
```

On the Linux-PC also runs a DHCP-Server with will answer to the target's DHCP Requests.

At last the ZiLOG USBSmartCable is connect between the target and Lunux-PC. This

USB -Device is routed to the Windows guest. It will be used by ZiLOG's Developer Studio for download, flashing and debugging.

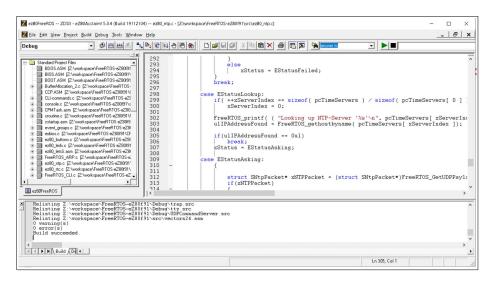
Changing to directory Z:\workspace (or on the linux to the shared) and clone the project <a href="https://github.com/notwendig/FreeRTOS-eZ80f91.git">https://github.com/notwendig/FreeRTOS-eZ80f91.git</a> including submodules.

Apply the patch to zulib.

On the Windows-guest run the ZiLOG Developer Studio. Open the Project-file Z:\workspace\FreeRTOS-eZ8091\uzib.zdsproj and build the uzlib[d].lib.

On a linux terminal change to directory uzlib and type make to build the packer/unpacker. Change to CPM directory and type make to build the CP/M 2.2 boot-tracks and the Disk-Image as packed C-Array.

Now you are ready to open and build the z80FreeROS.zdsproj, and build it.



Before you download and run the Demo to the Target, a terminal (PuTTY) should be running on the target's serial-port connection.

After the target has gotten it's IP you may start several other connection to the target.

## Regards

Jürgen