Sheet: LPC313x

File: LPC313x_DevBoard-LPC313x.sch

Sheet: RAM_MMC

File: LPC313x_DevBoard-RAM_MMC.sch

Double click inside the boxes to jump
to the corresponding schematic page

Use mouse wheel to zoom in and out

Sheet: NAND

File: LPC313x_DevBoard-NAND.sch

Sheet: Connectors_JTAG

File: LPC313x_DevBoard-Connectors_JTAG.sch

Sheet: Power

File: LPC313x_DevBoard-Power.sch

Sheet: Vias

File: LPC313x_DevBoard-Vias.sch

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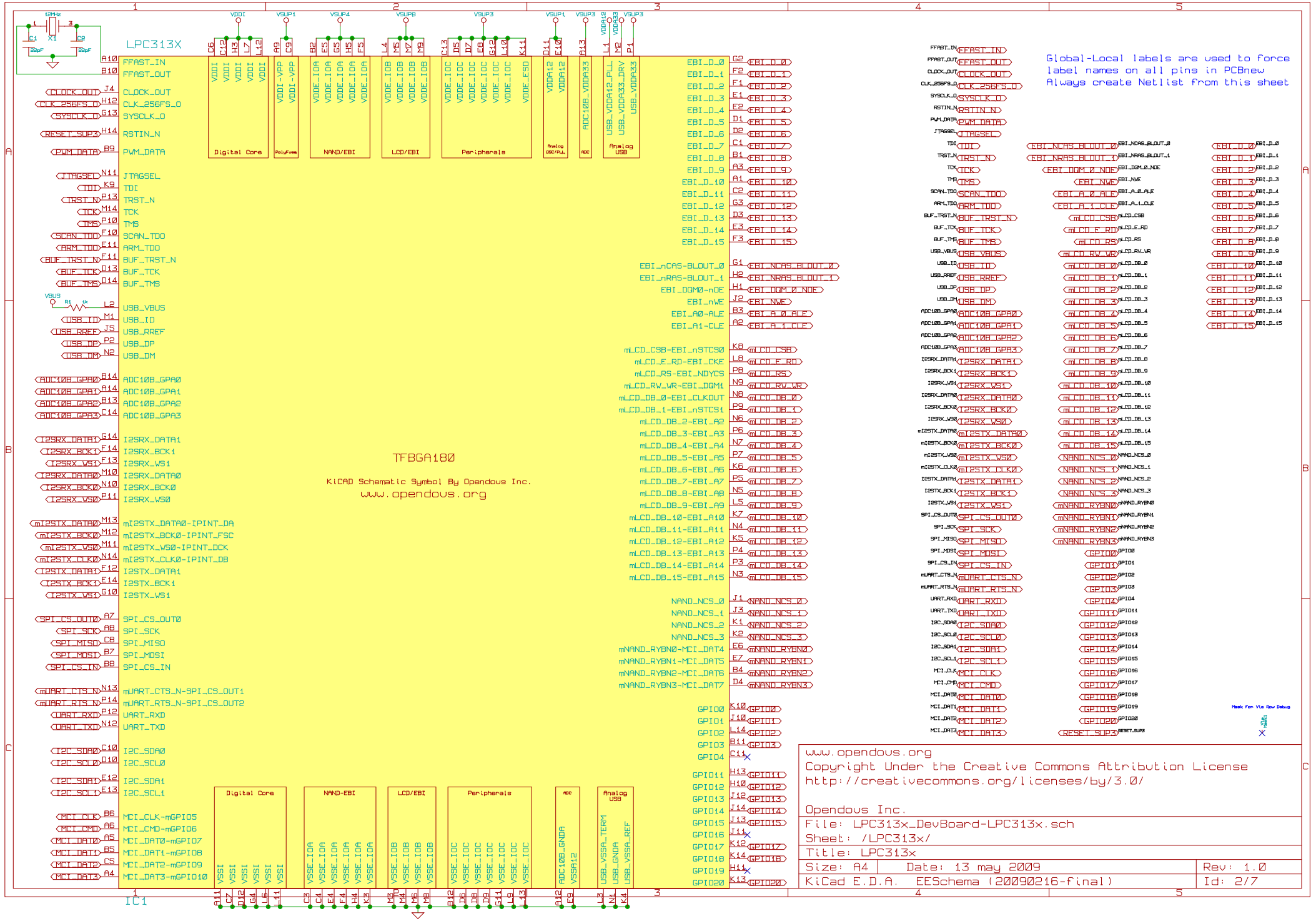
File: LPC313x_DevBoard.sch
Sheet: /
Title: LPC313x_DevBoard

Size: A4	Date: 13 may 2009	Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)		Id: 1/7


LPC313X
TFBGA180
KiCAD Schematic Symbol By Opendous Inc.
www.opendous.org
IC1
Global-Local labels are used to force label names on all pins in PCBnew
Always create Netlist from this sheet
Digital Core
NAND-EBI
LCD/EBI
Peripherals
ADC
Analog USB
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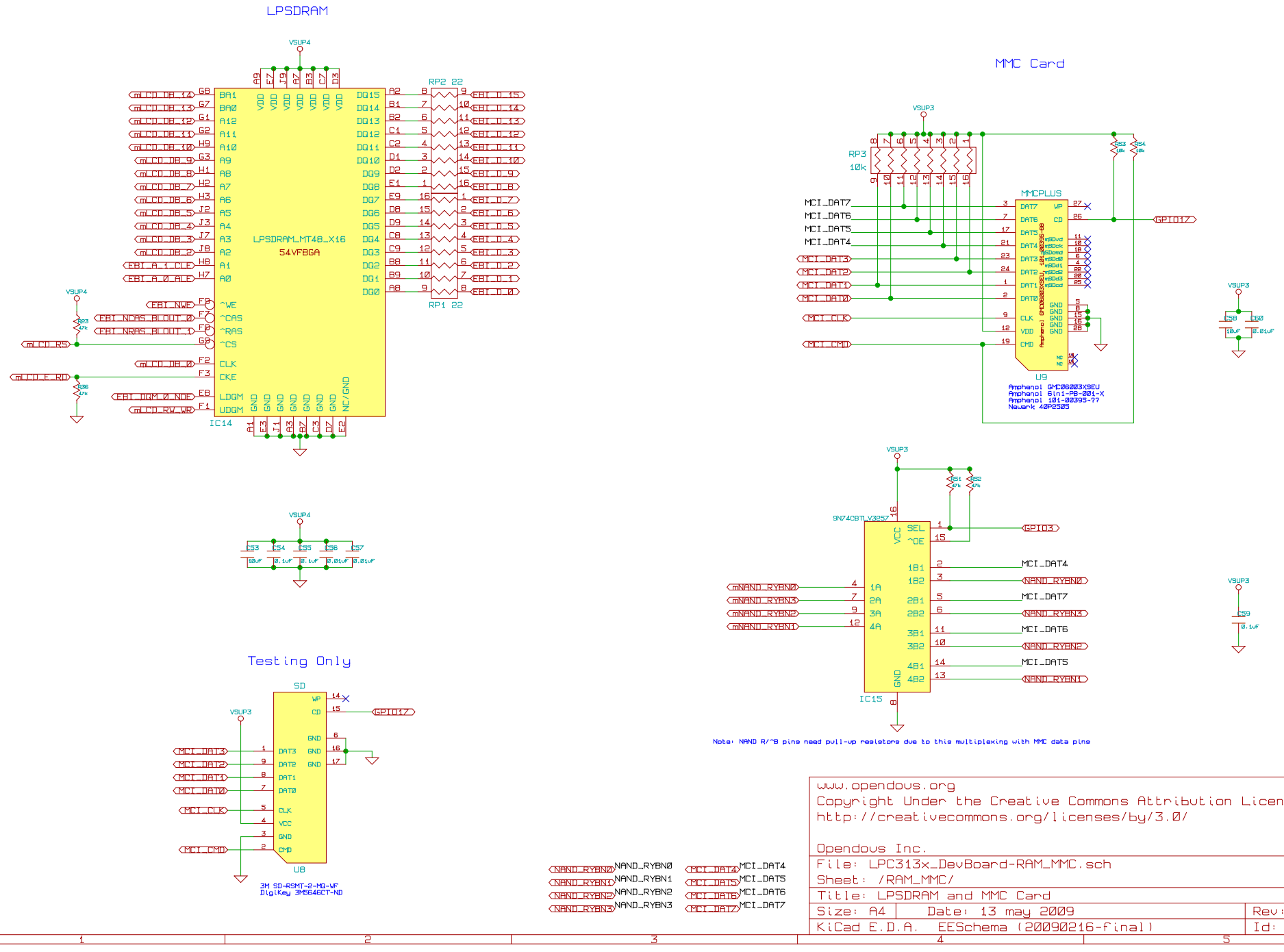
Opendous Inc.
File: LPC313x_DevBoard-LPC313x.sch
Sheet: /LPC313x/
Title: LPC313x
Size: A4
Date: 13 may 2009
Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)
Id: 2/7


LPSDRAM
LPSDRAM_MT48_X16
54VFBGA
IC14
RP2 22
RP1 22
MMC Card
MMCPLUS
U9
Amphenol GM106003X9EU
Amphenol 6ini-PB-001-X
Amphenol 101-00395-??
Newark 40P2525
RP3
10k
SN74CBT_V3257
IC15
Note: NAND R/^B pins need pull-up resistors due to this multiplexing with MMC data pins
Testing Only
SD
U8
3M SD-RSMT-2-MQ-WF
DigiKey 3MS646CT-ND
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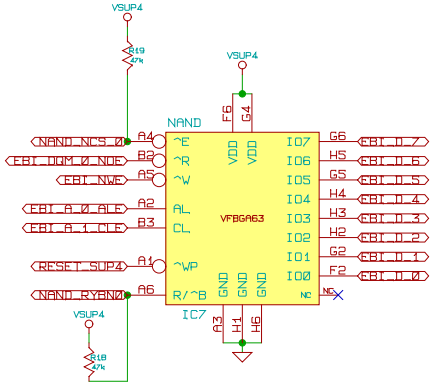
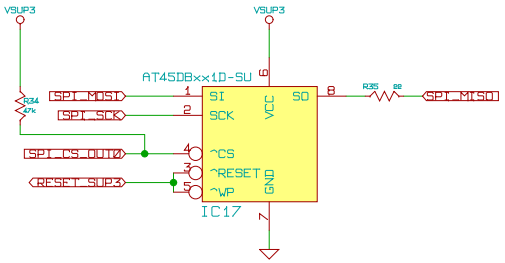
File: LPC313x_DevBoard-RAM_MMC.sch
Sheet: /RAM_MMC/
Title: LPSDRAM and MMC Card
Size: A4
Date: 13 may 2009
Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)
Id: 3/7

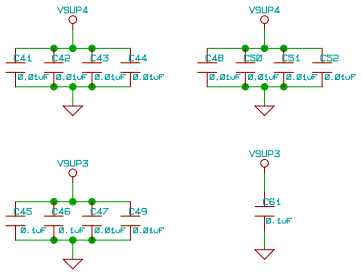
NAND



SPI Boot Flash

(Optional)





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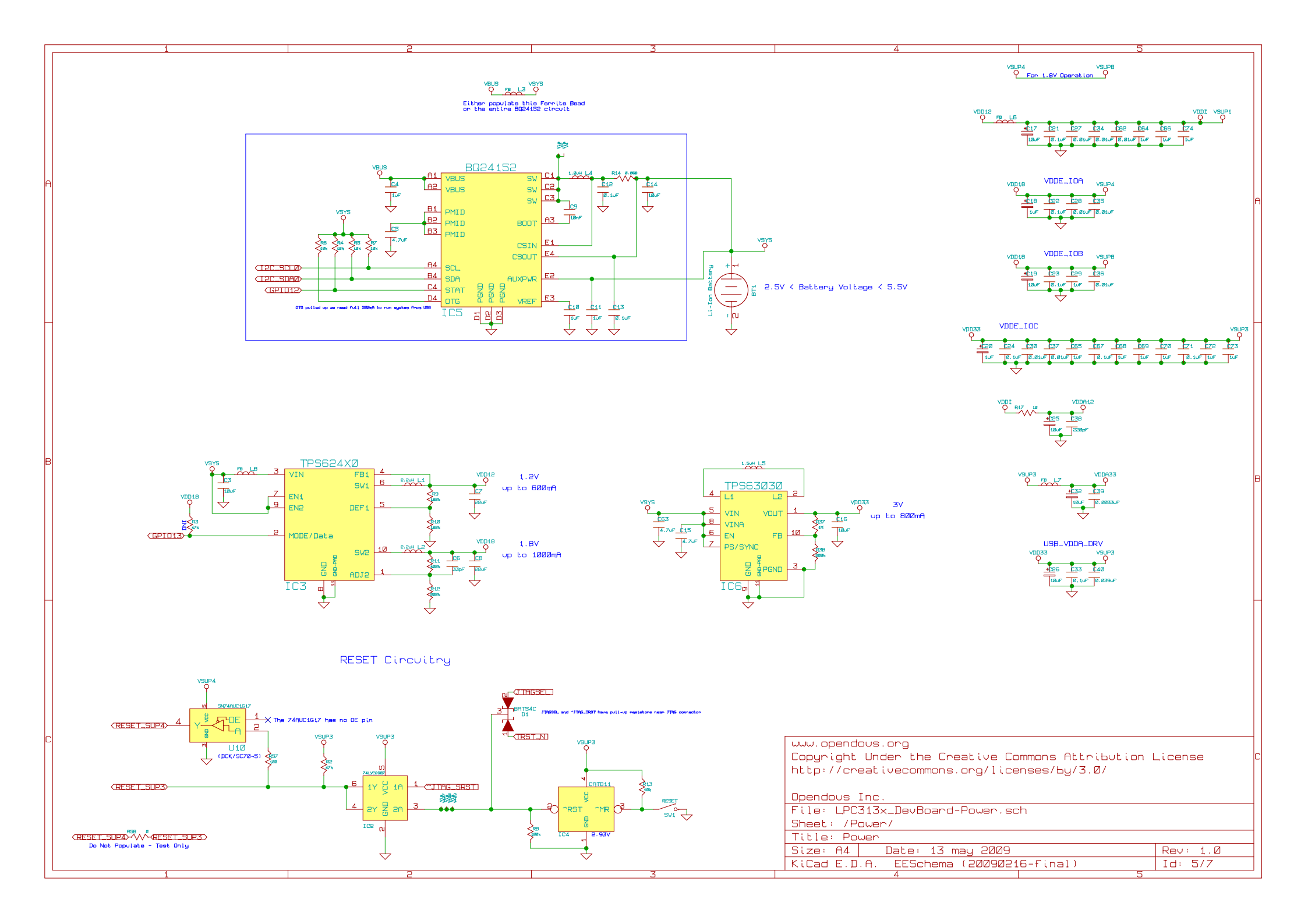
File: LPC313x_DevBoard-NAND.sch		
Sheet: /NAND/		
Title: NAND		
Size: A4	Date: 13 may 2009	Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)		Id: 4/7


Either populate this Ferrite Bead
or the entire BQ24152 circuit
BQ24152
IC5
2.5V < Battery Voltage < 5.5V
For 1.8V Operation
VDDE_IOA
VDDE_IOB
VDDE_IOC
TPS624X0
IC3
1.2V
up to 600mA
1.8V
up to 1000mA
TPS63030
IC6
3V
up to 800mA
USB_VDDA_DRV
RESET Circuitry
The 74AUC1G17 has no OE pin
Do Not Populate - Test Only
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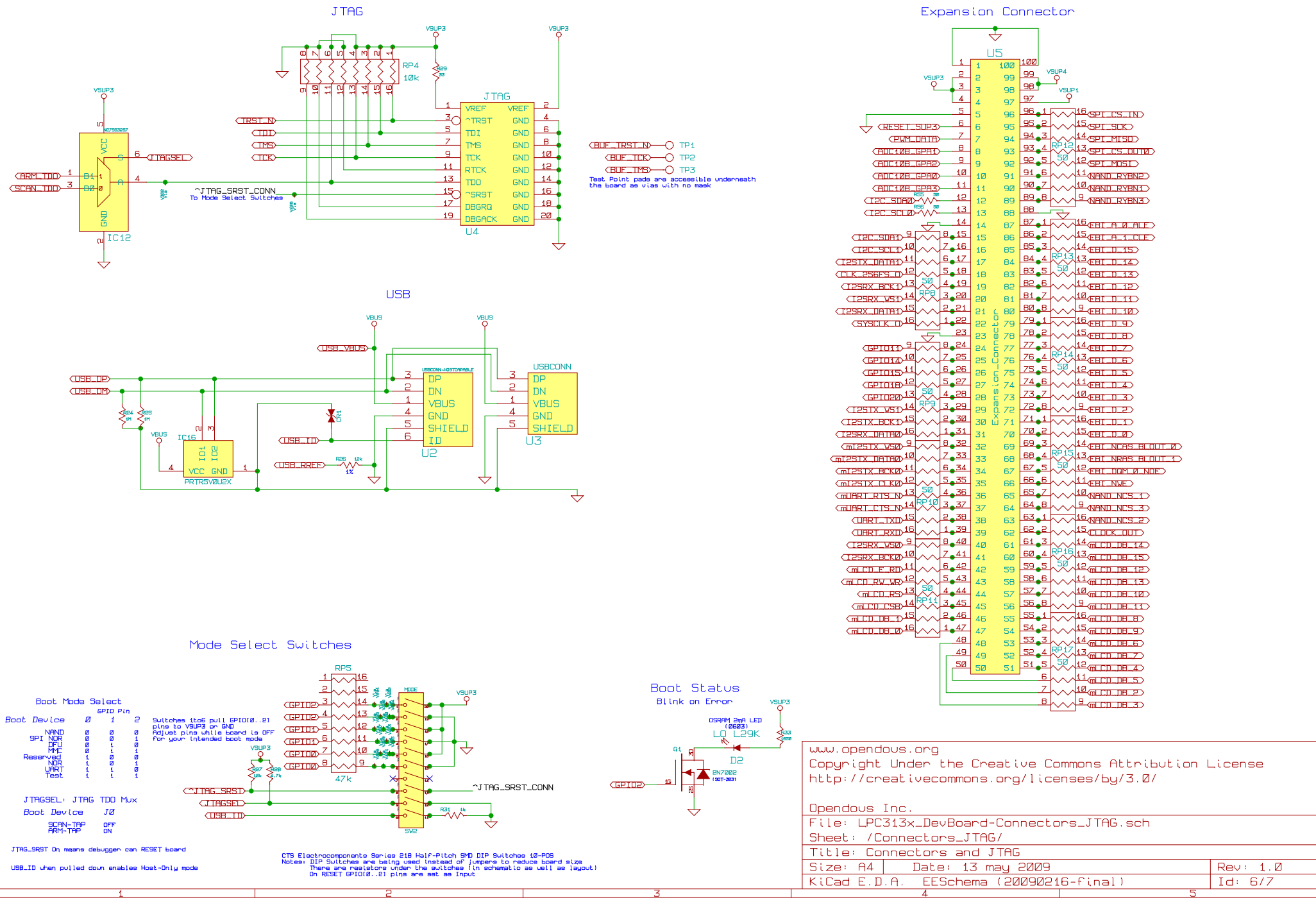
File: LPC313x_DevBoard-Power.sch
Sheet: /Power/
Title: Power
Size: A4
Date: 13 may 2009
Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)
Id: 5/7


JTAG
USB
Expansion Connector
Mode Select Switches
Boot Status
Blink on Error
Boot Mode Select
GPIO Pin
Boot Device 0 1 2
NAND 0 0 0
SPI NOR 0 0 1
DFU 0 1 0
MMC 0 1 1
Reserved 1 0 0
NOR 1 0 1
UART 1 1 0
Test 1 1 1
JTAGSEL: JTAG TDO Mux
Boot Device J0
SCAN-TAP OFF
ARM-TAP ON
JTAG_SRST On means debugger can RESET board
USB_ID when pulled down enables Host-Only mode
Switches 1to6 pull GPIO[0..21] pins to VSUP3 or GND
Adjust pins while board is OFF
For your intended boot mode
CTS Electrocomponents Series 218 Half-Pitch SMD DIP Switches 10-POS
Notes: DIP Switches are being used instead of jumpers to reduce board size
There are resistors under the switches (in schematic as well as layout)
On RESET GPIO[0..21] pins are set as Input
Test Point pads are accessible underneath the board as vias with no mask
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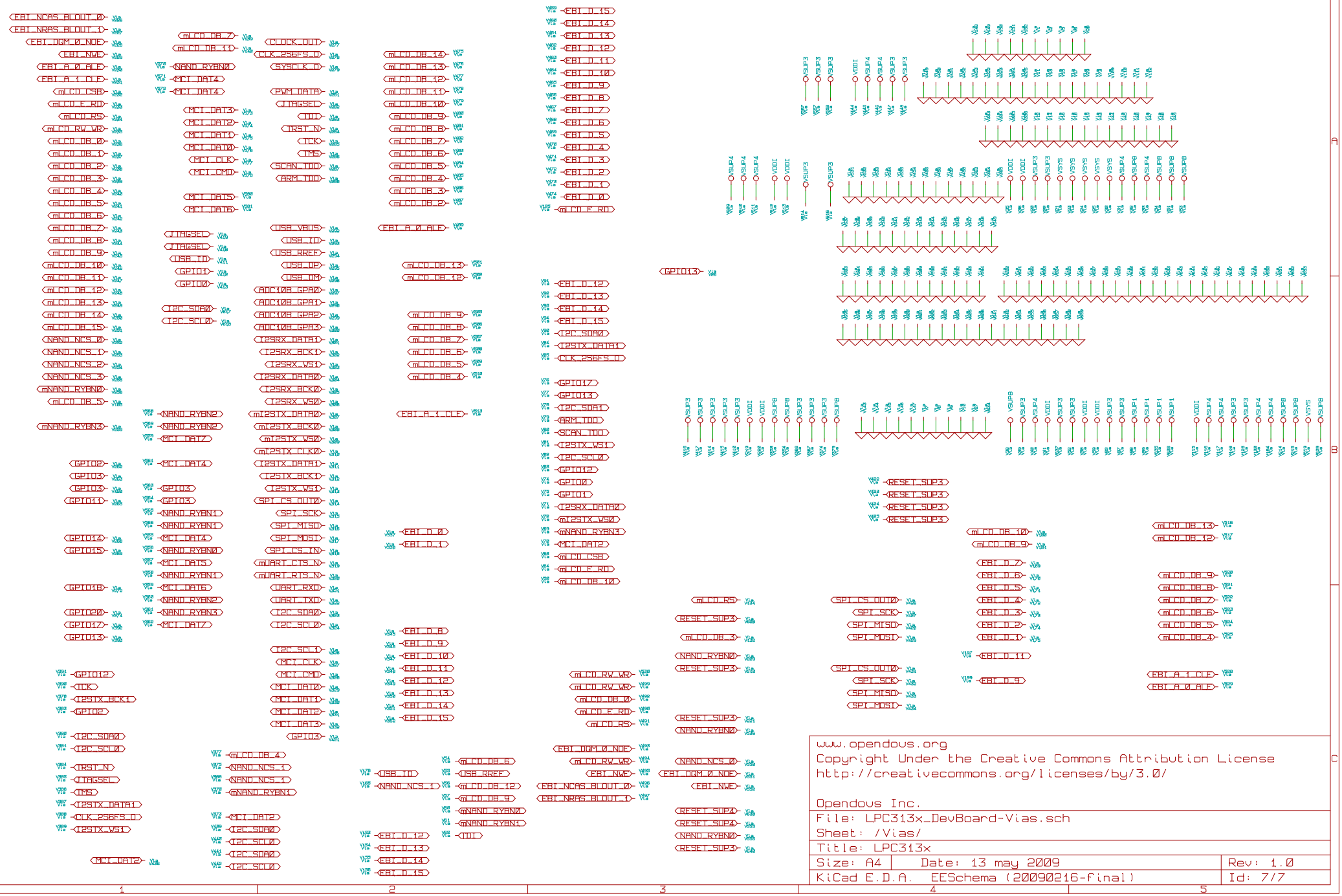
File: LPC313x_DevBoard-Connectors_JTAG.sch
Sheet: /Connectors_JTAG/
Title: Connectors and JTAG
Size: A4
Date: 13 may 2009
Rev: 1.0
KiCad E.D.A. EESchema (20090216-final)
Id: 6/7

When routing a board this complex, it helps to have persistant vias (vias that behave like components)