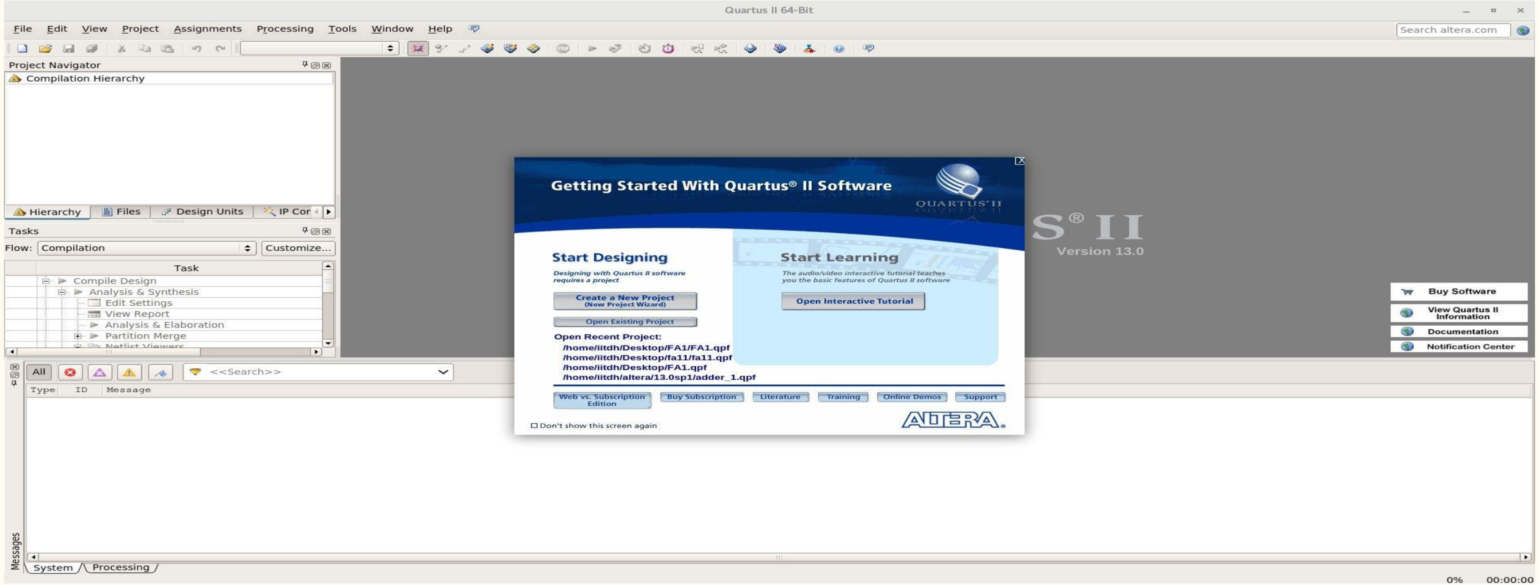
Introduction to CPLD & VHDL

Introduction

Steps to write VHDL code, dump it in CPLD and verify the written code functionality.

Step 1: Open Quartus II software.



Getting Started With Quartus® II Software

Start Designing

Designing with Quartus II software requires a project

Open Recent Project:

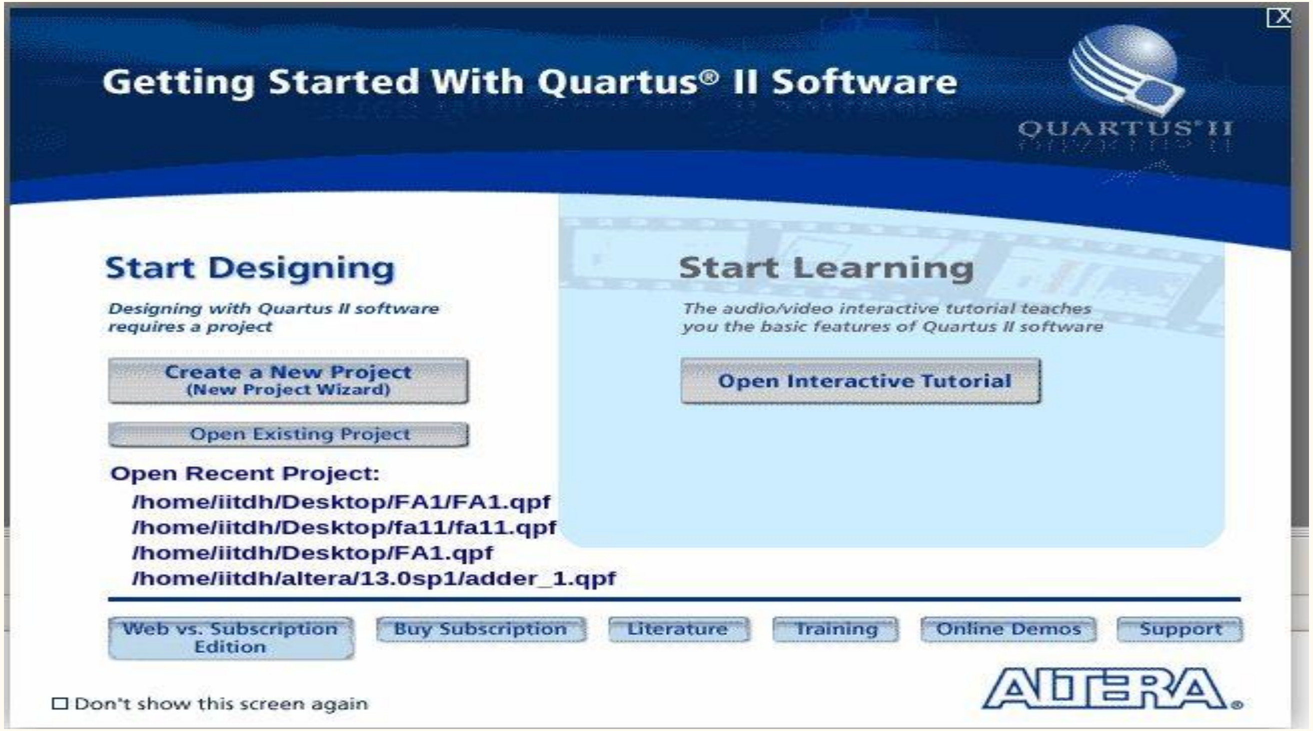
/home/iitdh/Desktop/FA1/FA1.qpf
/home/iitdh/Desktop/fa11/fa11.qpf
/home/iitdh/Desktop/FA1.qpf
/home/iitdh/altera/13.0sp1/adder_1.qpf

Start Learning

The audio/video interactive tutorial teaches you the basic features of Quartus II software

□ Don't show this screen again

Step 2: Creating new project



Getting Started With Quartus® II Software

Start Designing

Designing with Quartus II software requires a project

Open Recent Project:

/home/iitdh/Desktop/FA1/FA1.qpf
/home/iitdh/Desktop/fa11/fa11.qpf
/home/iitdh/Desktop/FA1.qpf
/home/iitdh/altera/13.0sp1/adder_1.qpf

Start Learning

The audio/video interactive tutorial teaches you the basic features of Quartus II software

□ Don't show this screen again

Click on ” Create a new Project”

Step 2: Creating new project

“New project wizard” opens.

Click on”Next”
Provide the directory where the project must be

placed. Provide the project name and the entity name.

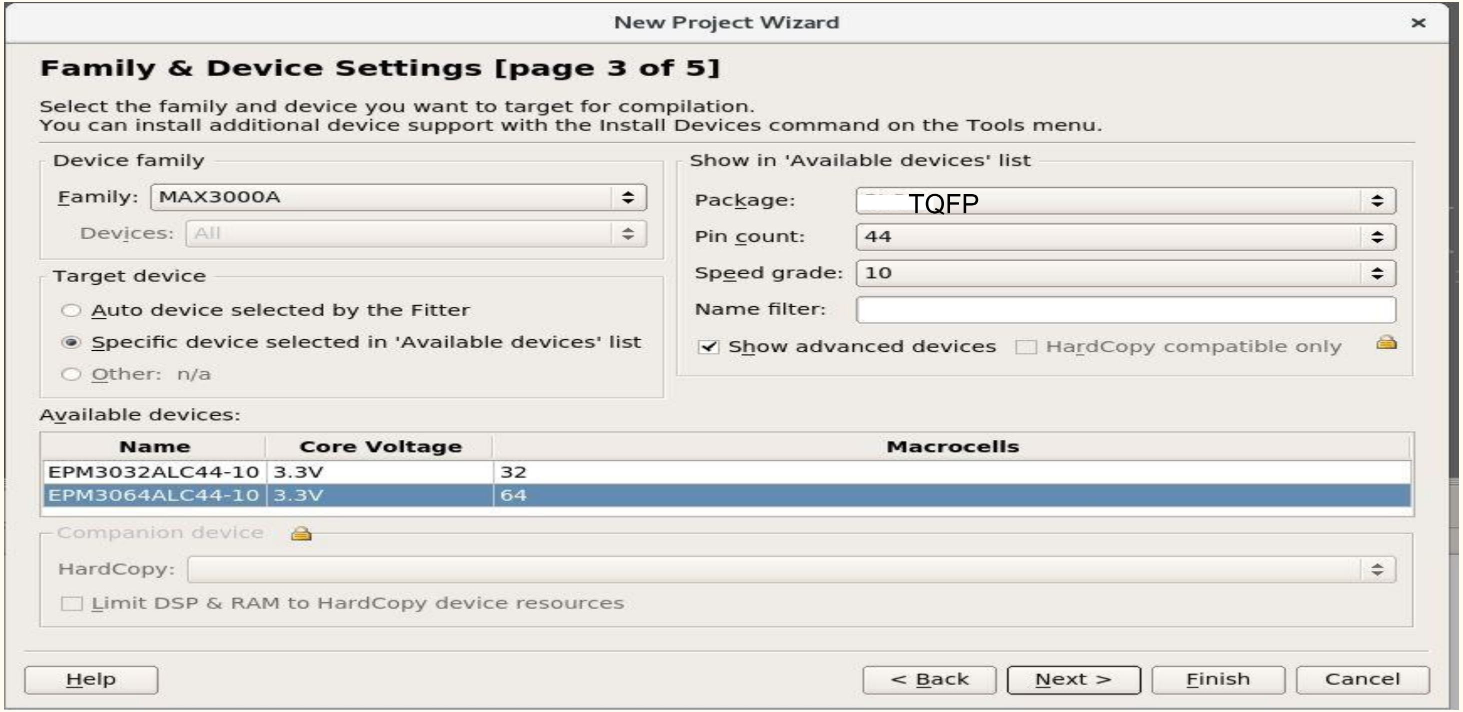
Note that project name and entity name must be same.

Click on “Next”.

Click on “Next”.

Step 2: Creating new project

Select the device, package,pin count, speed and core voltage as shown in the figure.



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: MAX3000A

Devices: All

Target device

○ Auto device selected by the Fitter

● Specific device selected in 'Available devices' list

○ Other: n/a

Show in 'Available devices' list

Package: TQFP

Pin count: 44

Speed grade: 10

Name filter:

☑ Show advanced devices □ HardCopy compatible only

Available devices:

Name	Core Voltage	Macrocells
EPM3032ALC44-10	3.3V	32
EPM3064ALC44-10	3.3V	64

Companion device

HardCopy:

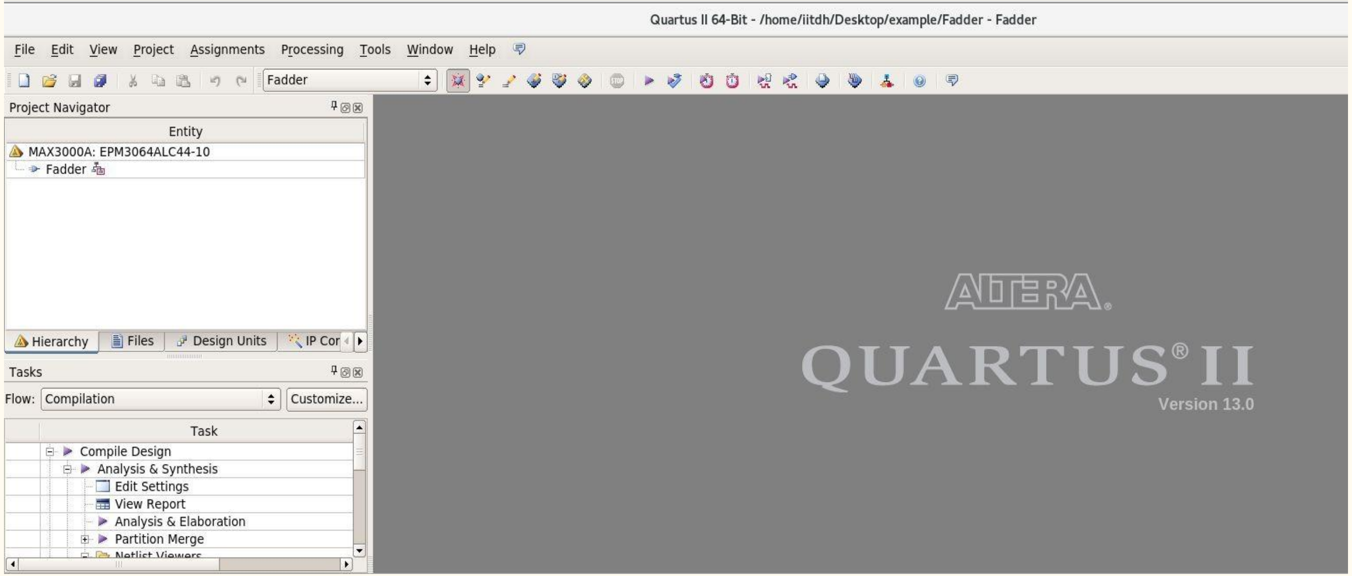
□ Limit DSP & RAM to HardCopy device resources

Step 2: Creating new project

Click on”Next”

Click on”Finish”.

Check if the project created appears in the project window.



Quartus II 64-Bit - /home/iitdh/Desktop/example/Fadder - Fadder

Project Navigator

Entity
MAX3000A: EPM3064ALC44-10
Fadder

Tasks

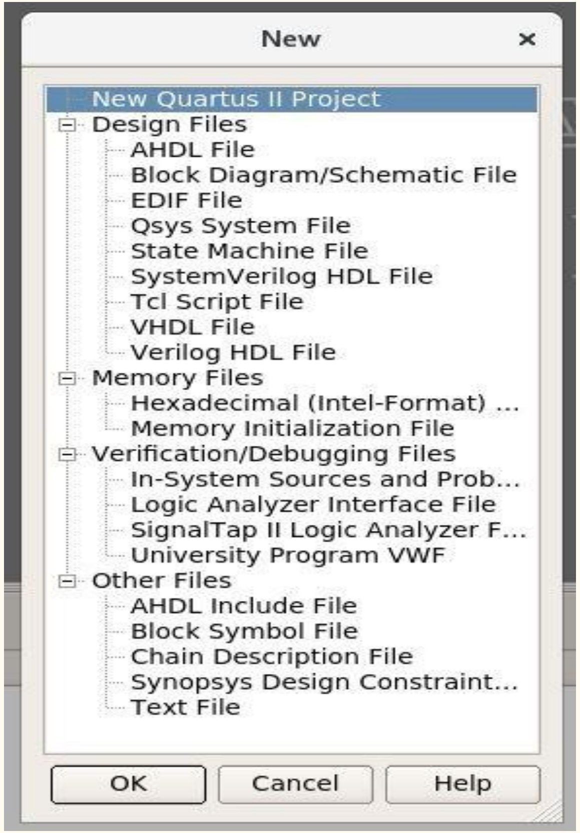
Flow: Compilation

Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers

Step3: Creating and compiling a File.

File -> New
Select “vhdl file” under Design files category. A vhdl file with “.vhd” extension opens.

Type the VHDL code and save the file in the project directory.



VHDL Code for a full adder (example)

```
library ieee;
use ieee.std_logic_1164.all;

entity fulladder is

port(a, b, c: in bit;

sum, carry : out bit);

end fulladder;

architecture dataflow of fulladder is

begin


sum <= a xor b xor c;
carry <= (a and b) or ((a xor b) and c);

end dataflow;
```

Step3: Creating and compiling a File.

To compile the code:

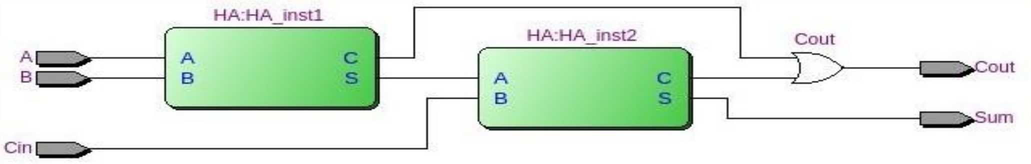
Processing-> start compilation.

The compilation will be done and if any errors (syntax) will be listed down in the messages window. If no errors then successful compilation message appears.

Step4: View RTL schematic of the written vhdl code.

Tools->Netlist viewer->RTL viewer.

This provides the equivalent high level circuit for the written code.



Sample RTL for a Full adder VHDL code.