Single Cycle Processor Report

8th March, 2024

1. Introduction

This report documents the development of a single cycle processor simulator for ToyRISC ISA. The simulator is implemented in Java and adheres to the specifications provided in the description. The primary goal of this part of the project is to simulate the execution of ToyRISC programs and generate statistics regarding the number of instructions executed and cycles taken.

2. Implementation Details

2.1 Simulation of the program

The simulation of the program involves five stages of the processor, which are executed in order. Between each pair of stages, there is a latch, and each latch type is described by a separate class. The implemented stages include:

1. IF (Instruction Fetch) Stage: This stage has been implemented and is responsible for fetching instructions from memory. The instructions are then passed to the next stage through the IF-OF latch.
2. OF (Operand Fetch) Stage: This stage is responsible for decoding the instructions and preparing them for execution. The contents of the ID latch are determined by the specific instruction being processed.

3. EX (Execution) Stage: In this stage, arithmetic and logic operations are performed based on the decoded instructions. The contents of the EX latch depend on the operation being executed.

4. MA (Memory Access) Stage: This stage handles memory read

5. RW (Register Write) Stage: The final stage is responsible for writing the results of instructions back to registers. The contents of the WB latch depend on the type of instruction and the data to be written back.

The simulation continues until an “end” instruction passes through the WB stage, at which point the simulation is marked as complete using setSimulationComplete().

3. Test Case Performance

The following table summarises the performance of the simulator for each test case: The table provides a summary of the performance of the simulator for each test case, including the number of instructions and how frequently each test case has been executed for

Test Case	Instructions	Executed Instructions
Fibonacci	21	79
Descending	21	278
Even or Odd	9	7
Prime	16	30
Palindrome	16	50

4. Conclusion

In conclusion, the ToyRISC single cycle processor simulator has been successfully implemented according to the given specifications. The simulator can load programs, execute instructions through the five processor stages, and record relevant statistics.