VLSI Global Router

Congestion Visualizer

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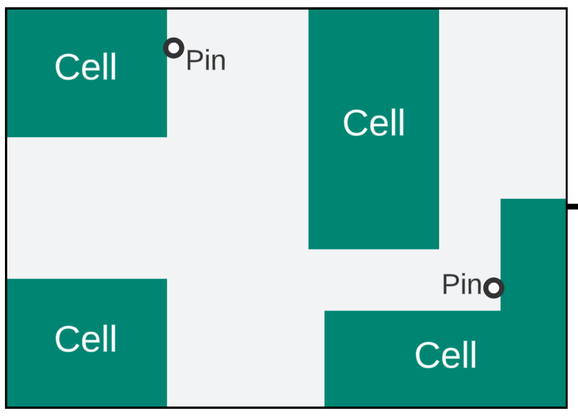
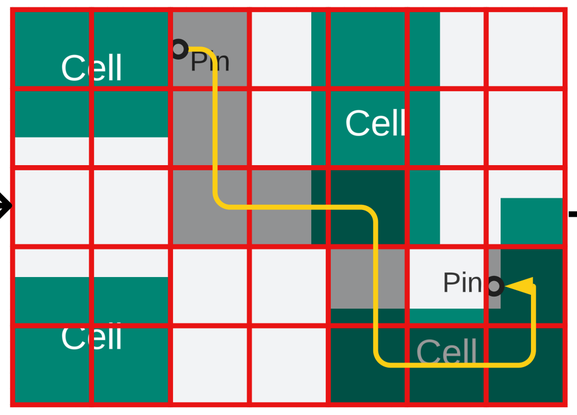
Introduction

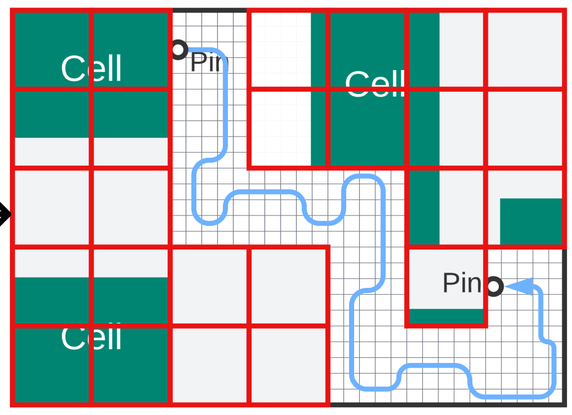
VLSI (Very Large Scale Integration) is the process of designing and fabricating integrated circuits that has millions of transistors on a chip. One of the steps in the design process is routing, which involves determining the optimal paths for the interconnects between various components on the chip. Global routing is a stage in the routing process that determines the long-distance connections between the different blocks of the chip.



Original Layout



Global Routing

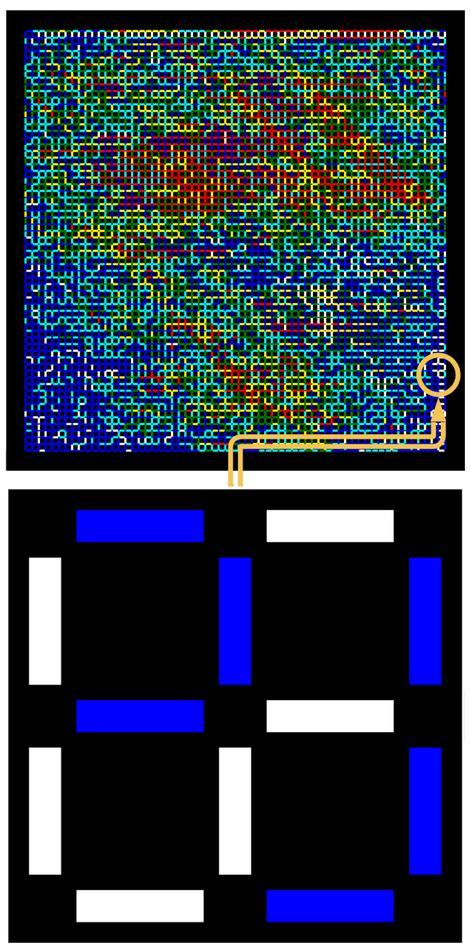


Detailed Routing

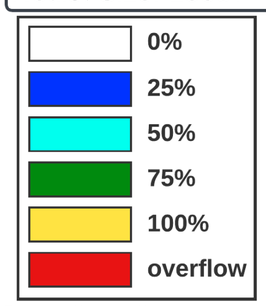
Objectives

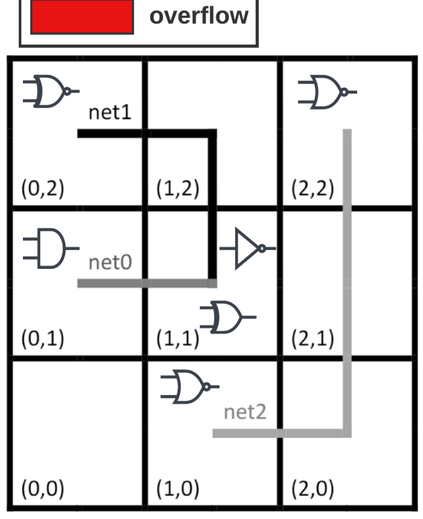
1. Minimum Overflow (demand-capacity)
2. Minimum Wirelength
3. Short execution time

Problem Statement

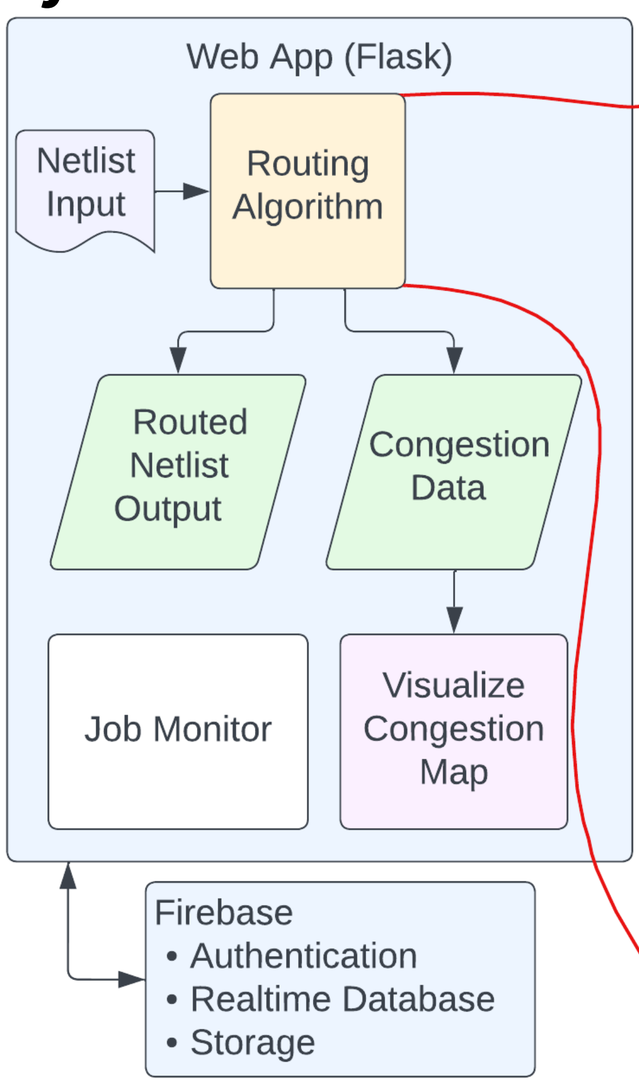


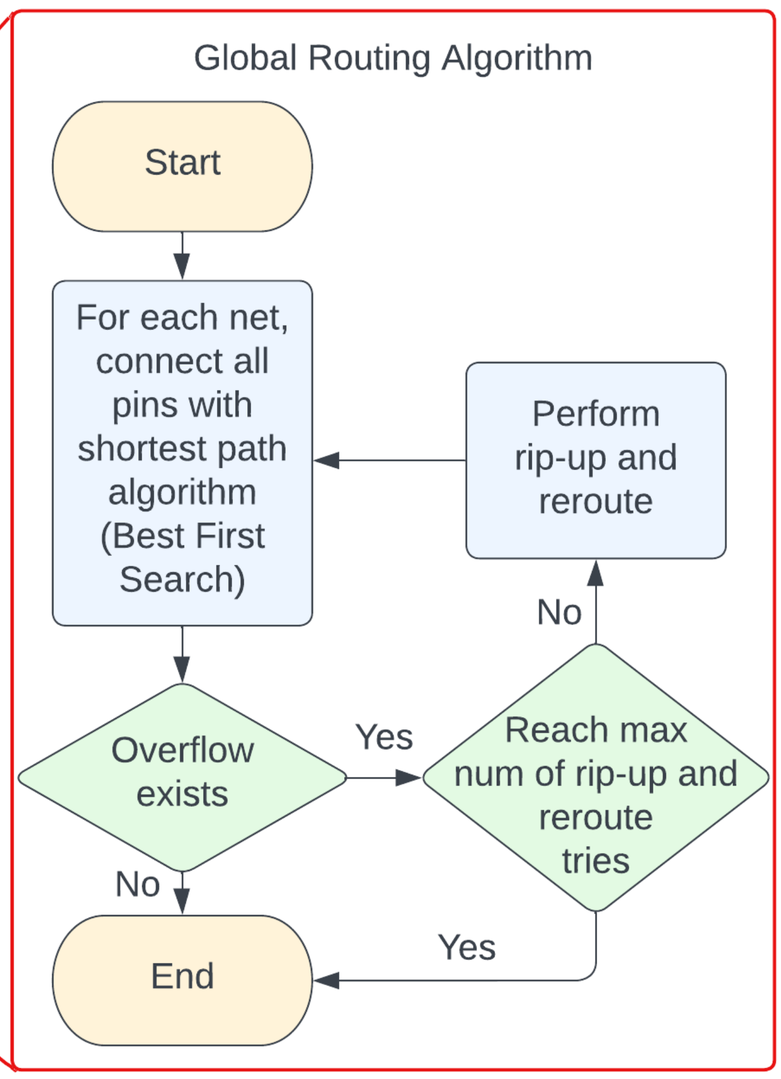
Name: IBM01
Vertical Capacity: 12
Horizontal Capacity: 14
Grid Size: 64 X 64
Netlist Size: 13357





System Architecture

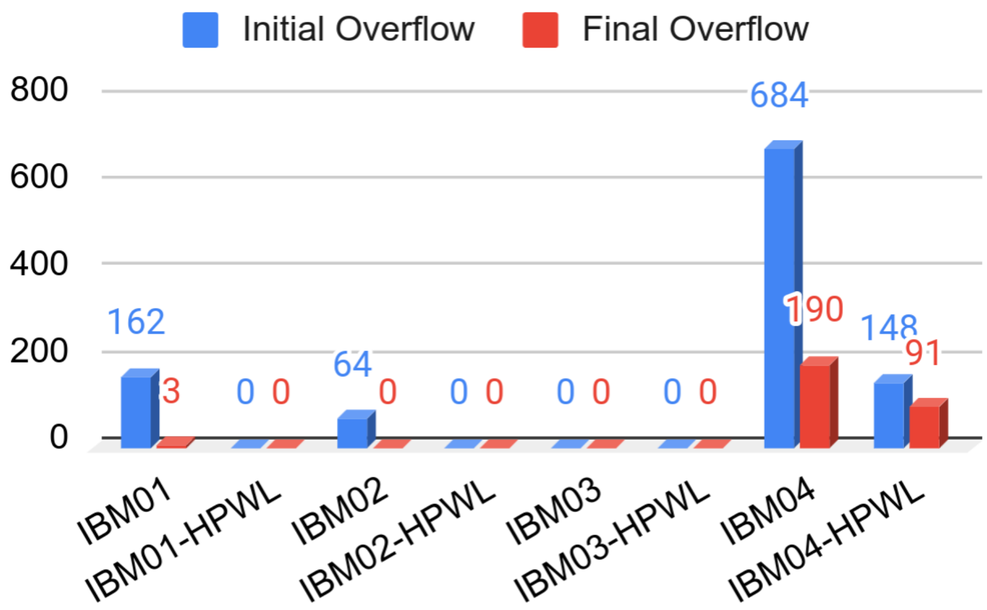




Conclusion and Results

Given that the nets are routed sequentially, it is better to route it in order of the net's HPWL (Half Perimeter Wire Length), allowing the router to perform routing on the nets with a smaller bounding box first.
Stochastic Property: Shuffle the netlist order
Deterministic Property: Sort it in ascending order of the net's HPWL
Parallelization: 5 Global Routers running in parallel during the initial stage

Overflow



Wirelength