[As per Choice I	•	stem (CBCS) scheme] c year 2018 - 2019)		
Subject Code	18CS33	IA Marks	40	
Number of Lecture Hours/Week	3:0:0	Exam Marks	60	
Total Number of Lecture Hours	50	Exam Hours	03	
	CREDITS -	03	•	
Module – 1				Teaching Hours
Photodiodes, Light Emitting Diodes and to base Bias, voltage divider bias Multivibrators using IC-555, Peak De Amplifier, Relaxation Oscillator, Curron Regulated Power Supply Parameters, converter. Text Book 1:Part A:Chapter 2(Section, 4.3, 4.4), Chapter 7 (section (7.2, 7.3. Chapter 9 RBT: L1, L2)	ns, Operational tector, Schmitt trent-to-Voltage an adjustable voltage ion 2.9,2.10,2.11)	Amplifier Application Cigger, Active Filters, Non d Voltage-to-Current Cone regulator, D to A and A. Chapter 4(Section 4.2)	Circuits: -Linear verter , A to D	8 Hours
Module – 2 Karnaugh maps: minimum forms of sw maps, four variable karnaugh maps, det prime implicants, Quine-McClusky Me implicant chart, petricks method, sir simplification using map-entered variable Text book 1:Part B: Chapter 5 (Sect RBT: L1, L2	ermination of min thod: determination inplification of in the	nimum expressions using e on of prime implicants, Th ncompletely specified fur	ssential e prime nctions,	8 Hours
Module – 3 Combinational circuit design and simul design, design of circuits with limited Hazards in combinational Logic, simula Multiplexers, Decoders and Program buffers, decoders and encoders, Programs, Programmable Array Logic. Text book 1:Part B: Chapter 8,Chap	I Gate Fan-in ,G ation and testing on mable Logic D grammable Logic	ate delays and Timing dia of logic circuits evices: Multiplexers, thre c devices, Programmable	agrams, ee state	8 Hours
Module – 4	ter > (Sections >)	1 10 310) 1121, 22		
Introduction to VHDL: VHDL descript multiplexers, VHDL Modules. Latches Edge-Triggered D Flip Flop 3,SR Flip additional inputs, Asynchronous Seque Text book 1:Part B: Chapter 10(Sect 11.9) RBT: L1, L2	s and Flip-Flops: o Flop, J K Flip l ntial Circuits	Set Reset Latch, Gated I Flop, T Flip Flop, Flip Flo	Latches, op with	8 Hours
Module – 5				
Registers and Counters: Registers and R shift registers, design of Binary counters SR and J K Flip Flops, sequential parity Text book 1:Part B: Chapter 12(Sect RBT: L1, L2	s, counters for oth y checker, state ta	er sequences, counter desig bles and graphs	gn using	8 Hours
Course outcomes: The students sho	auld be able to:			
Course outcomes. The students sho	outh of able to:			

- Design and analyze application of analog circuits using photo devices, timer IC, power supply and regulator IC and op-amp.
- Explain the basic principles of A/D and D/A conversion circuits and develop the same. Simplify digital circuits using Karnaugh Map, and Quine-McClusky Methods
- Explain Gates and flip flops and make us in designing different data processing circuits, registers and counters and compare the types.
- Develop simple HDL programs
- Question paper pattern:
- The question paper will have ten questions.
- Each full Question consisting of 20 marks
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module

TextBooks:

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning, 2019

Reference Books:

- 1. Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
- 2. Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.
- 3. M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
- 4. David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008

COURSE OBJECTIVES:

1	Explain the use of photoelectronics devices, 555 timer IC, Regulator ICs and uA741 opamp IC
2	Make use of simplifying techniques in the design of combinational circuits.
3	Illustrate combinational and sequential digital circuits
4	Demonstrate the use of flip flops and apply the same for registers
5	Design and test counters, Analog-to-Digital and Digital-to-Analog conversion

COURSE OUTCOMES (COs):

SL.	DESCRIPTION
NO	After Completing thus course, the students will be able to:
CO:1	Design and analyse application of analog circuits using photo devices, timer IC, power supply and regulator IC and op-amp.
CO:2	Simplify digital circuits using Karnaugh Map, and Quine-McCluskey Methods
CO:3	Designing different data processing circuits
CO:4	Develop simple HDL programs and Explain Gates and flip flops
CO:5	Explain and develop Registers & Counters

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MODULE 2

2.0: Introduction

Analog electronics is an electronics system where signal change continuously. **Analog signal** is a signal whose amplitude can take any value between given limits. A continuous signal. An **analog circuits** operates on continuous signals.

Digital electronics is a field of electronics involving the study of digital signals and the engineering of devices that use or produce them. **Digital signal** is a signal whose amplitude can have only given discrete values between defined limits. A signal that changes amplitude in discrete steps. A **digital circuits** operates on discrete signals.

Clock is a periodic, rectangular waveform used as a basic timing signal. **Duty cycle** for a periodic digital signal, the ratio of high level time to the period or the ratio of low level time to the period. A table that shows all of the input output possibilities of a logic circuit is called **truth table**.

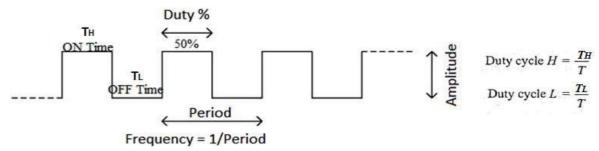


Fig: Clock Signal

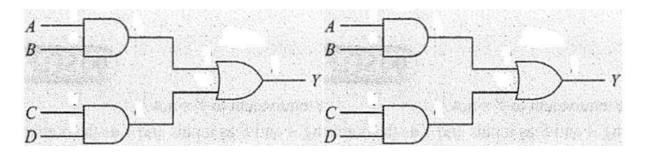
A **digital circuit** having one or more input signals but only one output signal is called a gate. **Logic circuit** is a digital circuit, a switching circuit, or any kind of two-state circuit that duplicates mental processes. The most **basic gates** are -the **NOT** gate (inverter), the **OR** gate and the **AND** gate.

NOT gate: A gate with only one input	Truth table	Logic diagram
and a complemented output. $F = \overline{A}$ or $F = A'$	A F 0 1 1 0	A — F
OR gate: A gate with two or more inputs. The output is high when any input is high.	AB C = A + B 0 0 0 0 1 1 1 0 1 1 1 1	$A \longrightarrow C = A + B$
AND gate: A gate with 2 or more inputs. The output is high only when all inputs are high.	AB C = A · B 0 0 0 0 1 0 1 0 0 1 1 1	$A \longrightarrow C = A \cdot B$

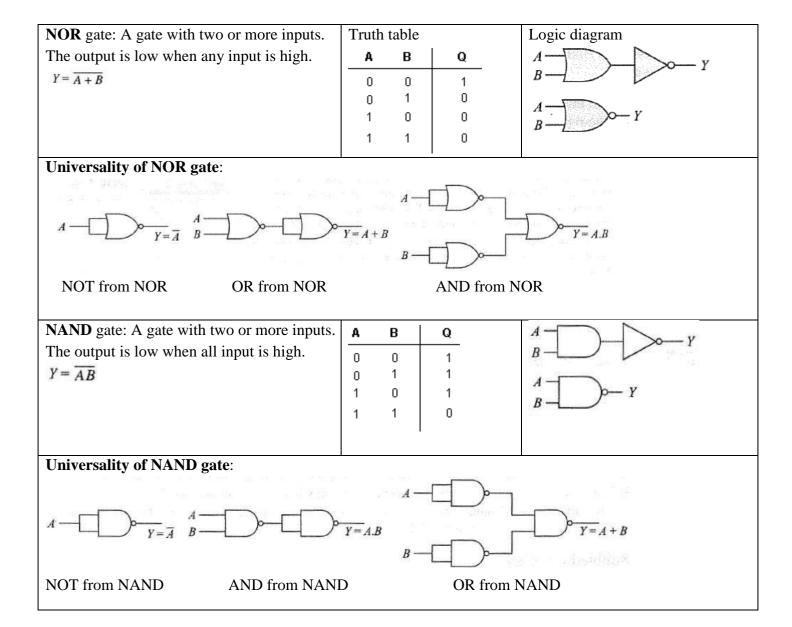
Realize following Boolean functions using basic gate.

$$i) Y=AB+CD$$

$$ii) Y = (A+B)(C+D)$$



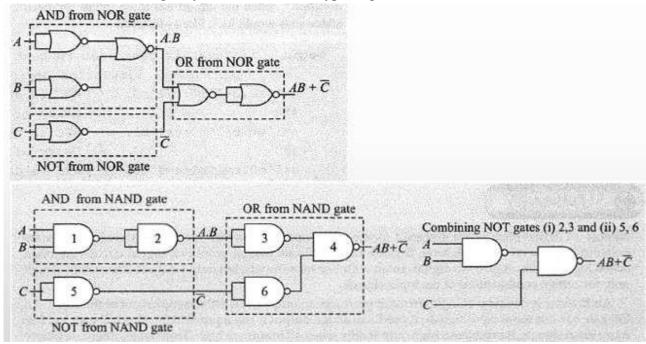
Any logic function/ logic circuit can be implemented using only one kind of gate then such gates are called **universal logic gates**. **NOR** gate and **NAND** gate are called universal logic gates.



Other important gates are XOR and XNOR gates.

Exclusive-OR gate: A gate with two or more inputs and output of is HIGH only when the number of HIGH inputs is odd.	X Y 0 0 0 1 1 0 1 1	X⊕Y 0 1 1 0	$X \oplus X \oplus Y$
Equivalence/exclusive-NOR gate: A gate with two or more inputs and output of is HIGH only when the number of HIGH inputs is even.	X Y 0 0 0 1 1 0 1 1	X ≡ Y 1 0 0 1	$X \longrightarrow Y \longrightarrow $

Realize Y = AB + C using only NOR and NAND type of gate.



Active-low refers to the concept in which a signal must be low to cause something to happen or to indicate that something has happened. **Assert** means to activate. If an input line has a bubble on it, you assert the input by making it low. If there is no bubble, you assert the input by making it high.

Laws of Boolean algebra

Operations with 0 and 1: 1. $X + 0 = X$ 2. $X + 1 = 1$	1D. $X \cdot 1 = X$ 2D. $X \cdot 0 = 0$
Idempotent laws: 3. $X + X = X$	3D. $X \cdot X = X$
Involution law: 4. $(X')' = X$	
Laws of complementarity: 5. $X + X' = 1$	5D. $X \cdot X' = 0$

Commutative laws: 6. $X + Y = Y + X$	6D. XY = YX
Associative laws: 7. $(X + Y) + Z = X + (Y + Z)$ = X + Y + Z	7D. $(XY)Z = X(YZ) = XYZ$
Distributive laws: 8. $X(Y + Z) = XY + XZ$	8D. $X + YZ = (X + Y)(X + Z)$
DeMorgan's laws: 9. $(X + Y)' = X'Y'$	9D. $(XY)' = X' + Y'$

Minimum Forms of Switching Functions

In a **positive logic** system, binary 0 stands for low voltage and binary 1 for high voltage. In a **negative logic** system, binary 0 stands for high voltage and binary 1 for low voltage. **Assert** means to activate. If an input line has a bubble on it, you assert the input by making it low. If there is no bubble, you assert the input by making it high. **Active-low** refers to the concept in which a signal must be low to cause something to happen or activate the circuit. **Active-high** refers to the concept in which a signal must be high to cause something to happen or to activate the circuit.

Combinational Circuits are circuits made up of different types of logic gates. The output of the combinational circuit depends on the values at the input at any given time. The circuits do not make use of any memory or storage device. A **literal** is a variable or its complement.

A **minterm** of n variables is a product of n literals in which each variable appears exactly once in either true or complemented form, but not both. A **maxterm** of n variables is a sum of n literals in which each variable appears exactly once in either true or complemented form, but not both.

Example: Minterms and Maxterms for Three Variables

Row No.	ABC	Minterms	Maxterms
0	000	$A'B'C' = m_0$	$A+B+C=M_0$
1	0 0 1	$A'B'C = m_1$	$A+B+C'=M_1$
2	0 1 0	$A'BC' = m_2$	$A + B' + C = M_2$
3	0 1 1	$A'BC = m_3$	$A + B' + C' = M_3$
4	1 0 0	$AB'C' = m_4$	$A'+B+C=M_4$
5	1 0 1	$AB'C = m_5$	$A' + B + C' = M_5$
6	1 1 0	$ABC' = m_6$	$A'+B'+C=M_6$
7	1 1 1	$ABC = m_7$	$A'+B'+C'=M_7$

Minterm expansion or a standard sum of products (SOP): A Boolean equation that is the logical sum of logical products. This type of equation applies to an AND-OR circuit.

Maxterm expansion or standard product of sums (POS): A Boolean equation that is the logical product of logical sums. This type of equation applies to an OR-AND circuit.

Steps to get SOP:

- 1) Locate each output 1 in truth table
- 2) Write the respective minterm

3) Apply OR operation to the minterms

Example:

A	В	C	Y			
0	0	0	0			
0	0	1	1	A.B.C	SOP:	
0	1	0	1	A.B.C	SOF.	
0	1	1	1	A.B.C	$\overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + \overline{A}.B.C + A.B.\overline{C}$	Σm(1, 2, 3, 6)
1	0	0	0		Albie + Albie + Albie + Albie	700,70
1	0	1	0			
1	1	0	1	A.B.C		
1	1	1	0			

Steps to get POS:

- 1) Locate each output 0 in truth table
- 2) Write the respective maxterm
- 3) Apply AND operation to the maxterms

Example:

Α	B	C	Y			
0	0	0	0	A+B+C		
0	0	1	1	The state of the s		
0	1	0	1			
0	1	1	1	normal au		
1	0	0	0	A+B+C		
1	0	1	Ŏ	A+B+C	POS:	
1	1	0	1	A+B+C	$(A+B+C)$. $(\overline{A}+B+C)$. $(\overline{A}+B+\overline{C})$. $(\overline{A}+\overline{B}+\overline{C})$	$=\Pi M(0, 4, 5, 7)$
1	1	1	0	A+B+C		

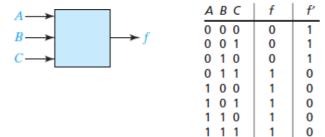
Conversion between SOP and POS:

- 1) Identifying complementary locations,
- 2) Changing mintenn to maxtenn or reverse, and finally
- 3) Changing summation by product or reverse

Example:
$$Y = F(A, B, C) = \prod M(O, 3, 6)$$

= $\sum m(l, 2, 4, 5, 7)$
Example: $Y = F(A, B, C) = \sum m(3, 5, 6, 7)$
= $\prod M(O, 1, 2, 4)$

Example: Combinational Circuit with Truth Table is given write SOP and POS expressions.



```
Minterms: A'BC, AB'C', AB' C, ABC', ABC

Maxterms: (A + B + C), (A + B + C'), (A + B' + C)

SOP:

f = A'BC + AB'C' + AB' C + ABC' + ABC

f = (A + B + C)(A + B + C')(A + B' + C)

f(A, B, C) = m_3 + m_4 + m_5 + m_6 + m_7

f(A, B, C) = M0 M1 M2

f(A, B, C) = M0 M1 M2
```

An **Incompletely specified function** is a Boolean function that only define output values for a subset of its inputs - i.e. a Boolean function who's output is a don't care for at least one of its input combinations. The **X**'s in the truth table indicate that we don't care whether the value of 0 or 1 is assigned to F.

Example: Truth Table with Don't-Cares

Α	В	C	F
0	0	0	1
0	0	1	Х
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	Х
1	1	1	1

In SOP we use m to denote the required minterms and d to denote the don't-care minterms.

$$F(A,B,C) = \Sigma m(0, 3, 7) + \Sigma d(1, 6)$$

In POS we use M to denote the required maxterms and D to denote the don't-care maxterms.

$$F(A,B,C) = \Pi M(2, 4, 5) \cdot \Pi D(1, 6)$$

Write minterm and maxterm expansions for the following truth table.

```
A B C D Z

0 0 0 0 1

0 0 0 1 0

0 0 1 0 0

0 0 1 1 1

0 1 0 0 0

0 1 1 0 1

0 1 1 0 1

0 1 1 1 0

1 0 0 0 0

1 0 0 1 1

1 0 1 0 X

1 0 1 1 X Answer:

1 1 0 1 X Z = \Sigma m(0, 3, 6, 9) + \Sigma d(10, 11, 12, 13, 14, 15)

1 1 1 1 X Z = \Pi m(1, 2, 4, 5, 7, 8) + \Sigma D(10, 11, 12, 13, 14, 15)
```

Find the minterm expansion of f(a, b, c, d) = a'(b' + d) + acd'.

```
f = a'b' + a'd + acd'
= a'b'(c + c')(d + d') + a'd(b + b')(c + c') + acd'(b + b')

= a'b'c'd' + a'b'c'd + a'b'cd' + a'b'cd + a'b'c'd + a'b'cd

+ a'bc'd + a'bcd + abcd' + ab'cd'
```

Duplicate terms have been crossed out, because X + X = X. This expression can then be converted to decimal notation:

The maxterm expansion for f can then be obtained by listing the decimal integers (in the range 0 to 15) which do not correspond to minterms of f:

$$f = \Pi M(4, 6, 8, 9, 11, 12, 13, 15)$$

Show that a'c + b'c' + ab = a'b' + bc + ac'.

We will find the minterm expansion of each side by supplying the missing variables. For the left side,

$$a'c(b + b') + b'c'(a + a') + ab(c + c')$$

= $a'bc + a'b'c + ab'c' + a'b'c' + abc + abc'$
= $m_3 + m_1 + m_4 + m_0 + m_7 + m_6$

For the right side,

$$a'b'(c + c') + bc(a + a') + ac'(b + b')$$

= $a'b'c + a'b'c + abc + a'bc + abc' + ab'c'$
= $m_1 + m_0 + m_7 + m_3 + m_6 + m_4$

Because the two minterm expansions are the same, the equation is valid.

2.1 Minimum Forms of Switching Functions

A minimum sum of products expression for a function is defined as a sum of product terms which

- (i) has a minimum number of terms and
- (ii) of all those expressions which have the same minimum number of terms, has a minimum number of literals.

The minimum sum of products corresponds directly to a minimum two-level gate circuit which

- (i) has a minimum number of gates and
- (ii) a minimum number of gate inputs.

The minimum sum of products is not necessarily unique; that is, a given function may have two different minimum sum of products forms, each with the same number of terms and the same number of literals. Given a minterm expansion, the minimum sum-of products form can often be obtained by the following procedure:

- (i) Combine terms by using \square '+ \square Y =(\square '+ \square)= \square . Do this repeatedly to eliminate as many literals as possible. A given term may be used more than once because X+X=X.
- (ii) Eliminate redundant terms by using the theorems of Boolean Algebra.

Example: Find a minimum sum-of-products expression for

F(a, b, c) =
$$\Sigma$$
 m (0, 1, 2, 5, 6, 7)
F = a'b'c' + a'b'c + a'bc' + ab'c + abc' + abc
F = a'b'(c'+c) + bc' (a'+a) + ac(b+b')
F = a'b' + bc' + ac
Or
F = a'b'c' + a'b'c + a'bc' + ab'c + abc' + abc
F = a'b'c' + a'bc' + a'b'c + ab'c + abc' + abc
F = a'c' + b'c + ab

A minimum product of sums expression for a function is defined as a product of sum terms which

- (i) has a minimum number of terms, and
- (ii) of all those expressions which have the same number of terms, has a minimum number of literals.

Unlike the maxterm expansion, the minimum product of sums form of a function is not necessarily unique. Given a maxterm expansion, the minimum product of sums can often be obtained by a procedure similar to that used in the minimum sum of products case, except that the theorem $(\Box + \Box ')(\Box + \Box) = \Box$ is used to combine terms.

Example:
$$F(a, b, c,d) = \Pi M (5, 7, 6, 14, 2, 10)$$

$$F = \{a+b'+c+d'\}(a+b'+c'+d')(a+b'+c'+d)(a'+b'+c'+d)(a'+b+c'+d)(a'+b+c'+d)$$

$$F = (a+b'+d')(b'+c'+d)(b+c'+d)$$

$$F = (a+b'+d')(c'+d)$$

Simplification of Boolean function reduces the gate count required to implement the circuit, the circuit works faster and circuit require less power consumption.

The various Boolean expression simplification techniques are

- 1) Algebraic techniques
- 2) Karnaugh Map/K-Map Method
- 3) Quine McCluskey Method
- 4) Entered Variable Map/ MEV/EMV Method

Switching/Boolean functions can generally be simplified by using the algebraic techniques. The disadvantages of algebraic procedure usage are

- (i) The procedures are difficult to apply in a systematic way,
- (ii) It is difficult to tell when we have arrived at a minimum solution.

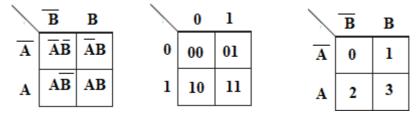
Karnaugh map/K map is a method simplifying and manipulating switching functions. K map method is faster and easier to apply than other simplification methods.

2.2 Two and Three Variable Karnaugh Maps

Karnaugh map of a function specifies the value of the function for every combination of values of the independent variables.

Two Variable K-Map

The number of cells in 2 variable K-map is four (2^2) , since the number of variables is two. The following figure shows 2 variable K-map and location of minterms on a 2 variable K-map.



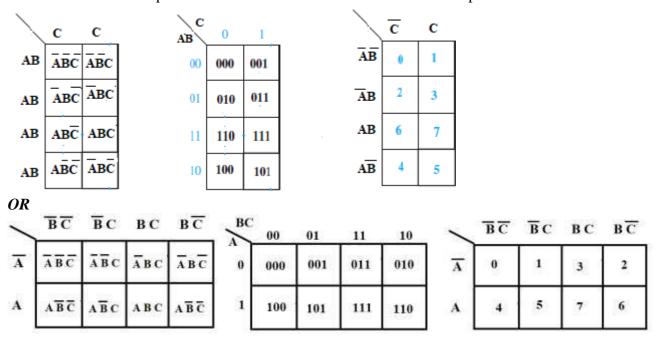
Example: Convert following truth table into K map.

$$Y = F(A, B) = \Sigma m (2, 3)$$

A size at	B	$m{y}_{ij}$		В	В
0	0	0	_	_	_
0	1	0	A	0	0
1 500	0	-1		1	1.
1	1	1	A	1 2	1 3

Three Variable K-Map

The number of cells in 3 variable K-map is eight (2³), since the number of variables is 3. The following figure shows 3 variable K-map and location of minterms on a 3 variable K-map.



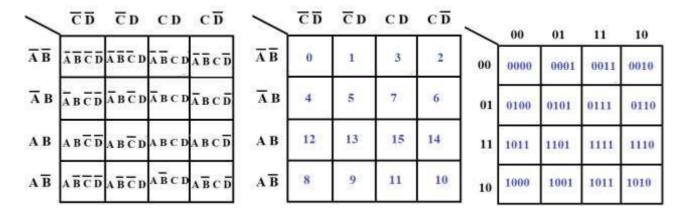
Example: Convert following truth table into K map.

$$Y = F(A, B, C) = \Sigma m (2,6,7)$$

A	В	C	Y						
0	0	0	0		_	$\overline{\mathbf{B}}\overline{\mathbf{C}}$	$\overline{\mathbf{B}}\mathbf{C}$	BC	$B\overline{C}$
0	0	1	. 0			20013007	10/28/10/23	110000000	
0	1	0	1	6 L 200	_			0	122
0	1	1	0		A	0 0	υ,	0	1,
1	. 0	0	0				-	-	-
1	0	1	0	250	Δ		0	1	1
1	1	0	1		A	0 4	5	7	6
1	1	1	1				-		

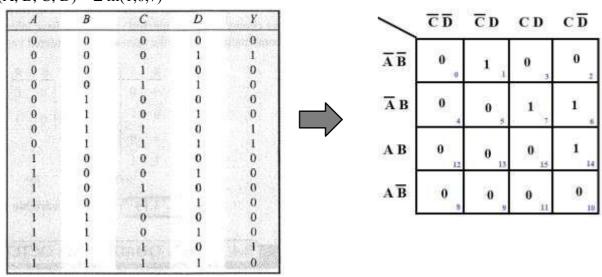
2.3 Four-Variable Karnaugh Maps

The number of cells in 4 variable K-map is sixteen (2⁴), since the number of variables is 4. The following figure shows 4 variable K-map and location of minterms on a 4 variable K-map.



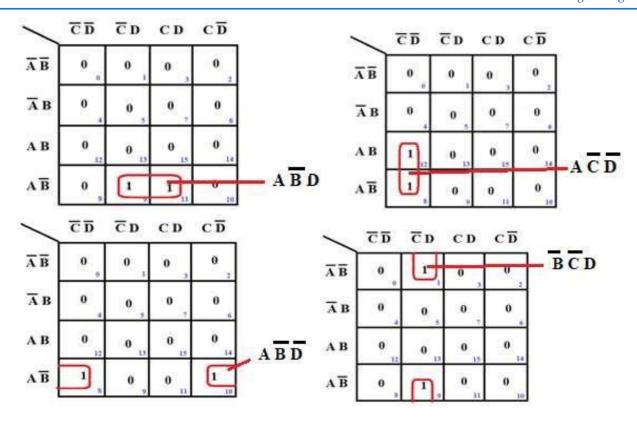
Example: Convert following truth table into K map.

$$Y = F(A, B, C, D) = \sum m(1,6,7)$$

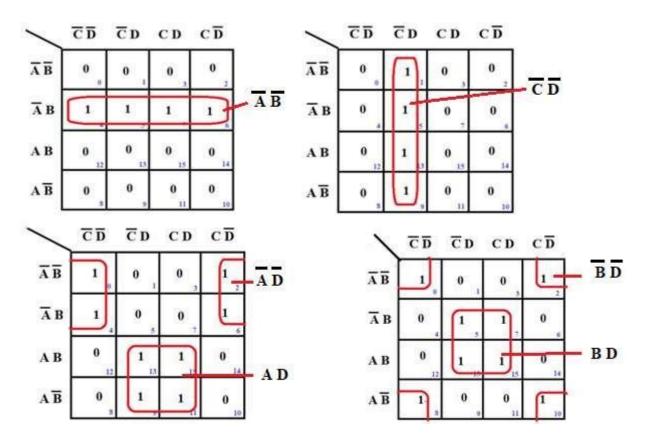


Pairs, Quads, and Octets

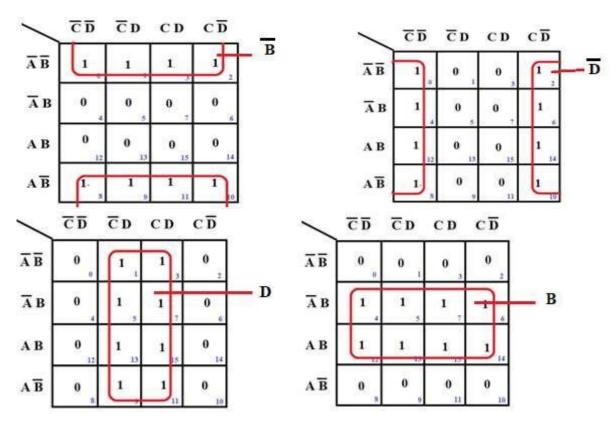
Two adjacent 1s in the K-map is called a *pair* and it eliminate the *variable* that changes form. Sample of pair



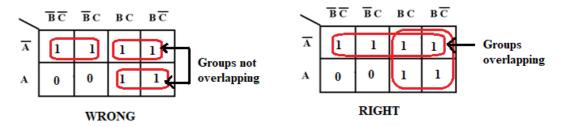
A *quad* is a group of four ls that are horizontally or vertically adjacent and a quad eliminates two variables and their complements.



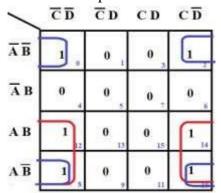
An *octet* is a group of 8 ls that are horizontally or vertically adjacent and an octet eliminates three variables and their complements.



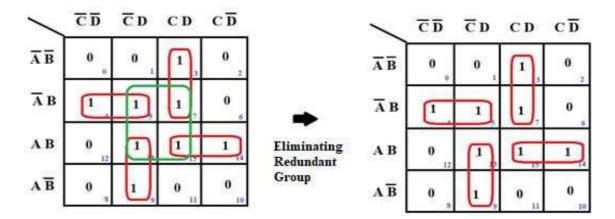
Overlapping of groups: We are allowed to use the same 1 more than once.



Rolling of Map: Groups may wrap around the table. The leftmost cell in a row may be grouped with the rightmost cell and the top cell in a column may be grouped with the bottom cell. Roll and overlap to get largest group.



Eliminating redundant group: A groups of 1s or 0s whose all members are overlapped by other groups is called redundant group. After encircling all possible group, eliminate any redundant group if any. We don't consider this group while writing the simplified equations from the K-map.



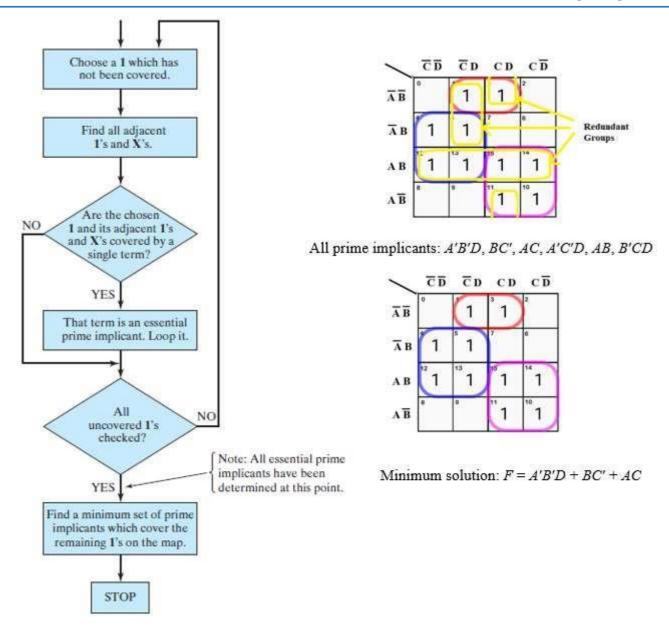
2.4 <u>Determination of Minimum Expressions using Essential Prime Implicants</u>

Any single 1 or any group of 1's which can be combined together on a map of the function F represents a product term which is called an implicant of F. Several implicants of F may be possible. A product term implicant is called a prime implicant if it cannot be combined with another term to eliminate a variable.

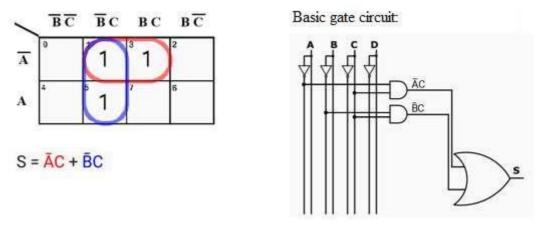
The following procedure can then be used to obtain a minimum sum of products from a Karnaugh map:

- 1) Choose a minterm (a 1) which has not yet been covered.
- 2) Find all 1's and X's adjacent to that minterm. (Check the n adjacent squares on an n-variable map.)
- 3) If a single term covers the minterm and all of the adjacent 1's and X's, then that term is an essential prime implicant, so select that term. (don't-care terms are treated like 1's in steps 2 and 3 but not in step 1.)
- 4) Repeat steps 1, 2, and 3 until all essential prime implicants have been chosen.
- 5) Find a minimum set of prime implicants which cover the remaining 1's on the map. (If there is more than one such set, choose a set with a minimum number of literals.)

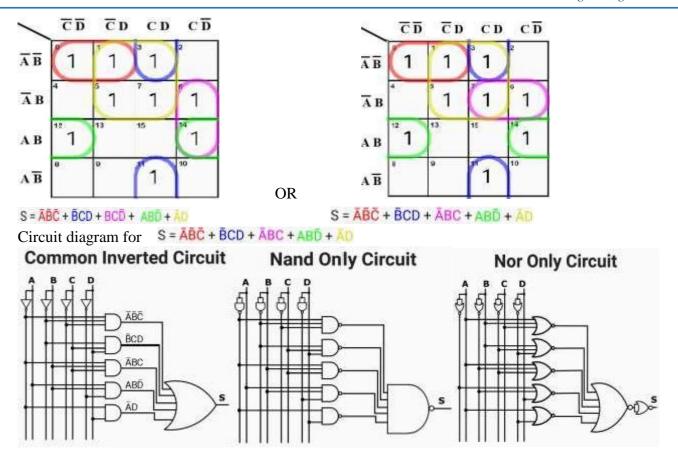
The following figure shows the flowchart for determining a minimum sum of products using a Karnaugh map with an example.



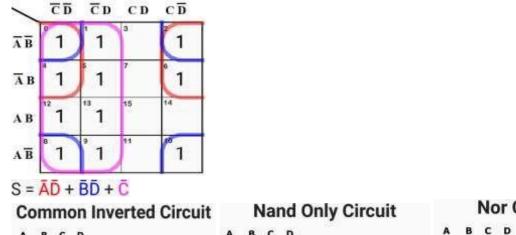
Solve $S(A,B,C)=\Sigma m(1,3,5)$ using K map and implement using basic gates.

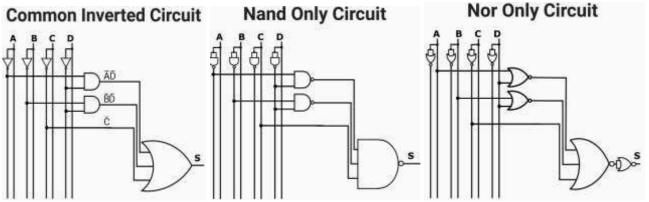


Solve S= $F(A,B,C)=\Sigma m(0, 1, 3, 5, 6, 7, 11, 12, 14)$ using Kmap and implement uisng basic, nand only and norly gates.

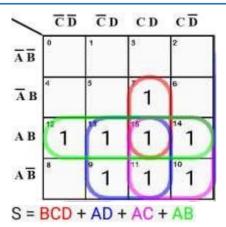


Solve S=F(A,B,C,D)= Σ m(0,1,2,4,5,6,8,9,10,12,13) using Kmap and implement uisng basic, nand only and norly gates.

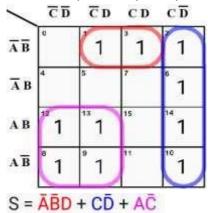




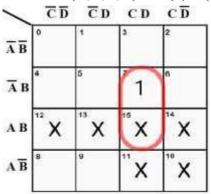
Solve $S = F(A,B,C,D) = \sum m(7,9,10,11,12,13,14,15)$ using K map to get minimum SOP expression.



Solve $S=F(A,B,C,D)=\Sigma m(1,2,3,6,8,9,10,12,13,14)$ using K map to get minimum SOP expression.



Solve $S=F(A,B,C,D)=\Sigma m(7)+d(10,11,12,13,14,15)$ using K map to get minimum SOP expression.



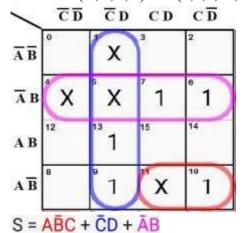
S = BCD

Solve $S = F(A,B,C,D) = \sum m(2,3,5,7,10,12) + d(11,15)$ using K map to get minimum SOP expression.

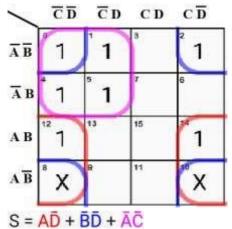
$\overline{C}\overline{D}$	C D	CD	CD
0	3	1	1
4	1	1	0
(1)	13	15 X	14
8	9	X	10 1
	1	1 1 13	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

$S = AB\overline{C}\overline{D} + \overline{A}BD + \overline{B}C$

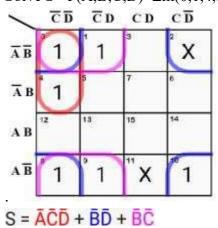
Solve $S=F(A,B,C,D)=\Sigma m(6,7,9,10,13)+d(1,4,5,11)$ using K map to get minimum SOP expression.

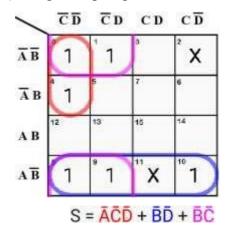


Solve $S = F(A,B,C,D) = \sum m(0,1,2,4,5,12,14) + d(8,10)$ using K map to get minimum SOP expression.

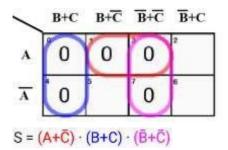


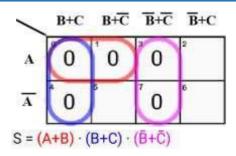
Solve $S = F(A,B,C,D) = \sum m(0,1,4,8,9,10) + d(2,11)$ using K map to get minimum SOP expression.



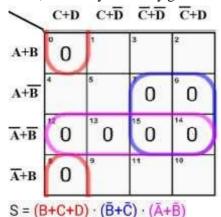


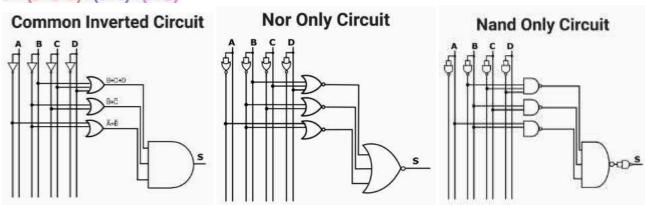
Solve $S=F(A,B,C,D)=\Pi M(0,1,3,4,7)$ using K map to get minimum POS expression.



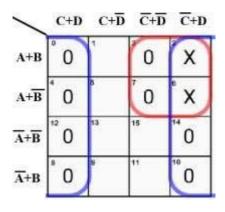


Solve $S=F(A,B,C,D)=\Pi M(0,6,7,8,12,13,14,15)$ using K map to get minimum POS expression and implement uisng basic, nand only and norly gates.

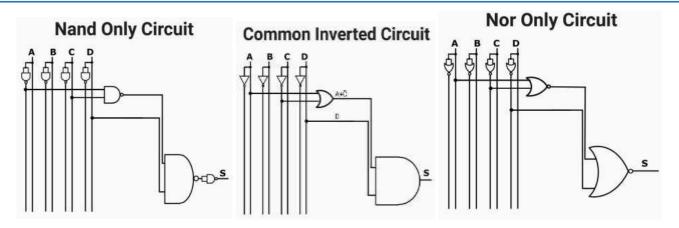




Solve $F(A,B,C,D)=\Pi M(0,3,4,7,810,12,14).\Pi D(2,6)$ using K map to get minimum POS expression and implement uisng basic, nand only and norly gates.

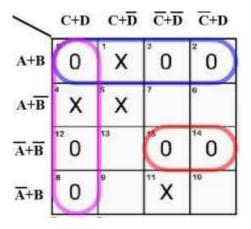


$$S = (A + \bar{C}) \cdot (D)$$



Solve S=F(A,B,C,D)= Σ m(6,7,9,10,13)+ Σ d(1,4,5,11) using K map to get minimum POS expression.

 $S = F(A,B,C,D) = \Pi M(0,2,3,8,12,14,15).\Pi D(1,4,5,11)$



$$S = (\overline{A} + \overline{B} + \overline{C}) \cdot (A + B) \cdot (C + D)$$

Limitations of K map:

Complexity of **K-map** simplification process increases with the increase in the number of variables K map is manual technique and simplification process heavily depends on the human ability.

2.5 **Ouine-McCluskey Method**

The Quine-McCluskey method provides a systematic simplification procedure which can be readily programmed for a digital computer. The Quine-McCluskey method reduces the minterm expansion (standard sum-of-products form) of a function to obtain a minimum sum of products.

Quine-McClusky method involves preparation of two tables; one determines prime implicants and the other selects essential prime implicants to get minimal expression. Prime implicants are expressions with least number of literals that represents all the terms given in a truth table. Prime implicants are examined to get essential prime implicants for a particular expression that avoids any type of duplication.

2.6 Determination of Prime Implicants

In order to apply the Quine-McCluskey method to determine a minimum sum-of-products expression for a function, the function must be given as a sum of minterms.

Step 1 – Arrange the given min terms in an ascending order and make the groups based on the number of ones present in their binary representations. So, there will be at most 'n+1' groups if there are 'n' Boolean variables in a Boolean function or 'n' bits in the binary equivalent of min terms.

Step 2 – Compare the min terms present in successive groups. If there is a change in only one-bit position, then take the pair of those two min terms. Place this symbol '_' in the differed bit position and keep the remaining bits as it is.

```
AB'CD' + AB'CD = AB'C
1 0 1 0 + 1 0 1 1 = 1 0 1 - \text{(the dash indicates a missing variable)}
X Y X Y' X
A'BC'D + A'BCD' \text{ (will not combine)}
0 1 0 1 + 0 1 1 0 \text{ (will not combine)}
```

Step 3 – Repeat step2 with newly formed terms till we get all prime implicants.

Given a function F of n variables, a product term P is an implicant of F if for every combination of values of the n variables for which P = 1, F is also equal to 1.

A prime implicant of a function F is a product term implicant which is no longer an implicant if any literal is deleted from it.

2.7 The Prime Implicant Chart:

The second part of the Quine-McCluskey method employs a prime implicant chart to select a minimum set of prime implicants.

Step 4 – Formulate the prime implicant table/chart. It consists of set of rows and columns. Prime implicants can be placed in row wise and min terms can be placed in column wise. Place '1' in the cells corresponding to the min terms that are covered in each prime implicant.

Step 5 – Find the essential prime implicants by observing each column. If the min term is covered only by one prime implicant, then it is essential prime implicant. Those essential prime implicants will be part of the simplified Boolean function.

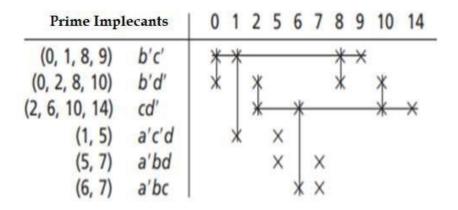
Step 6 – Reduce the prime implicant table by removing the row of each essential prime implicant and the columns corresponding to the min terms that are covered in that essential prime implicant. Repeat step 5 for Reduced prime implicant table. Stop this process when all min terms of given Boolean function are over.

Find the minimum SOP for the function $f(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$ using Quine McCluskey method.

Determination of prime implicants:

Sta	ige 1	Stag	ge 2	Stage	3
Minterms	abcd	Minterms	abcd	Minterms	a bcd
0	0000 ✓	0, 1	000- ✓	0, 1, 8, 9	-00-
1	0001 🗸	0, 2	00-0 🗸	0, 2, 8, 10	-0-0
2	0010 🗸	0, 8	-000 ✓	0, 8, 1, 9	-00-
8	1000 🗸	1, 5	0-01	0, 8, 2,10	0-0
5	0101 🗸	1, 9	-001 ✓	2, 6, 10, 14	10
6	0110 🗸	2, 6	0-10 🗸	2, 10, 6, 14	10
9	1001 🗸	2, 10	-010 ✓	- 5	
10	1010 🗸	8, 9	100- ✓		
7	0111 🗸	8, 10	10-0 ✓		
14	1110 🗸	5, 7	01-1		
		6, 7	011-		
		6, 14	-110 ✓		
		10, 14	1-10 🗸		

Prime implicant chart:



$$f = b'c' + cd' + a'bd$$

Determine the essential prime implicants using QM method for the function $f(A, B, C, D) = \sum M(0,1,2,3,10,12,11,13,14,15)$

Determination of prime implicants:

Sta	ge 1	2	Stage 2		Stage 3
ABCD	minterms	ABCD	minterms	ABCD	minterms
0000	(0)√	000-	(0,1)√	00	(0,1,2,3)
		0 0 - 0	(0,2)√	0 0	(0,2,1,3)
0001	(1)√				
0010	(2)√	00-1	(1,3)√	-01-	(2,10,3,11)
	·····	001-	(2,3)√	1-1-	(10,11,14,15)
0011	(3)√	-010	(2,10)√	1-1-	(10,14,11,15)
1010	(10)√	-011	(3,11)√	11	(12,13,14,15)
1100	(12)√	101-	(10,11)√	11	(12,14,13,15)
		1 - 1 0	(10,14)√		
1011	and	110-	(12,13)	1	
1011	(11)V	11-0	(12,14)√		
1101	(13)√		(11.15)		90000 TRO (T)
1110	(14)√	1 - 1 1	(11,15)√		
1111	(15)√	11-1 111-	$(13,15)$ $\sqrt{(14,15)}$ $\sqrt{(14,15)}$	100	

Prime implicant charts:

	0	1	2	3	10	11	12	13	14	15
A'B' (0,1,2,3)	٧	1	1	1	200	-		-		
B'C (2,3,10,11)			\checkmark	V	V	V		25		
AC (10,11,14,15)					V	V	Man.		V	V
AB (12,13,14,15)							V	V	1	V

$$Y = A'B' + B'C + AB$$
 or $Y = A'B' + AC + AB$

Find the minimum SOP for the function $f(A, B, C) = \sum m(2, 6, 7)$ using Quine McCluskey method.

Determination of prime implicants:

Sta	ige l	<u>St</u>	age 2
ABC	minterms	ABC	minterms
010	(2)√	-10	(2,6)
110	(6)√	11-	(6,7)
111	(7)√		

Prime implicant charts:

Prime Implicants	2	6	7
BC' (2,6)	V	V	
AB (6,7)		₩	1

$$Y = AB + BC'$$

2.8 Petrick's Method

Petrick's method is a technique for determining all minimum sum-of-products solutions from a prime implicant chart. The example discussed above has two minimum solutions. As the number of variables increases, the number of prime implicants and the complexity of the prime implicant chart may increase significantly. In such cases, a large amount of trial and error may be required to find the minimum solution(s).

Petrick's method is a more systematic way of finding all minimum solutions from a prime implicant chart than the method used previously. Before applying Petrick's method, all essential prime implicants and the minterms they cover should be removed from the chart.

Steps in Petrick's method:

- 1. Reduce the prime implicant chart by eliminating the essential prime implicant rows and the corresponding columns.
- **2.** Label the rows of the reduced prime implicant chart P_1 , P_2 , P_3 , etc.
- **3.** Form a logic function P which is true when all columns are covered. P consists of a product of sum terms, each sum term having the form $(P_{i0} + P_{i1} + \cdot \cdot \cdot)$, where P_{i0} , P_{i1} . . . represent the rows which cover column i.
- **4.** Reduce P to a minimum sum of products by multiplying out and applying X + XY = X.
- **5.** Each term in the result represents a solution, that is, a set of rows which covers all of the minterms in the table. To determine the minimum solutions, find those terms which contain a minimum number of variables. Each of these terms represents a solution with a minimum number of prime implicants.

6. For each of the terms found in step 5, count the number of literals in each prime implicant and find the total number of literals. Choose the term or terms which correspond to the minimum total number of literals, and write out the corresponding sums of prime implicants.

Find the minimum SOP form for the function $f(a,b,c)=\sum m(0,1,2,5,6,7)$ using pettricks method.

Determination of prime implicants:

S	tage 1		Stage 2
minterm	s abc		minterms abc
0	000	1	0, 1 00-
1	001	1	0,2 0-0
2	010	1	1,5 -01
5	101	1	2,6 -10
6	110	1	5,7 1-1
7	111	1	6,7 11-

Prime implicant charts:

	Prime In	nlicants	0	1	2	5	6	7
$\overline{P_1}$	(0, 1)	a'b'	X	×				
P_2	(0, 2)	a'c'	X		X			
P_3	(1, 5)	b'c		X		×		
P_4	(26)	bc			X		×	
P_5	(5, 7)	ac				X		X
P_6	(6, 7)	ab					×	X

$$\begin{split} P &= (P_1 + P_2)(P_1 + P_3)(P_2 + P_4)(P_3 + P_5)(P_4 + P_6)(P_5 + P_6) = 1 \\ \text{using } (X + Y)(X + Z) &= X + YZ \text{ and distributive law:} \\ P &= (P_1 + P_2P_3)(P_4 + P_2P_6)(P_5 + P_3P_6) \\ &= (P_1P_4 + P_1P_2P_6 + P_2P_3P_4 + P_2P_3P_6)(P_5 + P_3P_6) \\ &= P_1P_4P_5 + P_1P_2P_5P_6 + P_2P_3P_4P_5 + P_2P_3P_5P_6 + P_1P_3P_4P_6 + P_1P_2P_3P_6 + P_2P_3P_4P_6 + P_2P_3P_6 \\ \text{use } X + XY &= X \text{ to eliminate redundant terms from } P \\ P &= P_1P_4P_5 + P_1P_2P_5P_6 + P_2P_3P_4P_5 + P_1P_3P_4P_6 + P_2P_3P_6 \end{split}$$

The two solutions with the minimum number of prime implicants are obtained by choosing rows P_1 , P_4 , and P_5 or rows P_2 , P_3 , and P_6 .

$$F = a'b' + bc' + ac$$

OR

F = a'c' + b'c + ab

2.9 Simplification of Incompletely Specified Functions:

Given an incompletely specified function, the proper assignment of values to the don't-care terms is necessary in order to obtain a minimum form for the function. Modified Quine-McCluskey method is used to obtain a minimum solution when don't-care terms are present. In modified Quine-McCluskey method the don't-care terms are treated like required minterms when finding the prime implicants and don't-care columns are omitted when forming the prime implicant chart. If extra prime implicants are generated because of the don't-cares, the extra prime implicants are eliminated in the prime implicant chart.

Find the minimum SOP for the function $F(A, B, C, D) = \Sigma m(2, 3, 7, 9, 11, 13) + \Sigma d(1, 10, 15)$ using Quine McCluskey method.

Determination of prime implicants:

2	Stage 1		Sta	age 2		Stage 3	
mintern	ns ABCD		minterms	ABCD		minterms	ABCD
1	0001	1	(1,3)	00-1	1	(1, 3, 9, 11)	-0-1
2	0010	1	(1,9)	-001	1	(2, 3, 10, 11)	-01-
3	0011	1	(2,3)	001-	1	(3, 7, 11, 15)	11
9	1001	1	(2, 10)	-010	1	(9, 11, 13, 15)	11
10	1010	1	(3,7)	0-11	1		
7	0111	1	(3, 11)	-011	1		
11	1011	1	(9, 11)	10-1	1		
13	1101	1	(9, 13)	1-01	1		
5	1111	1	(10, 11)	101-	1		
			(7, 15)	-111	1		
			(11, 15)	1-11	1		
			(13, 15)	11-1	1		
0			(15, 15)	11-1	~		

Prime implicant chart:

(The don't-care columns are omitted when forming the prime implicant chart)

Prime Implicants	2	3	7	9 11	13
(1, 3, 9, 11) (2, 3, 10, 11) (3, 7, 11, 15) (9, 11, 13, 15)	x	X X X	х	X X X X X X	X

$$F = B'C + CD + AD$$

2.10 Simplification Using Map Entered Variables:

A technique called Map Entered Variable (MEV) or Entered Variable Map (EVM) is used to increase the effective size of k-map. It allows a smaller map to handle large number of variables. This is done by writing output in terms of input. It allows a smaller map to handle large number of variables. This is done by writing output in terms of input.

Rules for entering values in a Map Entered Variable K map are:

Rule No.	MEV f	Map Entry	Comments
1	0 0	()	If function equals 0 for both values of MEV, enter 0 in
1	1 0		appropriate cell of MEV Map.
2	0 1	1	If function equals 1 for both values of MEV, enter 1.

	1 1	_	
3	0 0 1 1	MEV	If function equals MEV, enter MEV
4	0 1 1 0		If the function is compliment of MEV, enter NEV
5	0 X 1 X	X	If function equals X, enter X
6	0 0 1 X	0	f=0 for MEV=0 and f=X for MEV=1,enter 0
7	0 X 1 0	0	f=X for MEV=0 and f=0 for MEV=1,enter 0
8	0 1 1 X	1	f=1 for MEV=0 and f=X for MEV=1,enter 1
9	0 X 1 1	1	f=X for MEV=0 and f=1 for MEV=1,enter 1

Minimization procedure for MEV/EVM:

- 1) Write all the variables (original and complimented forms are treated as two different variables) in the map as 0, leave 0's, minterms and don't cares as it is and obtain the SOP expression.
- 2) Select one variable and make all occurrences of that variable as 1, write minterms (1's) as don't cares, leave 0's and don't cares as it is. Now, obtain the SOP expression by multiply the obtained SOP expression with the concerned variable.
- 3) Repeat step 2 for all the variables in the k-map.
- 4) SOP of MEV/EVM is obtained by ORing all the obtained SOP expressions.

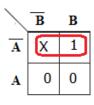
Example - A 3-variable function can be defined as a function of 2-variables if the output is written in terms of third variable.

Consider a function F(A,B,C) = (0,1,2,5)

A	В	C	F			in terms of `C',	Ente Map		Variable
0	0	0	1	writter	as:		i lap	13	
0	0	1	1	A	В	1 F			
0	1	0	1	0	0		/	B	В
0	1	1	0	O	0	1	A	1	Ē
1	0	0	0	0	1	C'	A		0
1	0	1	1	1	0	C	А	C	U
1	1	0	0	1	1	0			
1	1	1	0						

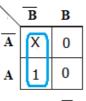


 $SOP1 = \overline{A} \overline{B}$



Step 2:

$$SOP2 = \overline{A} \overline{C}$$



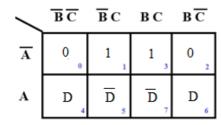
$$SOP3 = BC$$

$$F = \overline{A} \overline{B} + \overline{A} \overline{C} + \overline{B} C$$

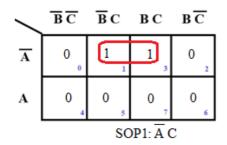
Solve $S=F(A,B,C,D)=\Sigma m(2,3,6,7,9,10,13,14)$ using MEV to get minimum SOP expression.

A	В	С	D	Y	MEV	
0	0	0	0	0	0	
0	0	0	1	0		
0	0	1	0	1	1	
0	0	1	1	1	1	
0	1	0	0	0	_	
0	1	0	1	0	0	
0	1	1	0	1		
0	1	1	1	1	1	
1	0	0	0	0	Б	
1	0	0	1	1	D	
1	0	1	0	1	D	
1	0	1	1	0	ע	
1	1	0	0	0	ъ	
1	1	0	1	1	D	
1	1	1	0	1	D	
1	1	1	1	0	ע	

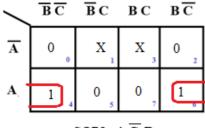
SOP
$$Y = \overline{A} C + A \overline{C} D + C \overline{D}$$



1)Write all the variables as 0, leave minterms, 0's and don't cares as it is and obtain the SOP expression.

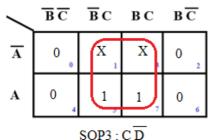


2) Replace all occurances of D with 1, all occurrences of D' with 0 and all 1's with don't care. Leave 0's and don't cares as it is.



 $SOP2 : A \overline{C} D$

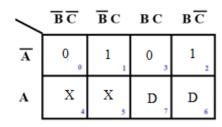
3) Replace all occurrences of D' with 1, all occurrences of D with 0 and all 1's with don't care. Leave 0's and don't cares as it is.



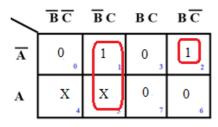
Solve $S=F(A,B,C,D)=\Sigma m(2,3,4,5,13,15) + \Pi d(8, 9, 10, 11)$ using MEV to get minimum SOP expression.

A	В	С	D	Y	MEV	
0	0	0	0	0	_	
0	0	0	1	0	0	
0	0	1	0	1	1	
0	0	1	1	1	1	
0	1	0	0	1	1	
0	1	0	1	1	•	
0	1	1	0	0	0	
0	1	1	1	0	V	
1	0	0	0	X	X	
1	0	0	1	X		
1	0	1	0	X	X	
1	0	1	1	X	71	
1	1	0	0	0	Ъ	
1	1	0	1	1	D	
1	1	1	0	0	D	
1	1	1	1	1	ע	



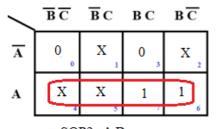


1)Write all the variables as 0, leave minterms, 0's and don't cares as it is and obtain the SOP expression.



 $SOP1:\overline{B}C,\overline{A}B\overline{C}$

2) Replace all occurances of D with 1, all occurrences of D' with 0 and all 1's with don't care. Leave 0's and don't cares as it is.



SOP2 : A D

3) Replace all occurrences of D' with 1, all occurrences of D with 0 and all 1's with don't care. Leave 0's and don't cares as it is.

\	BC	BC	ВС	ΒC
Ā	0. 0	X	0 3	X
A	X 4	X	0 ,	0
		NO S	OP	

NO SOP

References

Books:

- 1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning, 2019
- 2. Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.

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- 1. https://www.geeksforgeeks.org/introduction-of-k-map-karnaugh-map/
- 2. https://www.tutorialspoint.com/digital_circuits/digital_circuits_k_map_method.htm
- 3. https://www.tutorialspoint.com/digital_circuits/digital_circuits_quine_mccluskey_tabular_method.htm
- 4. https://www.geeksforgeeks.org/variable-entrant-map-vem-in-digital-logic/
- 5. https://www.allaboutcircuits.com/technical-articles/everything-about-the-quine-mccluskey-method/

Video Links:

- 1. https://youtu.be/5c16CswEG2A
- 2. https://youtu.be/lo3pTQ09QGI
- 3. https://youtu.be/PInDAFIQQNI
- 4. https://youtu.be/224iz7EAEXA
- 5. https://youtu.be/-A2aoqWckvs
- 6. https://youtu.be/CoMQLMqVFTI
- 7. https://youtu.be/1tYF6SyKLjs
- 8. https://youtu.be/LgS8HaHEcWM

Question bank

- Prove the universality of NAND and NOR Gates.
- 2] State Duality theorem. State and prove De Morgan's first & second theorems.
- 3] Determine the minimum sum-of-products for -

a) f1 (a, b, c) =
$$\sum (1, 3, 4, 5, 6, 7)$$

4] Determine the minimum product-of-sums for -

a) f1 (a, b, c) =
$$\sum (0, 1, 2, 3, 4, 6, 7)$$

5] Solve for the simplified Boolean expression using K-Map:

$$f1(a,b,c,d) = \bar{a}\bar{c}d + \bar{a}cd + \bar{b}\bar{c}\bar{d} + a\bar{b}c + \bar{a}\bar{b}c\bar{d}$$

$$f2(a,b,c,d) = (a+b+\bar{d})(\bar{a}+b+\bar{d})(a+\bar{b}+\bar{c}+d)(\bar{a}+\bar{b}+\bar{c}+\bar{d})(\bar{a}+\bar{b}+\bar{c}+\bar{d})$$

6] Find the minimum sum-of-products for —

(a) f1 (a, b, c) =
$$m0 + m2 + m5 + m6$$

(b) f2 (d, e, f) =
$$\sum m (0, 1, 2, 4)$$

(c) f3 (r, s, t) =
$$rt + rs + r's$$
)

(d)
$$f4(x, y, z) = M0 . M5$$

- 7] Design a 3-input, 1-output, minimal two-level gate combinational circuit; which has an output equal to 1 when majority of its inputs are at logic 1, and has output 0 when majority of inputs are at logic 0.
- 8] Design a minimal sum and minimal product combinational gate circuit to generate the odd parity bit for an 8421 BCD code.
- 9] Design (a) Binary-to-Gray Code Converter, and (b) Gray-to-Binary Code Converter
- [10] A switching circuit has two control inputs (C1 and C2), two data inputs (X1 and X2), and one output
- (Z). The circuit performs one of the logic operations AND, OR, EQU (equivalence), or XOR (exclusive
- OR) on the two data inputs. The function performed depends on the control inputs:

C ₁	C ₂	Function Performed by Circuit
0	0.	OR
0	1	XOR
1	0	AND
3	1	EQU

- (i) Derive a truth table for Z
- (ii) Use a Karnaugh Map to find minimum AND-OR Gate Circuit to realize Z.

11] A logic circuit realizing the function f has four inputs a, b, c, d. The three inputs a, b, and c are the binary representation of the digits 0 through 7 with a being the most significant bit. The input d is an odd-parity bit; that is, the value of d is such that a, b, c, and d always contains an odd number of 1's. (For example, the digit 1 is represented by abc = 001 and d = 0, and the digit 3 is represented by abcd = 0111.) The function f has value 1 if the input digit is a prime number. (A number is prime if it is divisible only by itself and 1; 1 is considered to be prime, and 0 is not.)

- a. Draw a Karnaugh map for f
- Find all prime implicants of f
- Find all minimum sum of products for f
- d. Find all prime implicants of f*
- e. Find all minimum product of sums for f.
- 12] Using Quine-McCluskey method, simplify;

a)
$$f'(a, b, c, d) = \sum m(3, 4, 5, 7, 10, 12, 14, 15) + \sum d(2)$$

b)
$$f(a, b, c, d) = \sum m(1, 5, 7, 9, 11, 12, 14, 15)$$

c)
$$f(a, b, c, d) = \sum m(0, 1, 3, 5, 6, 7, 8, 10, 14, 15)$$

d)
$$f(a, b, c, d) = \sum m(1, 3, 4, 5, 6, 7, 10, 12, 13) + \sum d(2, 9)$$

e)
$$f(a, b, c, d) = \sum m(9, 12, 13, 15) + \sum d(1, 4, 5, 7, 81, 11, 14)$$
.

University Questions:

2018 January

- 1) a. Find the minimum SOP and minimum POS expressions for the following function using K-map. $f(A, B, C, D) = \sum_{m} (1, 3, 4, 11) + \sum_{d} (2, 7, 8, 12, 14, 15)$. (06 Marks)
 - b. What are the disadvantages of K-map method? How they are overcome in Quine Mccluskey method. Simplify following function using Q-M method f(A, B, C, D) = Σ_m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14).
 - c. What is Map-Entered Variable method? Using MEV method simplify following function: $f(A, B, C, D) = \sum_{m} (2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11).$ (06 Marks)

OR

- a. With the help of flow chart explain how to determine minimum sum of products using Karnaugh map.
 (06 Marks)
 - b. Using Q-M method simplify the following function $F(A, B, C, D) = \sum_{m}(2, 3, 7, 9, 11, 13) + \sum_{d}(1, 10, 15).$ c. With example explain Petrik's method. (06 Marks)

2019 July