⚠ You have previously submitted this assignment with David Rama Jimeno. Group can only change between different assignments.

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COMP.CE.240 (/comp.ce.240/spring-2024/) / 3. Exercise 1 (/comp.ce.240/spring-2024/E01/) / 3.1 Exercise 01: General issues and introduction to Modelsim

Assignment description (/comp.ce.240/spring-2024/E01/introduction/)	My submissions (1/1000)

This course has already ended.

Exercise 01: General issues and introduction to Modelsim

At first we will get familiar with all the necessary tools that are used on this course.

First tool is the Mentor Graphics ModelSim (https://en.wikipedia.org/wiki/ModelSim) -simulator. It is powerful, but still easy to use simulator, which is used in industry very widely. It supports the most common hardware description languages (VHDL/Verilog/SystemVerilog/SystemC) and also mixed-language designs.

In this exercise we simulate and verify the functionality of a small VHDL-block and revise the general arrangements of the exercises.

The phases in practice:

1. You can work remotely and access the servers using VNC connection following the instructions (https://intra.tuni.fi/en/handbook?page=2640) in intra
   or optionally work in class TC219
2. Register yourself to some exercise group in the course Moodle
   - Use also the "Form a group" -tool in Plussa to get paired with your exercise partner. **From now on every time when returning an exercise, please double check that you are submitting as a group** (in the top right corner and the bottom of the page).

3. Do the ModelSim-tutorial (https://plus.tuni.fi/comp.ce.240/spring-2024/material/modelsim_tutorial/). The tutorial is made using Linux as an example but it can

be applied also with Windows. For that reason it is also somewhat outdated e.g. all the makefiles related stuff don't hold for Windows.

4. The exercises will be returned by Git version control system. If you are not familiar with Git, you can fix that by checking e.g. some of the following sources:
    - Git - book (https://git-scm.com/book/en/v2)
    - Git cheatsheet (https://www.git-tower.com/blog/git-cheat-sheet/)

5. Optional: Get to know Emacs (https://www.gnu.org/software/emacs/). It is a great text editor and it has an excellent VHDL mode. There is a bit of a learning curve, but basic usage is quite simple once you know the basic shortcuts. Note that they are some way different than other text editors like Notepad++.
    - You don't need to spend much time for this now, maybe just figure out some basic shortcuts and mess around with them a little. You will become more familiar when you begin writing your own code.
    - Here is a cheat sheet (https://plus.tuni.fi/comp.ce.240/spring-2024/material/emacs-help/) of some of the basic commands.
    - More thorough guides can be found as links from the General information (https://plus.tuni.fi/comp.ce.240/spring-2024/material/misc/) page here in Plussa or from Google.
    - Emacs works for Linux, Windows and MacOS. It is also already installed on the computers in TC219.

Return

Obtain the files specified below and put them under E01 folder in your Git repository once you are assigned them. Remember to do a git push. Return the files also by file return in the bottom of this page. NOTE: It is enough to do the returning on this page before the deadline, as you don't have repositories yet.

- Files to return:
    - `wave.png`
    - `answer01.txt`
- For wave.png:
    - Screen capture of the correctly working system's wave form window so that the input is generated using a macro . Alternatively an exported wave form picture.
- In your answer01.txt:
    - Brief report of the required corrections to example code.
    - Brief report of errors added on purpose to example code and what was their result.
    - Brief report of the input generation. What is the difference between force-commands and test benches coded with VHDL? How many states is in the state machine of the test bench?

wave.png

Choose File No file chosen

answer01.txt

Choose File No file chosen

Submit with David Rama Jimeno Submit

Earned points

1 / 1

Exercise info

Assignment category
VHDL exercises

Your submissions
1 / 1000

Points required to pass
1

Deadline
Sunday, 21 January 2024, 23:59

Late submission deadline
Friday, 31 May 2024, 23:59

Group size
1-2

Total number of submitters
62

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