Ain Shams University
Faculty of Engineering
Third year – Computers and Systems

Report on
PCI Verilog

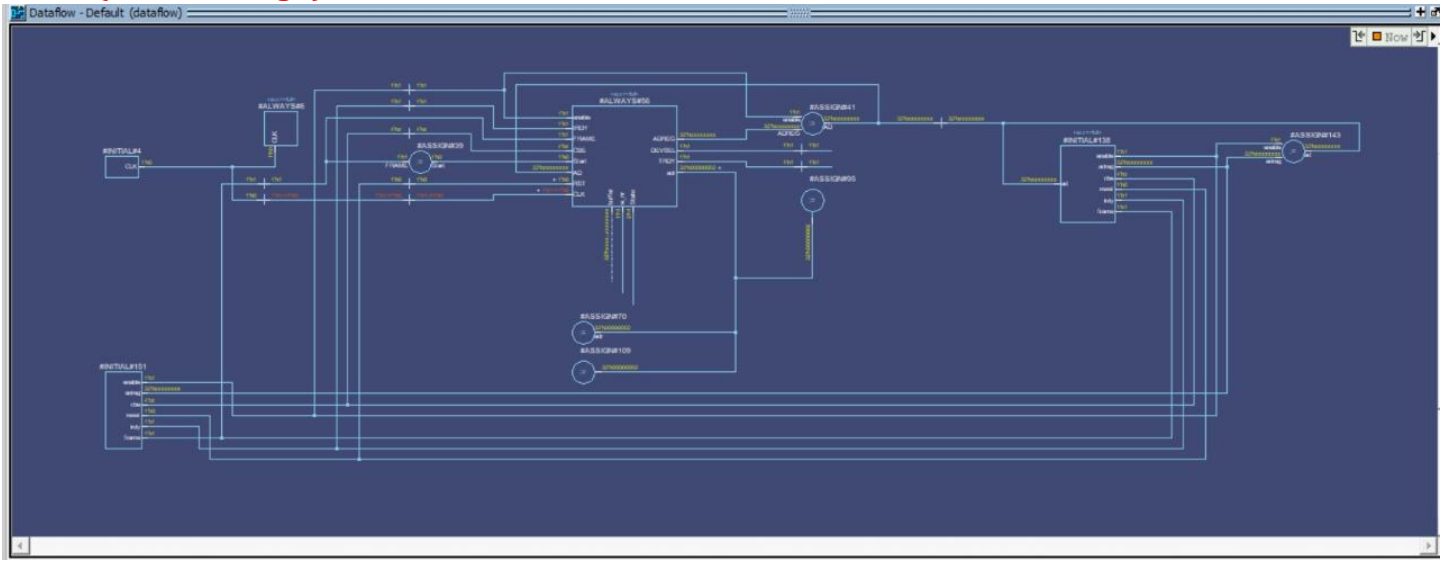
1701596	نوران احمد فؤاد
17E0026	روان خالد احمد
1700553	ريناد مصطفى محمد
1701111	ماهينور عمرو احمد

Cairo 2020

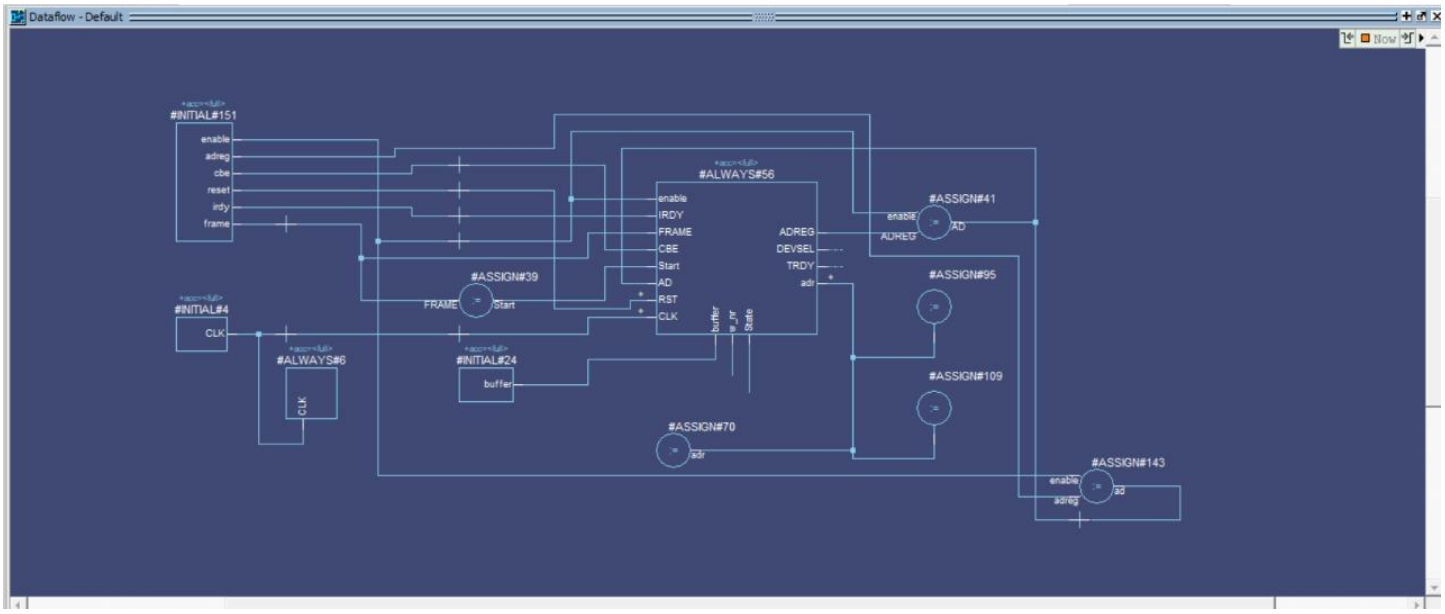
Table of Contents

Block Diagram

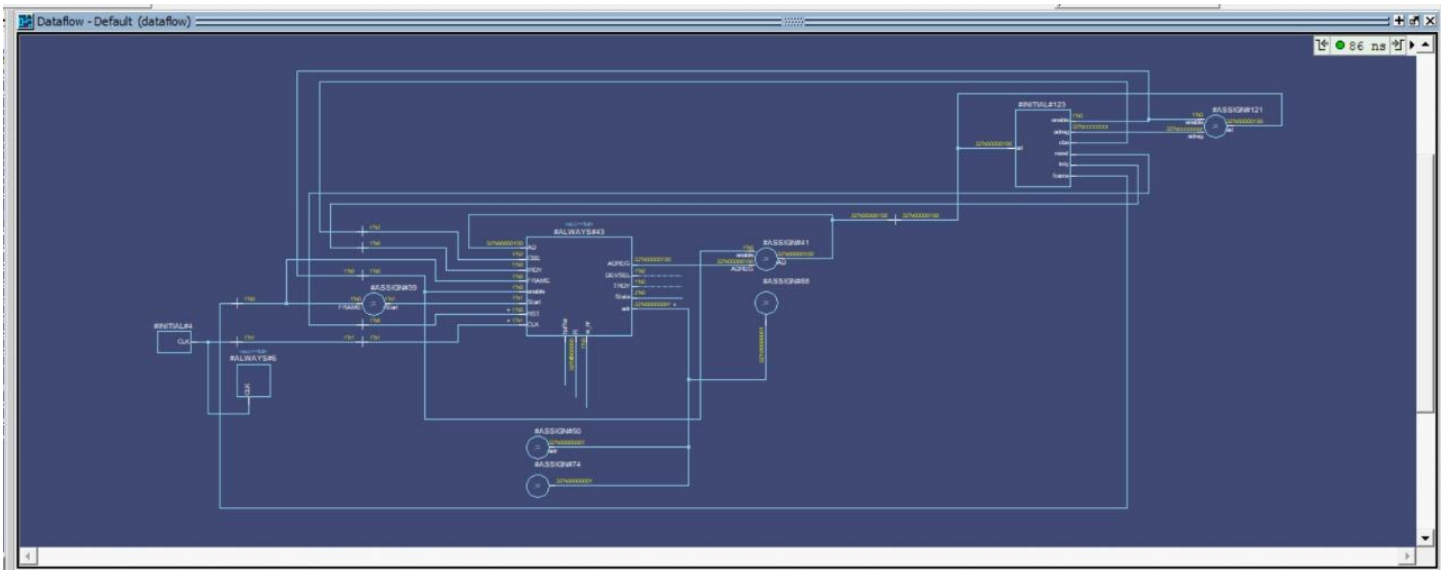
Write (Whole Design)



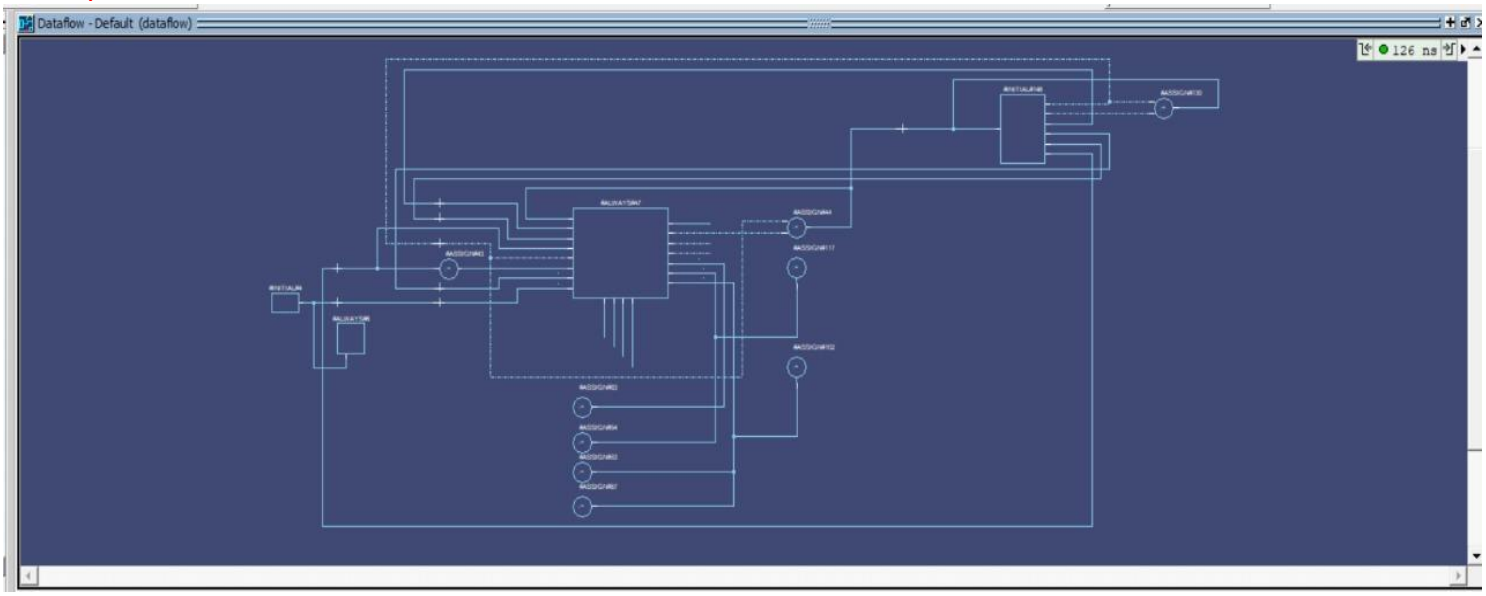
Write (Signals only)



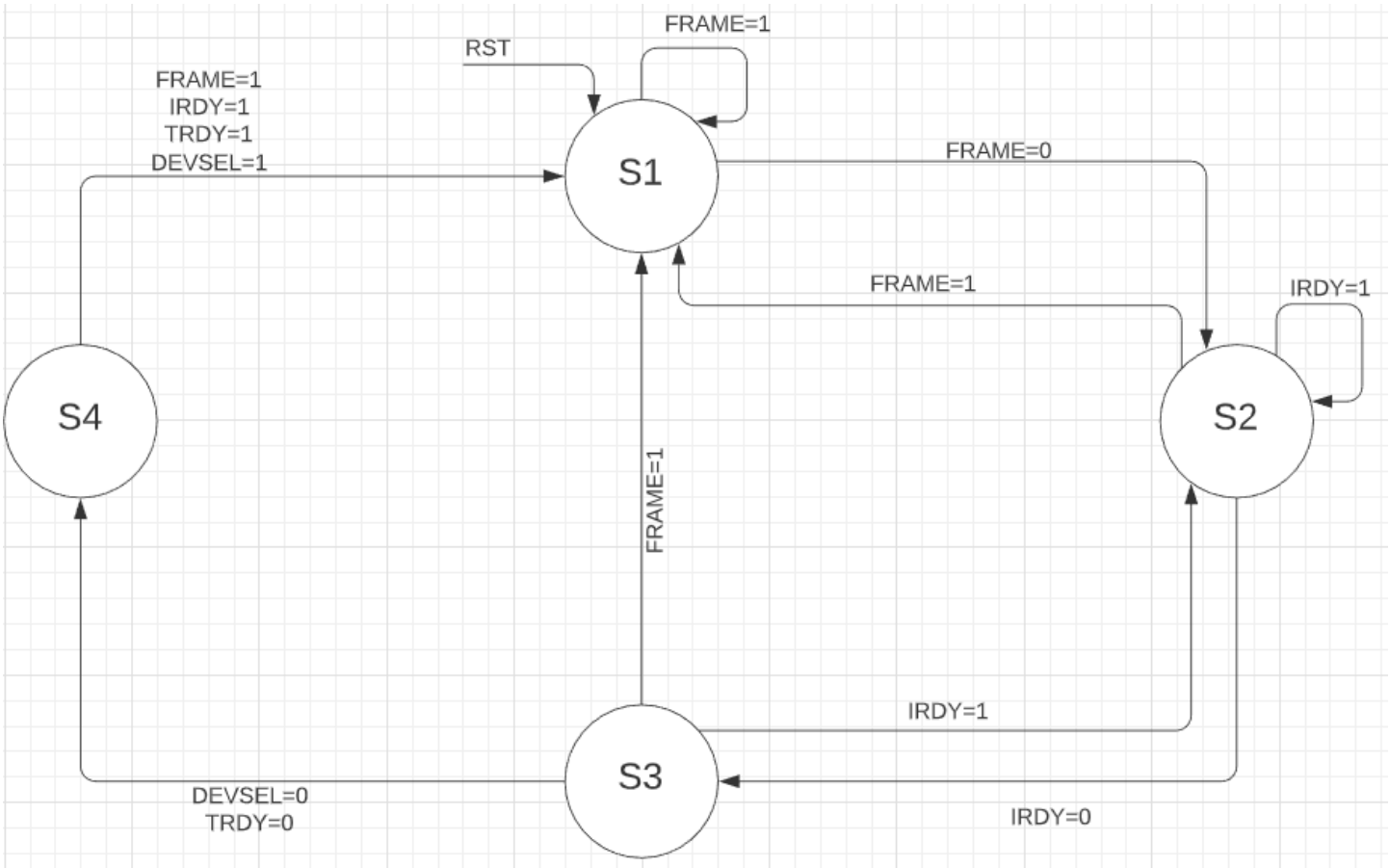
Write/Read



Write/Read with IRDY=1



Finite State Machine Diagram

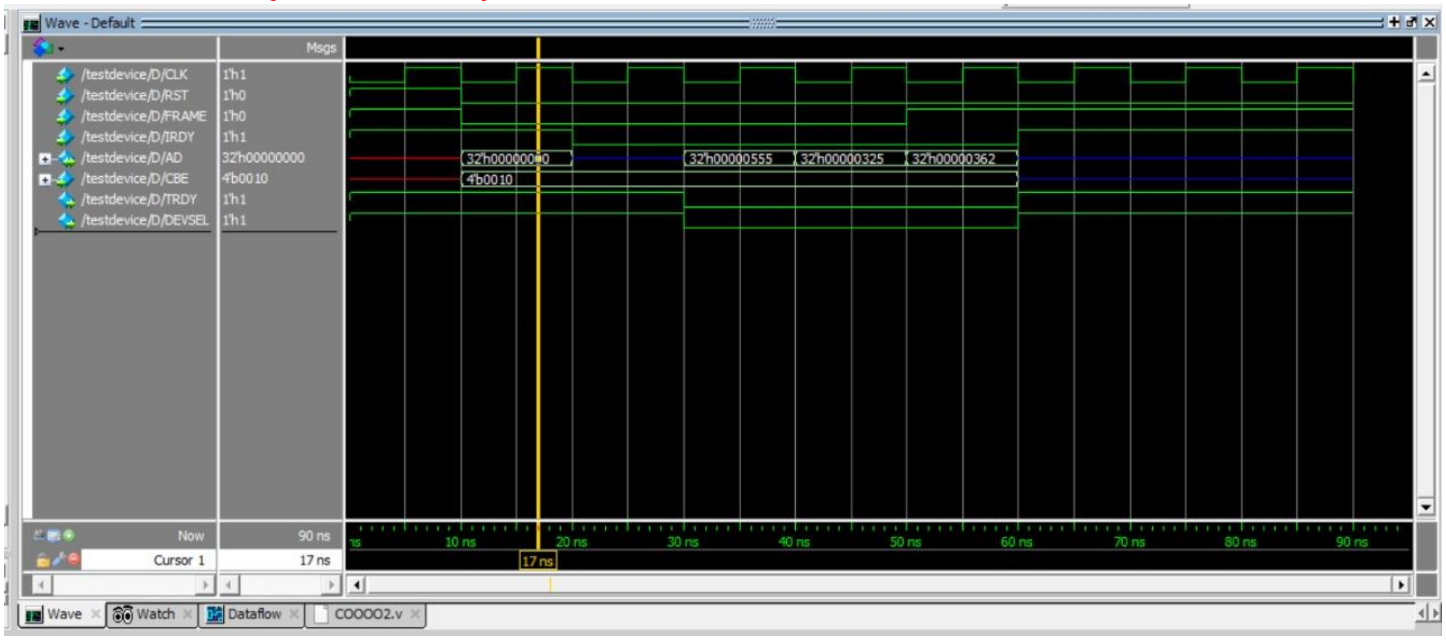


Signals and Their Description

Signal	Description
RST	Starts everything from the beginning, initializes the signals (DEVSEL,TRDY)
Frame	Determines when the transaction starts (Active low)
IRDY	Determines when the Master is ready to send/receive data (Active low)
TRDY	Determines when the Target is ready to send/receive data (Active low)
DEVSEL	Determines when the Target recognizes its address (Active low)
C/BE	In the address phase (C) determines if it's a read or write transaction In the data phase in (Write) , (BE) masks the data sent by the master to the target
AD	Address data multiplexed
enable	Determines whether Address Data (AD) is input or output
R	It's the BE after extension to 32 bits
w_nr	A 1 bit signal determines whether we read or write
ADREG	Used with enable to send or receive data
adr	Address location in the small buffer
ladr	Address location in the large buffer
adreg	Used with enable to send or receive data in Test Bench

Different Scenarios

Read transaction (3 Data Phases)



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a read command (0110) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator tri-states the address in preparation for the target driving read data. The initiator asserts IRDY# low indicating it is ready to capture read data. The target drives TRDY# high indicating it is not yet providing valid read data. (Turn Around)

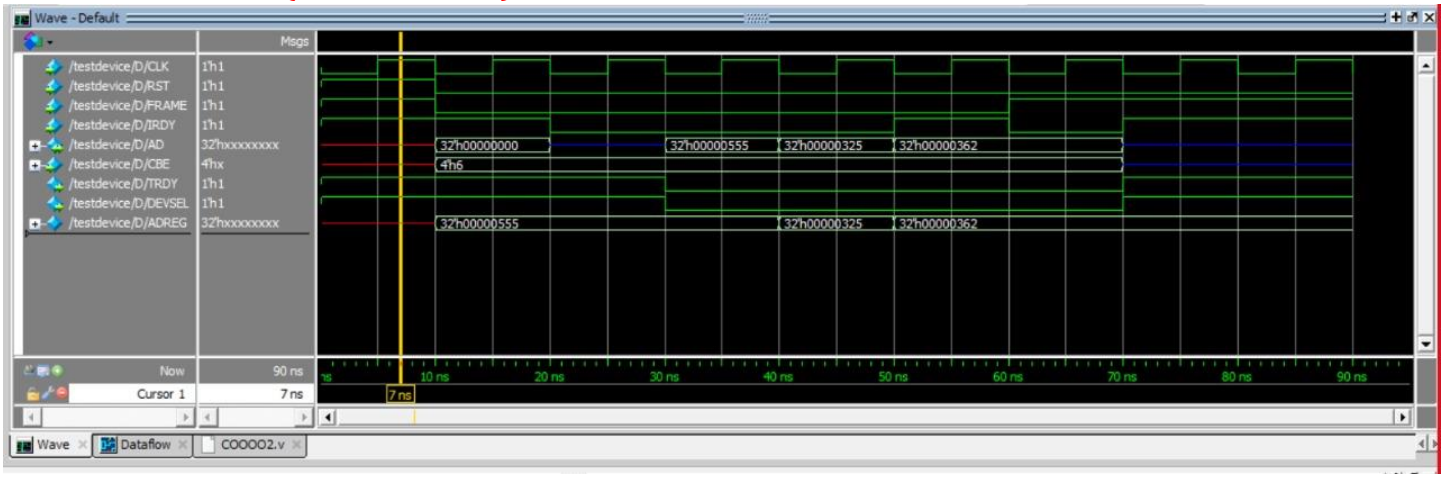
Cycle 4 - The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Medium). The target provides valid data and asserts TRDY# low indicating to the initiator that data is valid. IRDY# and TRDY# are both low during this cycle causing a data transfer to take place. The initiator captures the data. This is the first data phase.

Cycle 5 - The second data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

Cycle 6 - The third data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target. The initiator drives FRAME# high indicating this is the final data phase (master termination).

Cycle 7 - FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated.

Read with IRDY=1 (3 Data Phases)



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a read command (0110) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator tri-states the address in preparation for the target driving read data. The initiator asserts IRDY# low indicating it is ready to capture read data. The target drives TRDY# high indicating it is not yet providing valid read data. (Turn Around)

Cycle 4 - The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Medium). The target provides valid data and asserts TRDY# low indicating to the initiator that data is valid. IRDY# and TRDY# are both low during this cycle causing a data transfer to take place. The initiator captures the data. This is the first data phase.

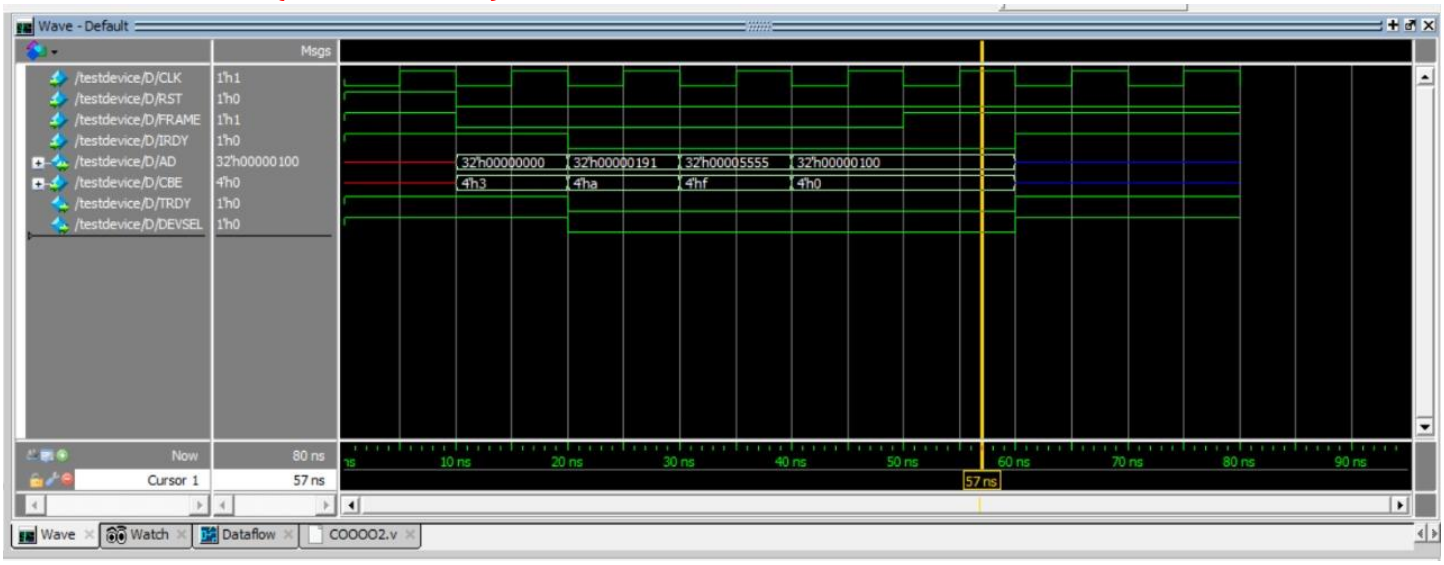
Cycle 5 - The second data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

Cycle 6 - The initiator deasserts IRDY# indicating it is not ready to capture the next data.

Cycle 7 - The initiator asserts IRDY# low it's now ready to capture the next data. The third data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target. The initiator drives FRAME# high indicating this is the final data phase (master termination).

Cycle 8 - FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated.

Write transaction (3 Data Phases)



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a write command (0111) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator drives valid write data and byte enable signals. The initiator asserts IRDY# low indicating valid write data is available. The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Fast). The target drives TRDY# low indicating it is ready to capture data. The first data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

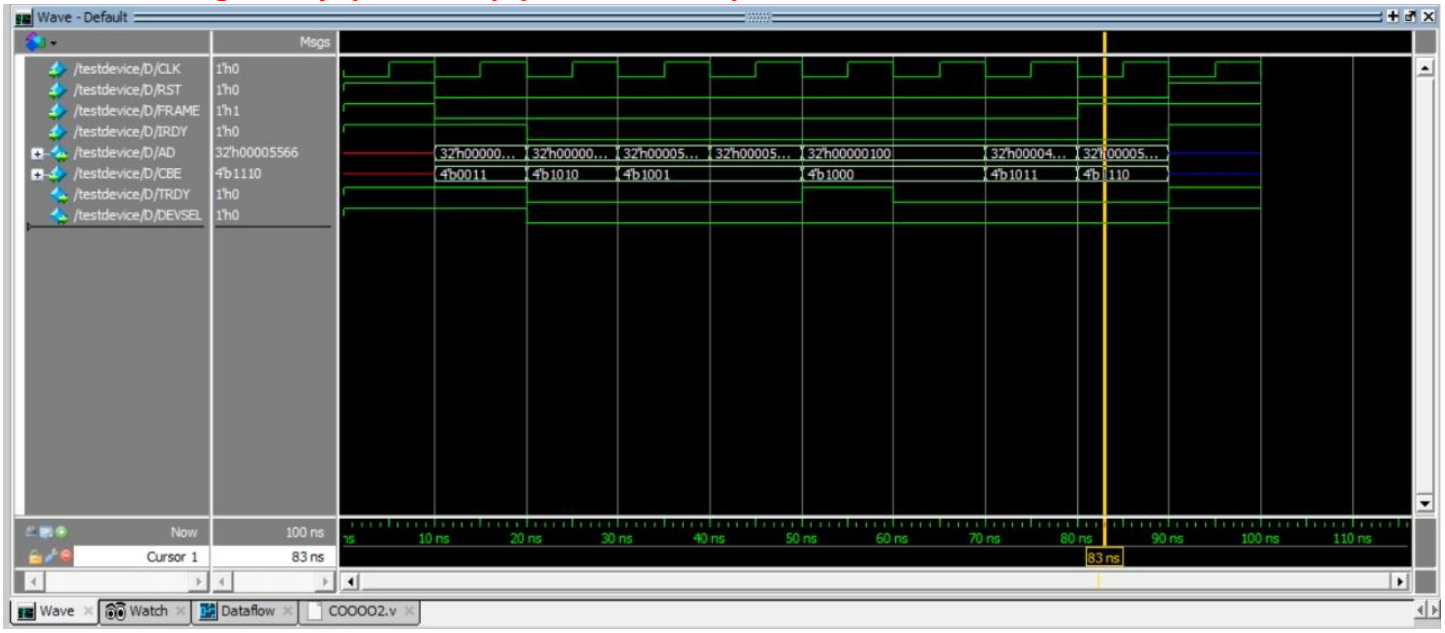
Cycle 4 - The initiator provides new data and byte enables. The second data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 5 - The initiator provides new data and byte enables. The third data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 6 - The initiator drives FRAME# high indicating this is the final data phase.

Cycle 7 - FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated.

Write with target busy (2 Buffers) (6 Data Phases)



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a write command (0111) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator drives valid write data and byte enable signals. The initiator asserts IRDY# low indicating valid write data is available. The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Fast). The target drives TRDY# low indicating it is ready to capture data. The first data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 4 - The initiator provides new data and byte enables. The second data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 5 - The initiator provides new data and byte enables. The third data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Now the first buffer is full and we have to move the data to another larger buffer so the first one would be empty and ready to receive data again.

Cycle 6 - The initiator provides new data and byte enables. The target deasserts TRDY# indicating it is not ready to capture the next data.

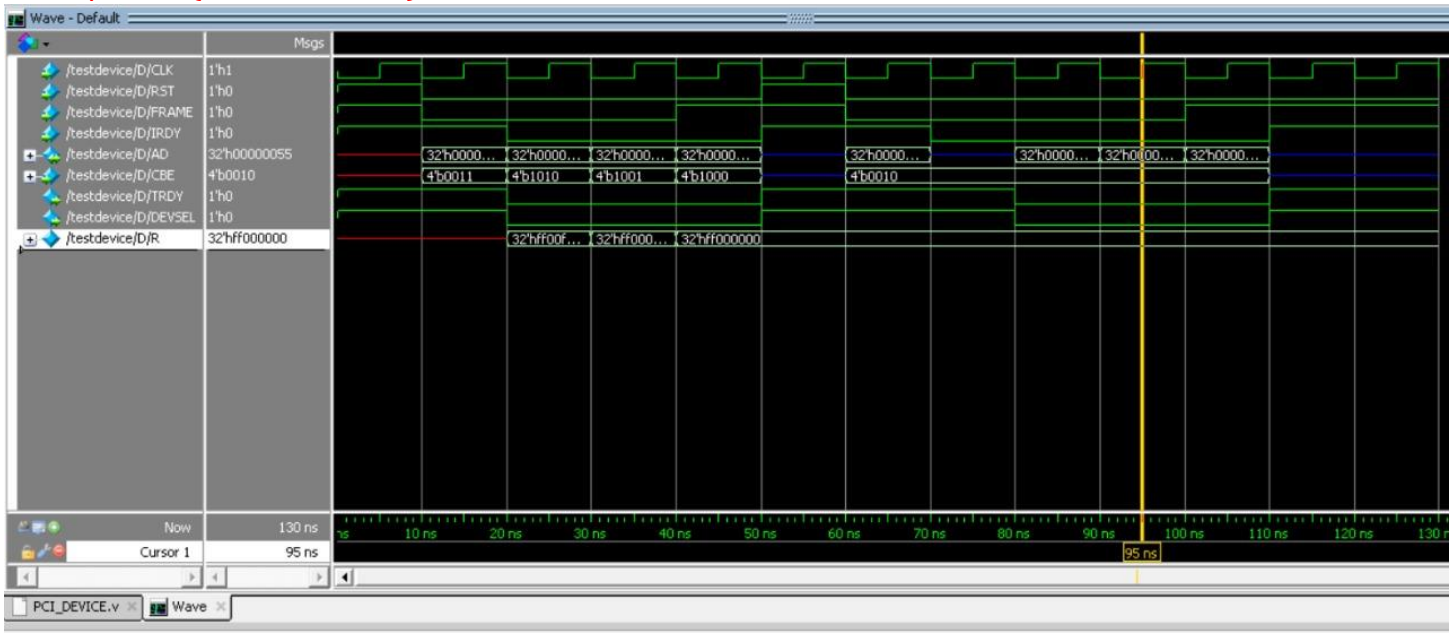
Cycle 7 - The target becomes ready and asserts TRDY# low. The fourth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 8 - The initiator provides new data and byte enables. The fifth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 9 - The initiator provides new data and byte enables. The sixth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data. The initiator drives FRAME# high indicating this is the final data phase.

Cycle 10 - FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated.

Write/Read (3 Data Phases)



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a write command (0111) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator drives valid write data and byte enable signals. The initiator asserts IRDY# low indicating valid write data is available. The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Fast). The target drives TRDY# low indicating it is ready to capture data. The first data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 4 - The initiator provides new data and byte enables. The second data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 5 - The initiator provides new data and byte enables. The third data phase occurs as both IRDY# and TRDY# are low. The target captures the write data. The initiator drives FRAME# high indicating this is the final data phase.

Cycle 6 – FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated. (Turn Around)

Cycle 7 – FRAME# is asserted low and the initiator (Master) asserts a valid address and places a read command (0110) on the C/BE# signals. This is the address phase.

Cycle 8 - The initiator tri-states the address in preparation for the target driving read data. The initiator asserts IRDY# low indicating it is ready to capture read data. The target drives TRDY# high indicating it is not yet providing valid read data. (Turn Around)

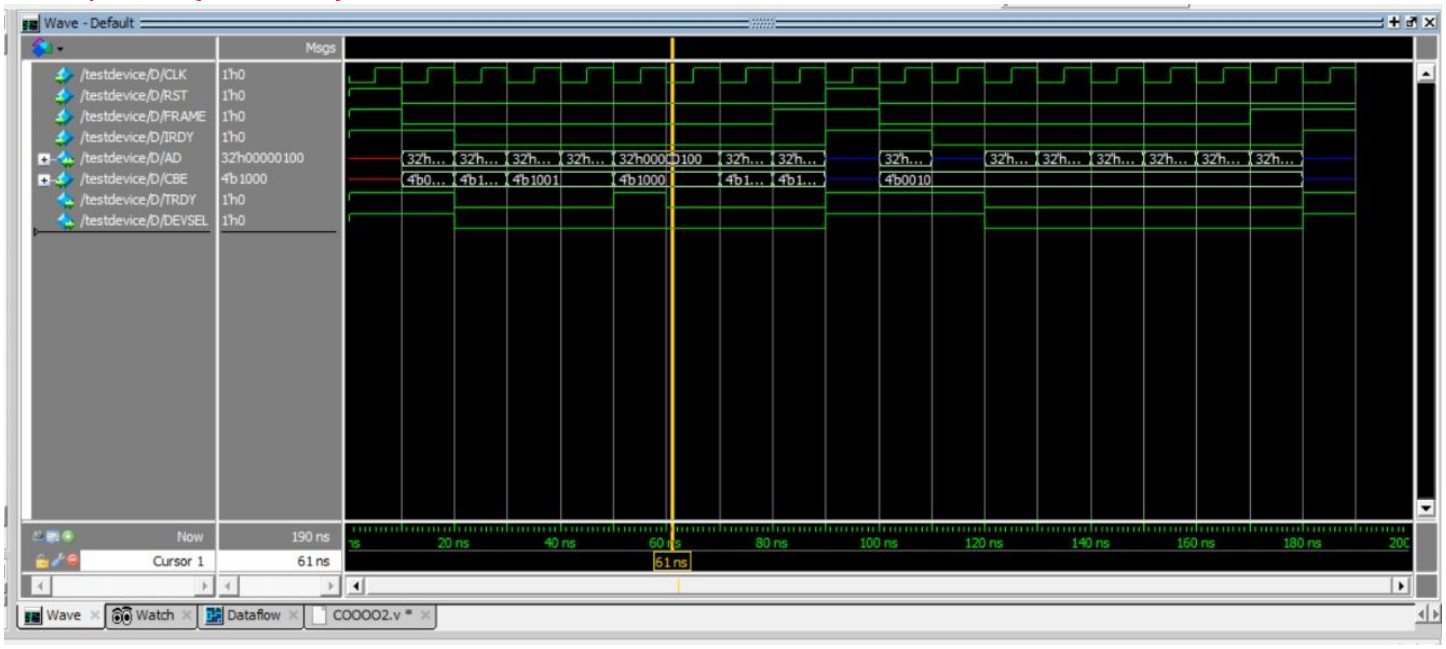
Cycle 9 - The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Medium). The target provides valid data and asserts TRDY# low indicating to the initiator that data is valid. IRDY# and TRDY# are both low during this cycle causing a data transfer to take place. The initiator captures the data. This is the first data phase.

Cycle 10 - The second data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

Cycle 11 - The third data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target. The initiator drives FRAME# high indicating this is the final data phase (master termination).

Cycle 12 – FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated. (Turn Around)

Write/Read (2 Buffers). Read from the small buffer first



Cycle 1 - The bus is idle.

Cycle 2 - The initiator (Master) asserts a valid address and places a write command (0111) on the C/BE# signals. This is the address phase.

Cycle 3 - The initiator drives valid write data and byte enable signals. The initiator asserts IRDY# low indicating valid write data is available. The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Fast). The target drives TRDY# low indicating it is ready to capture data. The first data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 4 - The initiator provides new data and byte enables. The second data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 5 - The initiator provides new data and byte enables. The third data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Now the first buffer is full and we have to move the data to another larger buffer so the first one would be empty and ready to receive data again.

Cycle 6 - The initiator provides new data and byte enables. The target deasserts TRDY# indicating it is not ready to capture the next data.

Cycle 7 - The target becomes ready and asserts TRDY# low. The fourth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 8 - The initiator provides new data and byte enables. The fifth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data.

Cycle 9 - The initiator provides new data and byte enables. The sixth data phase occurs as both IRDY# and TRDY# are low. The target captures the write data. The initiator drives FRAME# high indicating this is the final data phase.

Cycle 10 - FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated. (Turn Around)

Cycle 11 – FRAME# is asserted low and the initiator (Master) asserts a valid address and places a read command (0110) on the C/BE# signals. This is the address phase.

Cycle 12 - The initiator tri-states the address in preparation for the target driving read data. The initiator asserts IRDY# low indicating it is ready to capture read data. The target drives TRDY# high indicating it is not yet providing valid read data. (Turn Around)

Cycle 13 - The target asserts DEVSEL# low as an acknowledgment it has positively decoded the address (Medium). The target provides valid data and asserts TRDY# low indicating to the initiator that data is valid. IRDY# and TRDY# are both low during this cycle causing a data transfer to take place. The initiator captures the data. This is the first data phase.

Cycle 14 - The second data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

Cycle 15 - The third data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

In the first 3 data phases, the data is being read from the first small buffer which is holding the last 3 data written in it in the write transaction

Cycle 16 - The fourth data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

Cycle 17 - The fifth data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target.

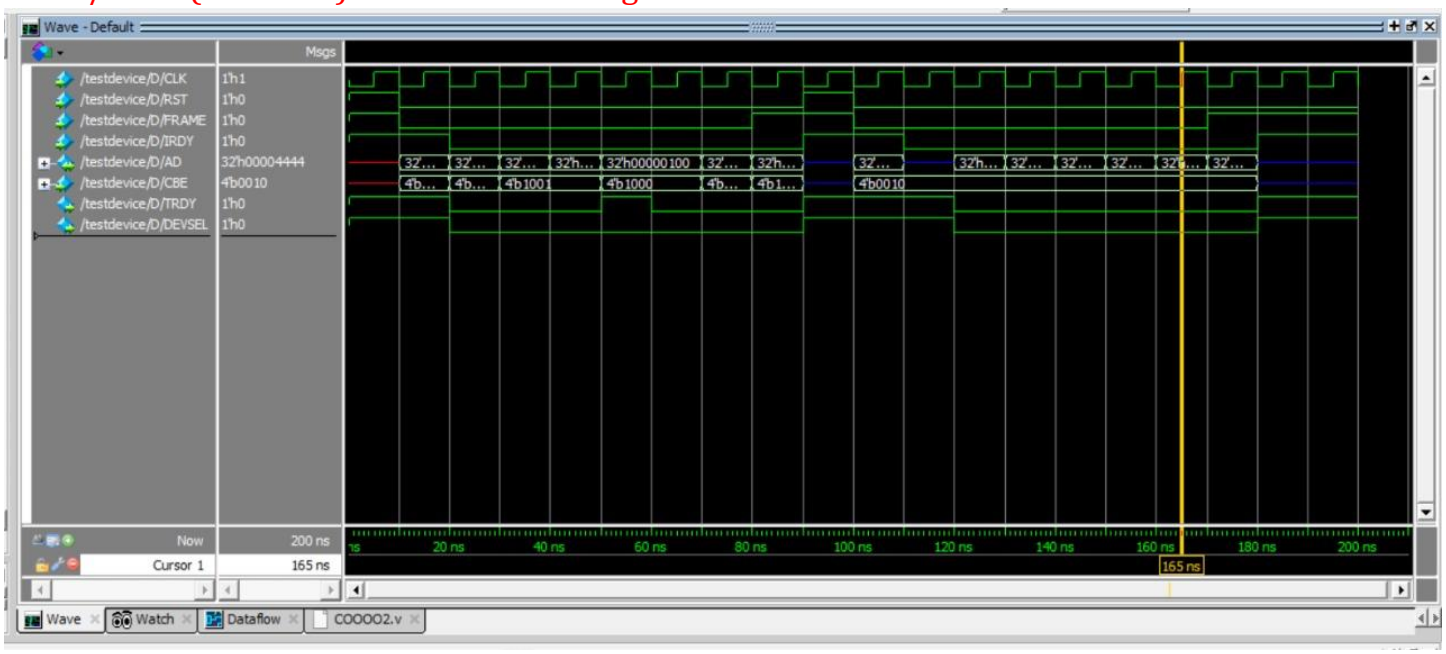
Cycle 18 - The sixth data phase occurs as both IRDY# and TRDY# are low. The initiator captures the data provided by the target. The initiator drives FRAME# high indicating this is the final data phase (master termination).

In the second 3 data phases, the data is being read from the second large buffer which is holding the first 3 data written in the write transaction.

So the data isn't read in the right order.

Cycle 19 – FRAME#, AD, and C/BE# are tri-stated, as IRDY#, TRDY#, and DEVSEL# are driven inactive high for one cycle prior to being tri-stated. (Turn Around)

Write/Read (2 Buffers). Read from the large buffer first



It's the same as the previous scenario BUT in the read transaction:

In the first 3 data phases, the data is being read from the second large buffer which is holding the first 3 data written in the write transaction.

In the second 3 data phases, the data is being read from the first small buffer which is holding the second 3 data written in the write transaction.

So the data is read in the right order.

Table of Contributions

Name	Contribution
نوران احمد فؤاد	Coding and report
روان خالد احمد	Coding and report
ريناد مصطفى محمد	Coding and report
ماهينور عمرو احمد	Coding and report