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PDK

PDK Content

- ❑ Creating New Libraries
- ❑ Primitive Library (Foundry Provided)
- ❑ Digital Standard Cell Library (Foundry Provided standard cell library ”SKY WATER” / Third Party Provided Digital Standard Cell Libraries)
- ❑ Build Space Libraries (Foundry Provided)
- ❑ IO and Periphery Libraries (SKY 130 / Third Party)
- ➢ It contains 5 layers.

File Types

- ❑ Parameterized cell generator
- ❑ Drc Deck / Lvs Deck
- ❑ GDS Generator
- ❑ Library Exchange Format Macros
- ❑ Timing Files
- ❑ Netlists
- ❑ Device Models
- ❑ Schematic / Schematic symbols
- ❑ Verilog Testbench
- ❑ Xspice / Parameterized Cell

What’s the devices that this technology supports?

- ❑ MIM Capacitor MiM Capacitor
- ❑ Varactors

- ❑ Vertical Parallel Plate (VPP) capacitors
- ❑ Diodes
- ❑ NMOS ESD FET
- ❑ 5.0V/10.5V NMOS FET
- ❑ 11V/16V NMOS FET
- ❑ 1.8V low-VT NMOS FET
- ❑ 1.8V NMOS FET
- ❑ 3.0V native NMOS FET
- ❑ 5.0V native NMOS FET
- ❑ 20V NMOS FET
- ❑ 20V isolated NMOS FET
- ❑ 20V native NMOS FET
- ❑ 20V NMOS zero-VT FET
- ❑ Bipolar (NPN)
- ❑ 5.0V/10.5V PMOS FET
- ❑ 10V/16V PMOS FET
- ❑ 1.8V high-VT PMOS FET
- ❑ 1.8V low-VT PMOS FET
- ❑ 1.8V PMOS FET
- ❑ 20V PMOS FET
- ❑ Bipolar (PNP)
- ❑ Generic Resistors
- ❑ P+ poly precision resistors
- ❑ P- poly precision resistors
- ❑ SONOS cells
- ❑ SRAM cells

what is the usage of each layer?

- Metal 1 : Power, Vdd, Vss.
- Metal 2 : I/O ports.
- Metal 3,4,5 : For large designs and decreasing chip resistance.

what are the rule that are available in the DRC?

Antenna Rules