TIMA

Coprocessor FIR AxC

Documentation

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1 Revision History

Date	Version	Description	Author
09/07/2018	1.0	Initial Release	Gabriel Villanova

2 Architecture

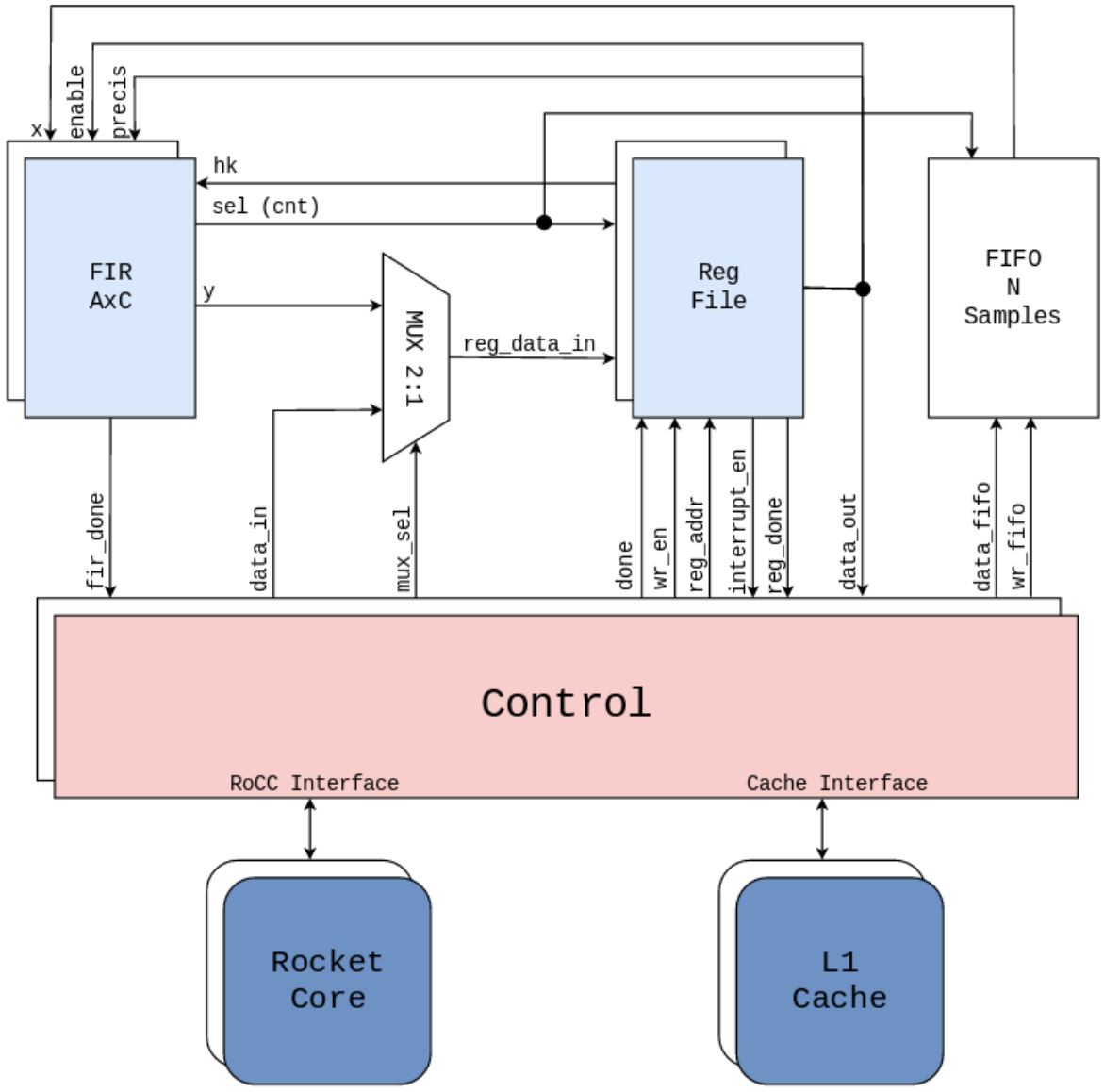

Figure 1: Coprocessor FIR AxC Architecture.

3 ISA

Instruction	Pseudocode	Description	Opcode
fir.mov rs2, rs1	rs2 $\leftarrow rs1$	Move rs1 value to reg. rs2	0b0000000
fir.fifo.put rs1	FIFO(put,rs1)	Put rs1 value into FIFO	0b0000001
fir.str rs2, rs1	Reg[rs2] $\rightarrow Mem[rs1]$	Store Reg[rs2] data in addr. rs1	0b0000010

Table 1: ISA Specification

4 Register Map

Reg. Address	Pseudonym	Description	Access Type
0x00	Coef[0]	Coeficient FIR n=0	Read/Write
0x01	Coef[1]	Coeficient FIR n=1	Read/Write
0x02	Coef[2]	Coeficient FIR n=2	Read/Write
0x03	Coef[3]	Coeficient FIR n=3	Read/Write
...	...	Coeficient FIR n=...	Read/Write
0x1F	Coef[31]	Coeficient FIR n=31	Read/Write
0x20	Precision	Configure the precision to calculate	Read/Write
0x21	Status Register	Status of Coprocessor	Read/Write
0x22	Result Register	Result of FIR AxC operation	Read/Write

Table 2: Register Map FIR AxC

4.1 Status Register

Status Register	**[xLen-1]**	**[xLen-2:2]**	**[1]**	**[0]**
R/W	Done	Reserved	Enable Int.	Enable FIR

Table 3: Status Register

5 Interfaces and Components

5.1 RoCC and L1 Cache Interfaces

5.2 Control

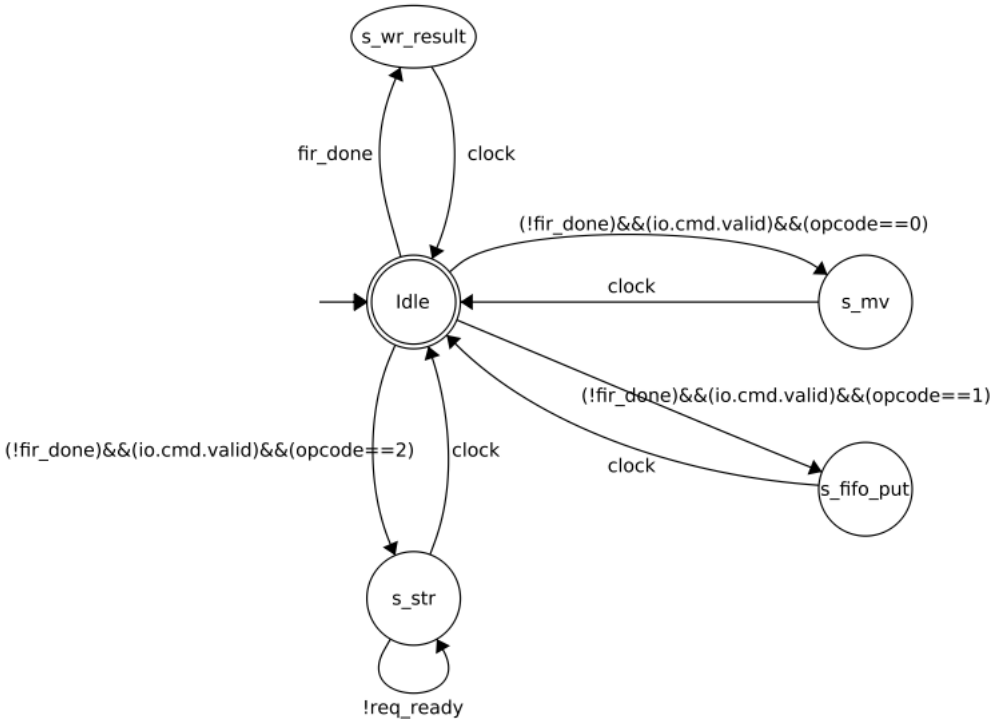

Figure 2: Control FSM.

6 Programming Model

7 Examples of Results

8 Reference