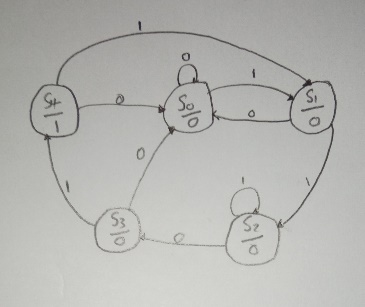
**Overlapping Sequence Detector “1101”**

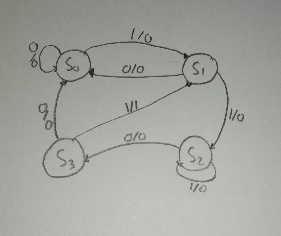
The 1101 detector is a digital circuit that detects the presence of a specific bit sequence 1101 in an incoming data stream. The circuit can be implemented using two different types of Finite State Machines (FSMs): Moore and Mealy. In this report, we will discuss the tradeoffs and differences between these two implementations.

**Moore FSM:**



The Moore FSM has only one output, which depends only on the current state of the machine. This means that the Moore FSM requires more states to implement the same functionality as a Mealy FSM. However, the tradeoff is that the implementation is simpler since the output signal does not depend on the input signal.

**Mealy FSM:**



The Mealy FSM has outputs that depend on both the current state and the input signal. This means that the Mealy FSM requires fewer states to implement the same functionality as a Moore FSM. However, the tradeoff is that the implementation is more complex since the output signal depends on the input signal.

**Verilog Code:** [Please check Phase1-Task3](https://github.com/nourhussin/Chipion_Program)

In conclusion, both types of FSMs have their own tradeoffs and differences. The choice between the two depends on the specific requirements of the application. While Moore FSMs are simpler to design, they require more states to implement the same functionality as a Mealy FSM. Mealy FSMs, on the other hand, are more complex to design but require fewer states to implement the same functionality as a Moore FSM.