LAB 07

Analog IC Design – Xschem and Master Micro Tools gm/ID Design Methodology

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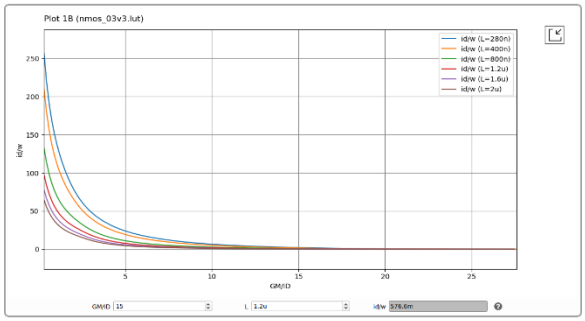
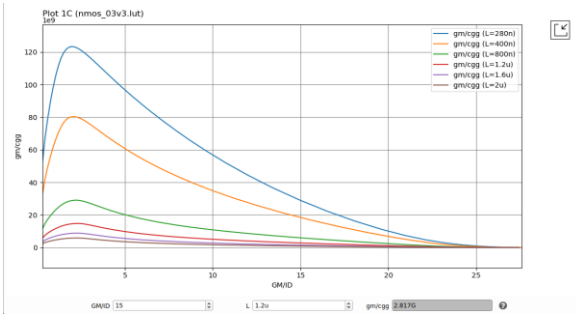
Part 1: gm/ID Design Charts

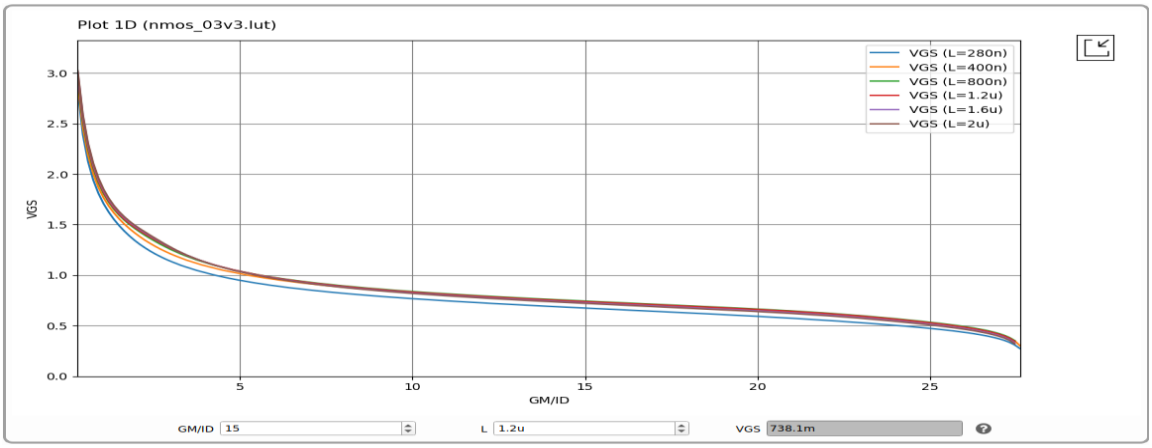
1. NMOS Charts



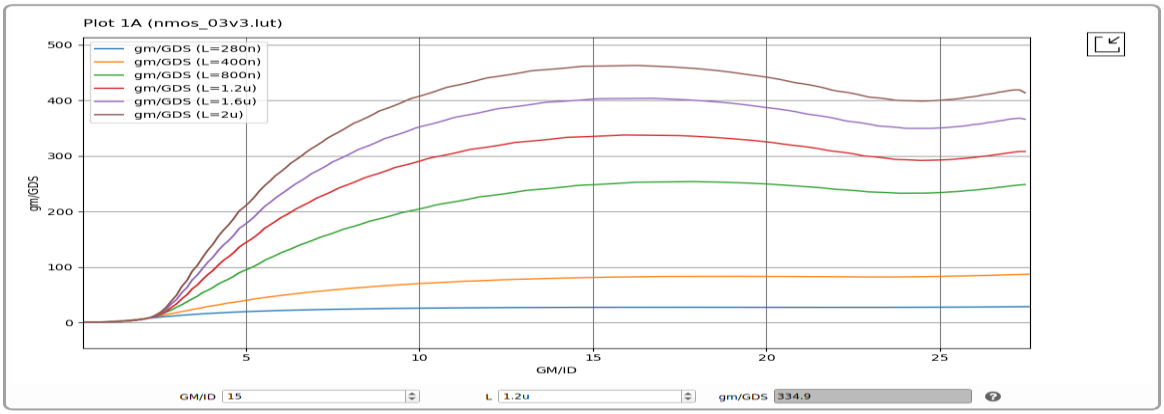
ID/W vs gm/ID



gm/Cgg vs gm/ID

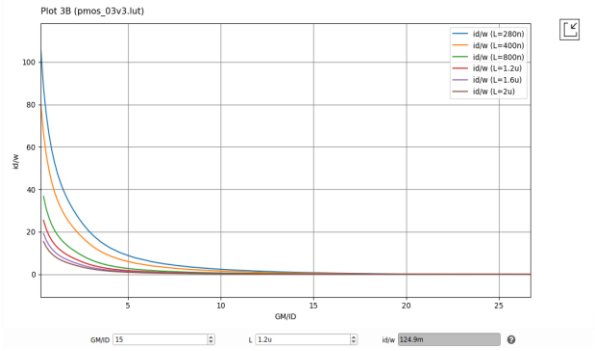


VGS vs gm/ID

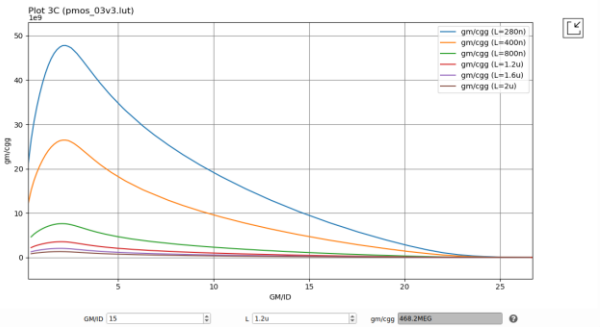


gm/gds vs gm/ID

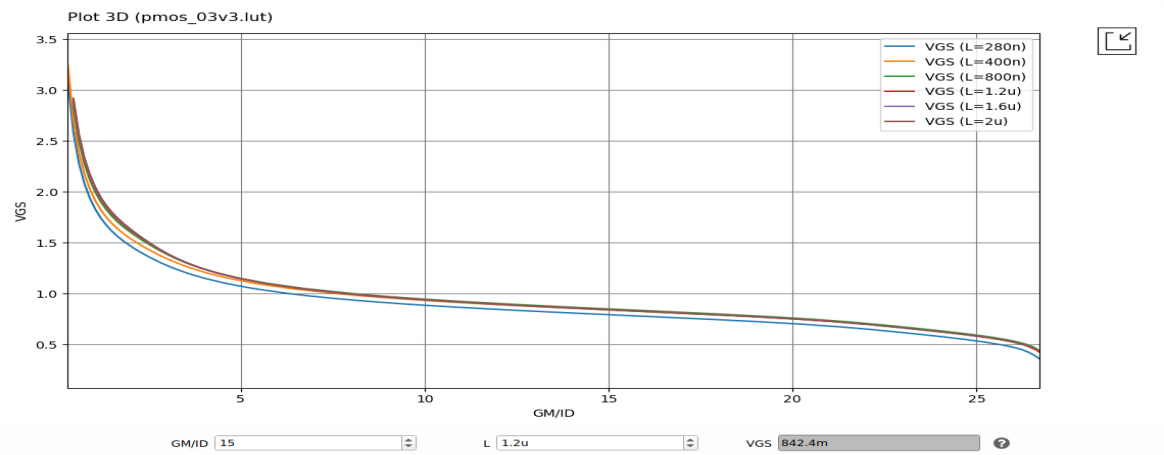
2. PMOS Charts



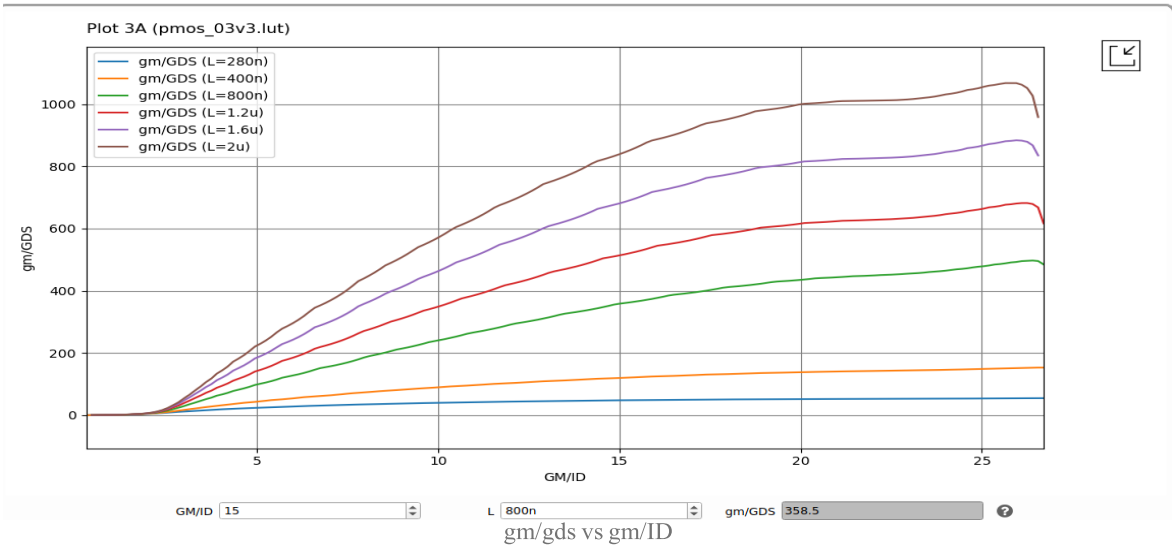
ID/W vs gm/ID



gm/Cgg vs gm/ID



VGS vs gm/ID



gm/gds vs gm/ID

Part 2: OTA Design

1. Desired Specs

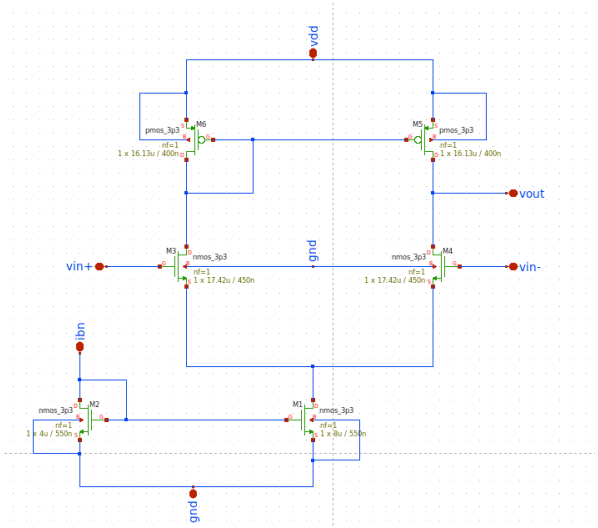
Technology	0.18 µm cmos
Supply voltage	1.8 V
Load	5 pF
Open loop dc voltage gain	>= 34 dB
Cmrr @ dc	>= 74 dB
Phase margin	>= 70º
Cm input range – low	<= 1 V
Cm input range – high	>= 1.5 V
GBW	>= 10 MHz

Desired Specs

The required gain is not high (only 34 dB ≈ 50) so it can be achieved by a simple single stage OTA.
Since the required CMIR is close to the supply voltage, we need to use an NMOS input stage.

Since the type of input pair is NMOS we are going to use sourcing IDC connection.

2. OTA schematic

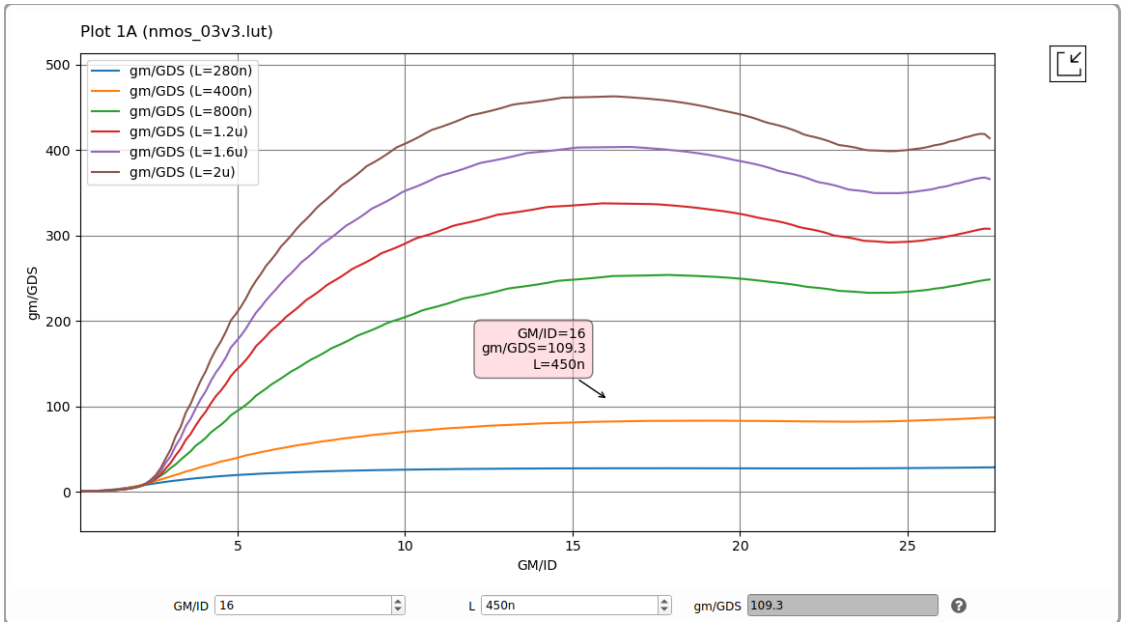


3. OTA design steps

To design 5T OTA, we can divide it into 3 stages (input, current mirror, and tail source stage).

- # Design of input pair:

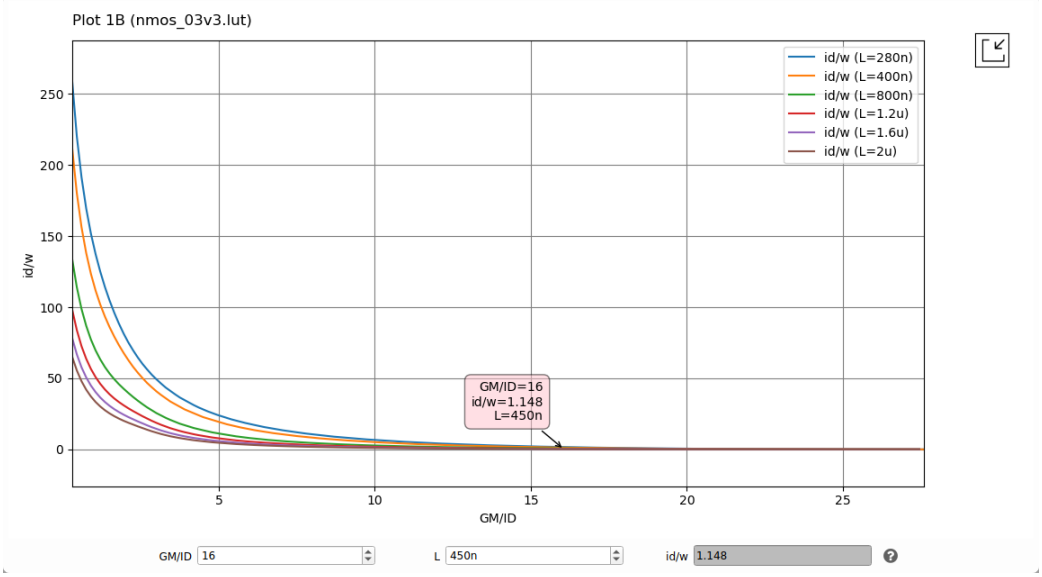
$GBW = gm/\ 2\pi CL \Rightarrow gm = GBW * 2\pi * CL = 314.1\ us$
@ $ID = 40/2 = 20\ uA \Rightarrow gm/id = 16\ S/A$
Then $Ao = gmro/2 > 50$ @$gm\ gds > 100$



gm/gds vs gm/id

From graph we noticed that the least L to achieve our specs is $L \approx 450$ nm

- Now we need to calculate the width of input pair
- So, we are searching for which id/w give us gm/id = 16, L = 450 nm
- from graph we noticed that id/w = 1.148

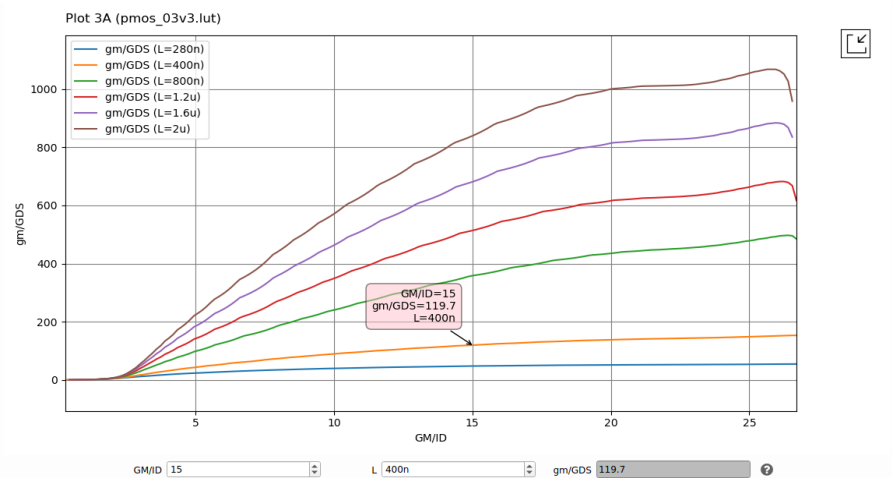


ID/W vs gm/id

For L = 450nm => ID/W=1.148 @ ID = 20uA Then $W \approx 17.42$ um

- # Design of CM load:

By assuming equal gds of input pair = CM Load Gds5,6 < 3.14uS Let gm/id = 15 Gm = id * gm/id = 300us @ gm/gds > 95.5



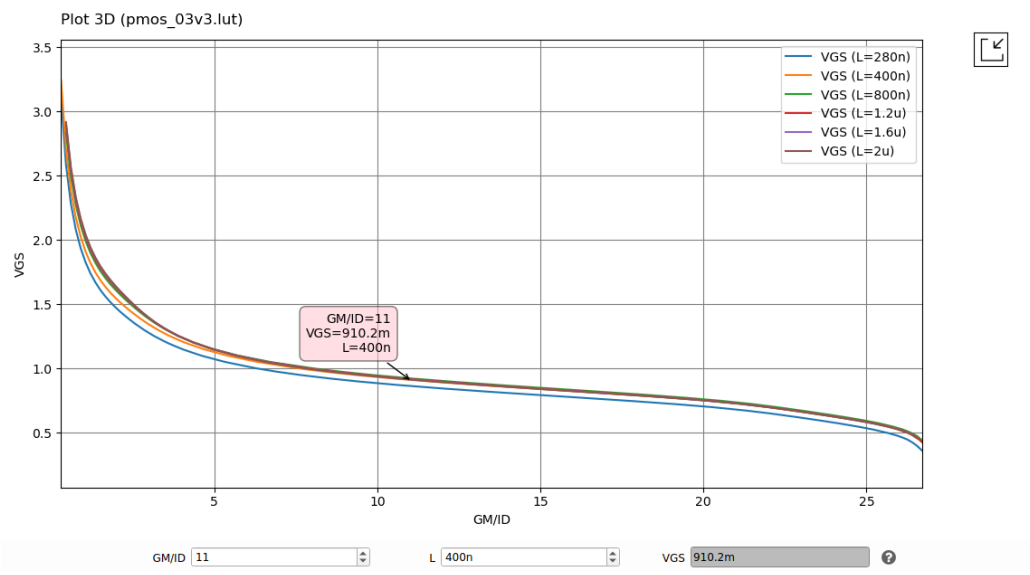
gm/gds vs gm/id

$L \approx 400$ nm

Now We need to Calculate the accurate gm/id, so first we need to calculate vgs
For the CM Load

$Vincm_{MaX}$< VDD-VGS6+VTH3 Then VGS6 <1.0769 V, VGS6 = 1V

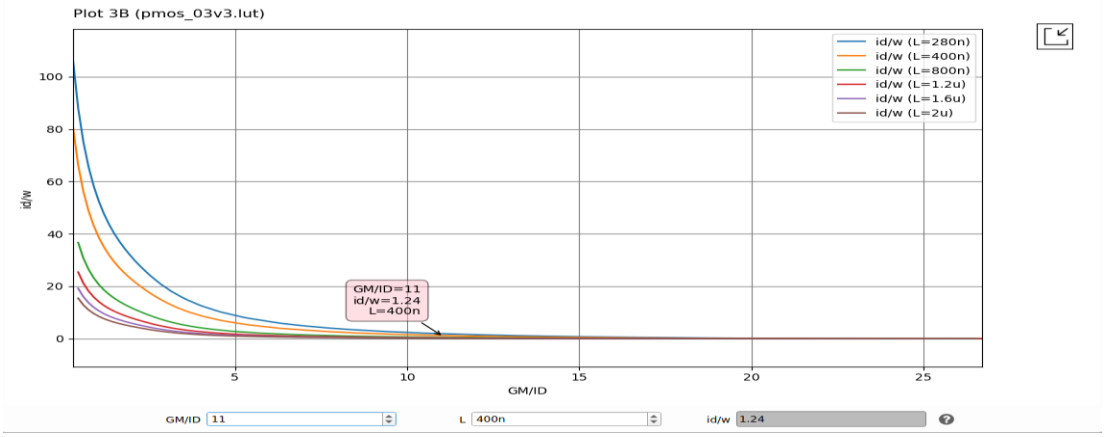
Let's see at which gm/id and L = 0.4 um Vgs will give us this value



vgs vs gm/id

gm/id = 11

Now we need to calculate the width of CM Load so, we see which id/w give us
gm/id = 11, from graph we noticed that id/w =1.24 so W = 16.13 um

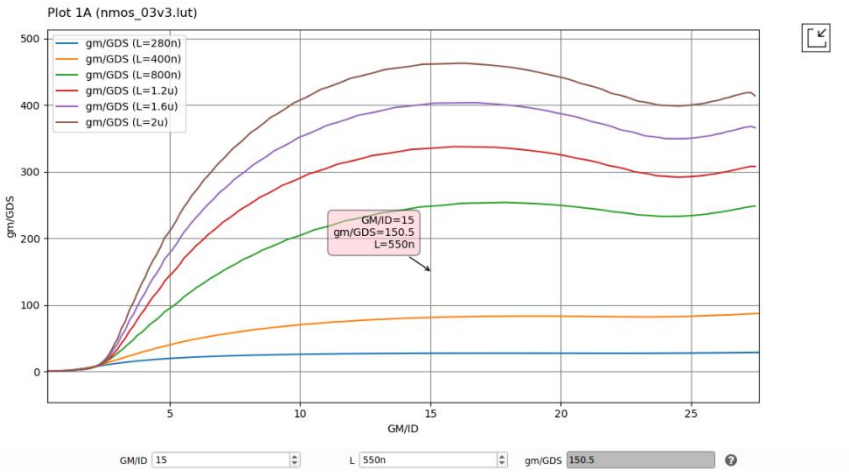


ID/W vs gm/id

Vgs vs gm/ID

- # Design of CM tail:

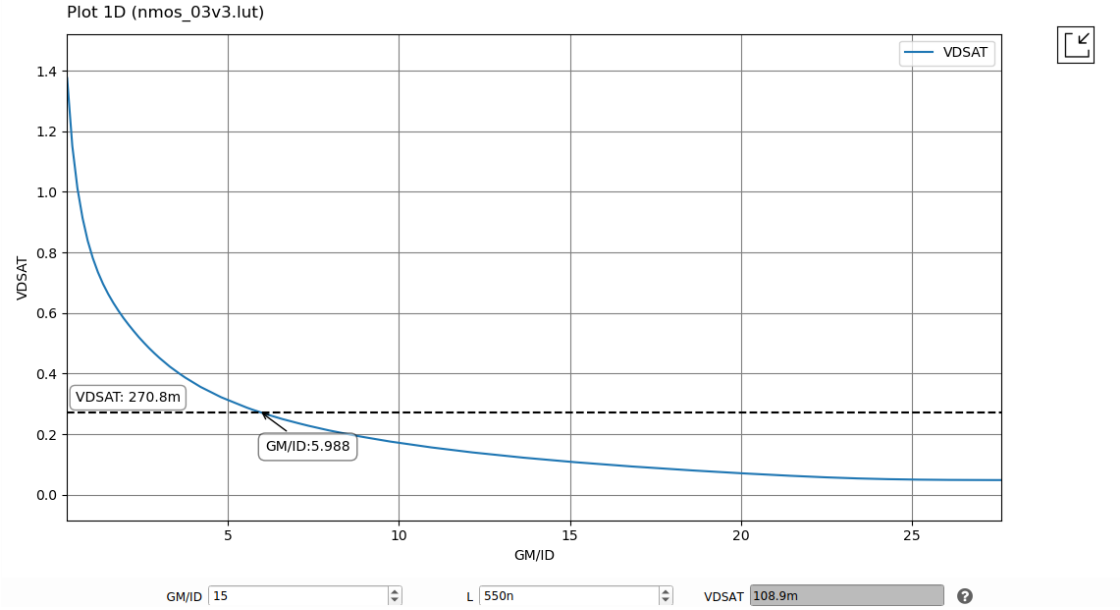
1. Avd = 50 from the given.
2. Avcm = 9.96*10-3 = 1/2*Rss*gm5,6 = 1/(2*Rss*(220*10^-6)) .
3. the value of Rss=228185.4691=1/gds Then gds < 4.38*10-6 S
4. Let's assume gm/id=15 Then gm/gds > 136.9



gm/gds vs gm/id

L = 0.55 um

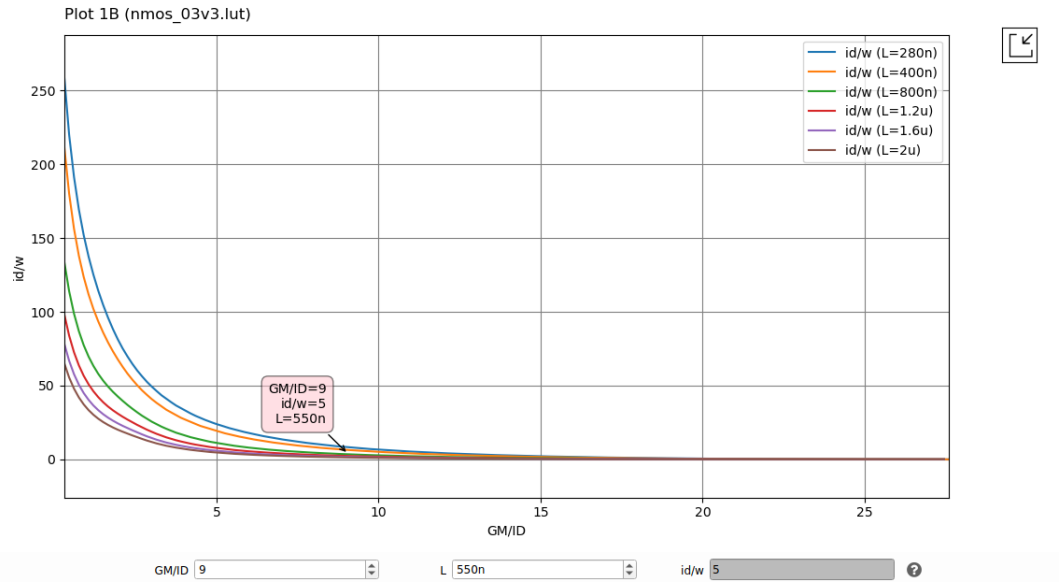
By applying KVL: 1>Vgs3,4 + vdsat→ vdsat<0.2708



vdsat vs gm/id

By plotting vdsat vs gm/id ,we get gm/id = 6, let's take some margin so, proper value of **gm/id= 9**

By plotting id/w vs gm/id we get value of W



Id/w vs gm/id

W = 8 um

Now We Have Finished our specs for each part, let's do summary chart for specs.

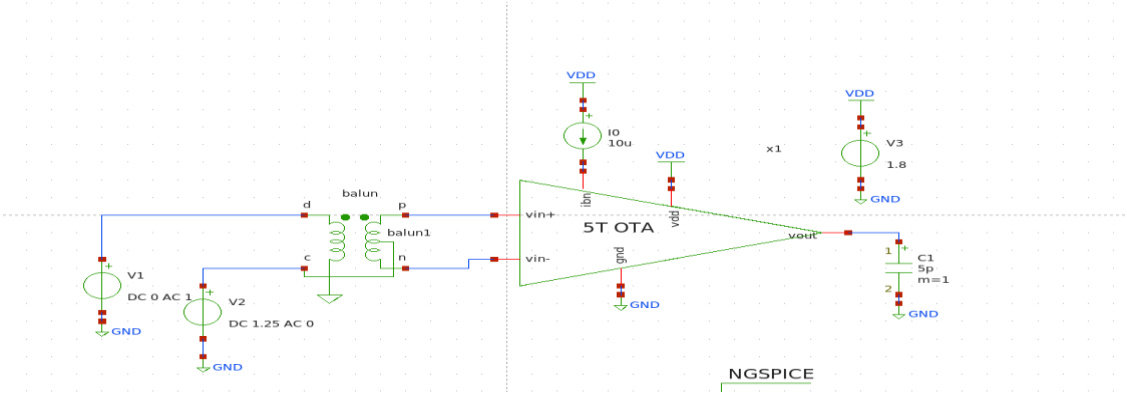
4. OTA Devices Sizing

Param	M3,4(Input pair)	M1(CM TAIL)	M5,6(CM LOAD)
W	17.42 µm	8 µm	16.13 µm
L	0.45 µm	0.55 µm	0.4 µm
g_m	320 µs	360 µs	220 µs
I_d	20 µA	40 µA	20 µA
g_m/I_D	16	9	11
V_{GS}	729 mV	870.7 mV	911.9 mV
V_{Dsat}	99.85 mV	190.6 mV	161.2 mV
V_{ov}	25.3 mV	164.2 mV	135 mV
V_*	126.4 mV	223.8 mV	184.5 mV

OTA Devices Sizing

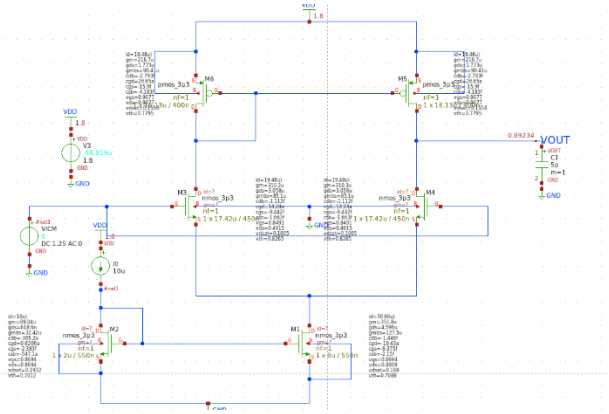
Part 3: Open-loop OTA simulation

1. OP simulation



Open-loop testbench

2) DC OP For Each Transistor



Schematic

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm6.m0	m.x1.xm5.m0	m.x1.xm4.m0
model	pmos_3p3.12	pmos_3p3.12	nmos_3p3.12
id	1.94943e-05	1.94943e-05	1.94946e-05
gm	0.00021884	0.00021884	0.000321042
gmbs	9.04565e-05	9.04565e-05	8.77743e-05
gds	1.7743e-06	1.7743e-06	3.15388e-06
vgs	0.907724	0.907724	0.84251
vth	0.779516	0.779516	0.828319
vds	0.907723	0.907723	0.484783
vdsat	0.155492	0.155492	0.0961079

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm3.m0	m.x1.xm1.m0	m.x1.xm2.m0
model	nmos_3p3.12	nmos_3p3.9	nmos_3p3.9
id	1.94946e-05	3.89887e-05	1e-05
gm	0.000321042	0.000352132	8.90372e-05
gmbs	8.77743e-05	0.000127629	3.24216e-05
gds	3.15388e-06	4.48154e-06	6.18586e-07
vgs	0.84251	0.86944	0.86944
vth	0.828319	0.708842	0.701212
vds	0.484783	0.407477	0.869433
vdsat	0.0961079	0.188044	0.193168

DC OP parameters

```
vout = 8.923424e-01
```

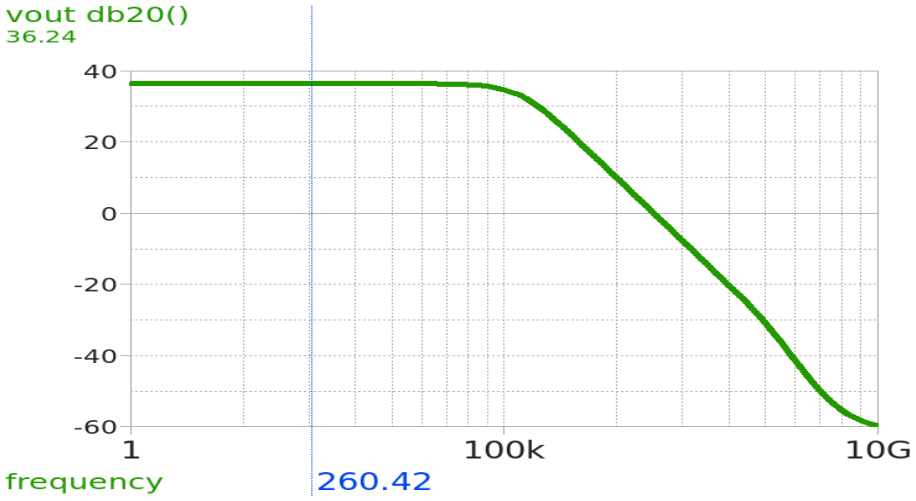
Vout

Comments on OP:

Comment:

- The current and gm in the input pair are exactly equal.
- $V_{out} = V_{DD} - V_{DS5} = V_{DD} - V_{GS6} = 0.892\ V$ because the current in both Transistors are equal because no mismatch.

2. Diff small signal ccs



diff gain bode plot (magnitude)

```
gain                =  6.487973e+01 at=  1.000000e+00
bw                  =  1.548170e+05
gbw = 1.004449e+07
```

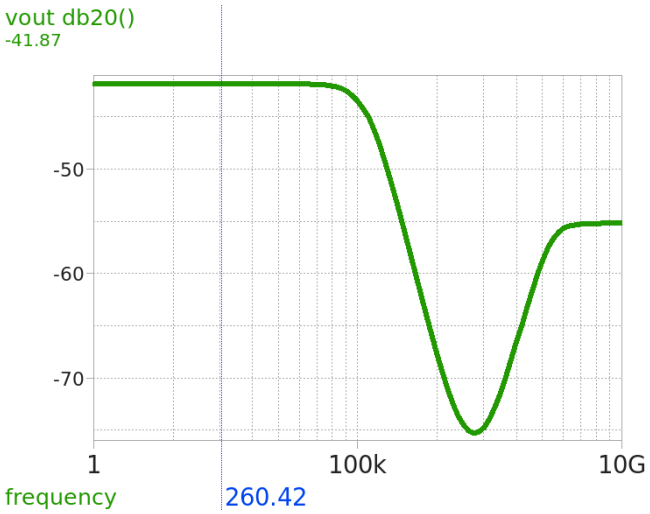
diff small signal results

$$diff\ gain = \text{gm3,4(ro5,6//ro3,4)}, BW = \frac{1}{2\pi \text{Rout} * \text{CL}}, GBW = \frac{g_{m3,4}}{2\pi \text{CL}}$$

Spec	*Simulation*	*Hand analysis*
DC diff gain	36.24 *dB*	36.27 *dB*
BW	154.81 *KHz*	156.86 *KHz*
GBW	10.04 *MHz*	10.2 *MHz*

simulation vs hand analysis

3. CM small signal ccs



CM gain bode plot (magnitude)

```
cmgain                =  7.871319e-03 at=  1.000000e+00
```

CM gain Results

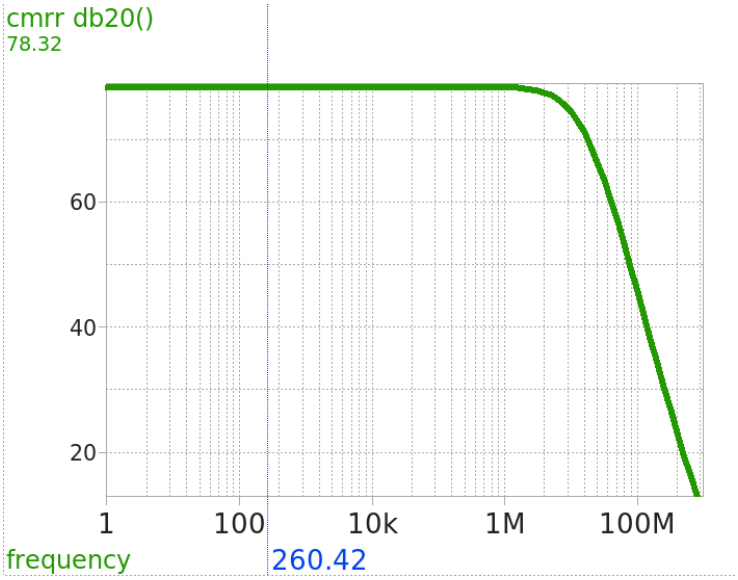
calculation of DC CM gain with hand analysis:

$$Avcm = \frac{1}{2gm5,6 * ro1} = -40.81dB$$

Spec	*Simulation*	*Hand analysis*
DC CM gain	$-41.87\ dB$	$-40.81\ dB$

simulation vs hand analysis

4. CMRR



CMRR bode plot (magnitude)

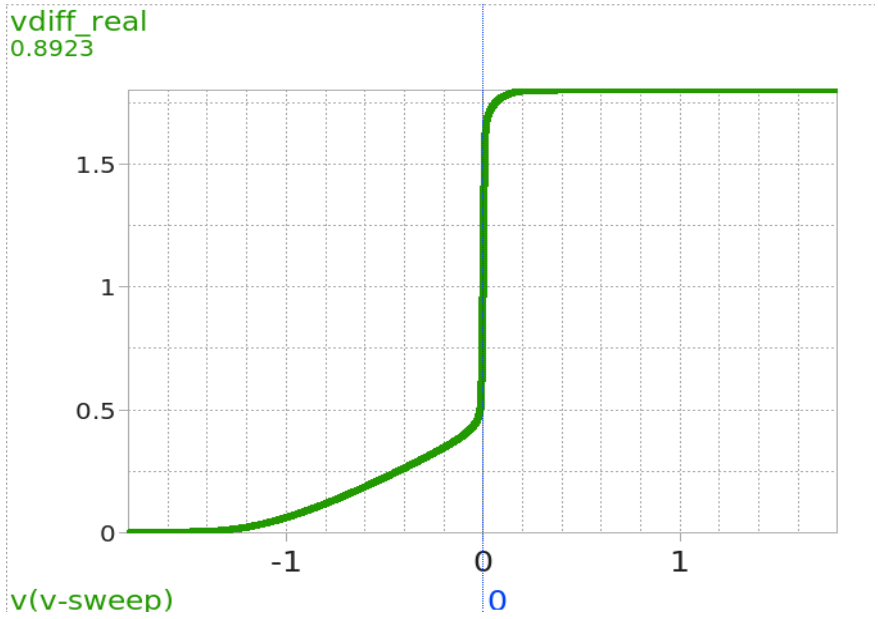
calculation of CMRR with hand analysis:

CM Gain=$\frac{1}{2*gm5*ro1}$, Diff Gain=$\frac{gm3*ro5*ro3}{ro5+ro3}$, CMRR=$\frac{Avd}{Acm}$ = 7152.5

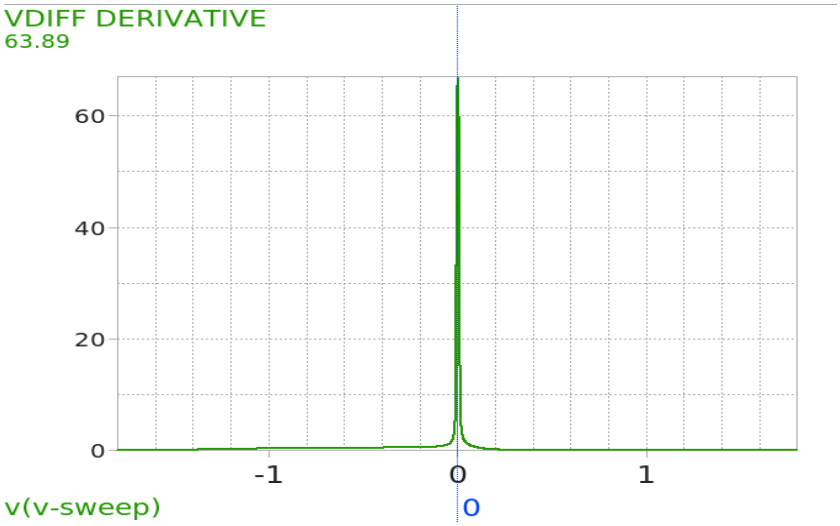
Spec	*Simulation*	*Hand analysis*
CMRR	78.6 dB	$A_{vd} - A_{vCM} = 77.09dB$

simulation vs hand analysis

5. Diff large signal ccs



Vout vs VID



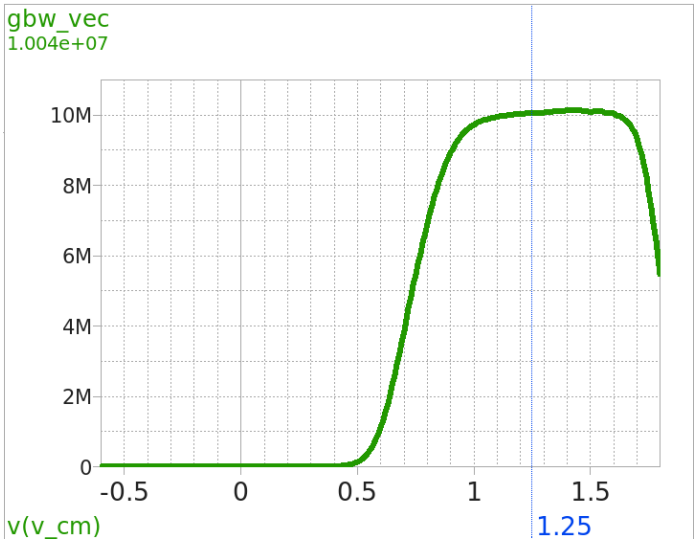
derivative(Vout) vs VID

Comments on Diff large signal:

Comment:

- The value of Vout @ (VID = 0) = 0.8923 , Because at Vid = 0, the currents in both branches are equal, since there is no mismatch or differential input and all four transistors operate in saturation with approximately equal ro values. As a result, a voltage divider is formed through these equal resistances, producing a supply voltage equal to VDD.
- $simulation\ A_{vd} = 64.87, peak = 63.89$ they are the same.

6. CM large signal ccs (GBW vs VICM)



GBW vs VICM

```
vcm_min = 9.200000e-01
vcm_max = 1.720000e+00
```

CMIR

calculation of CM input range (CMIR)with hand analysis:

$$V_{GS3,4} + V_{DSsat1} < \text{VICMR} < VDD - V_{GS5,6} - V_{DSsat3,4} + V_{GS3,4}$$

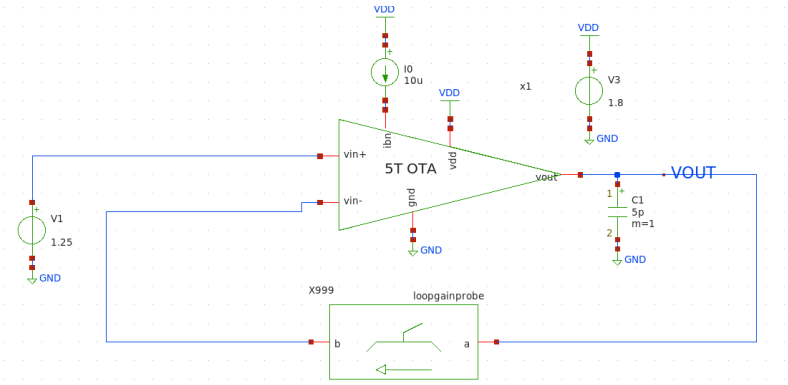
$$1 \quad < \text{VICMR} < \quad 1.64$$

Spec	Analytical	Simulation
$\boldsymbol{Vcm\ max}$	1.64	1.72
$\boldsymbol{Vcm\ min}$	1	0.92

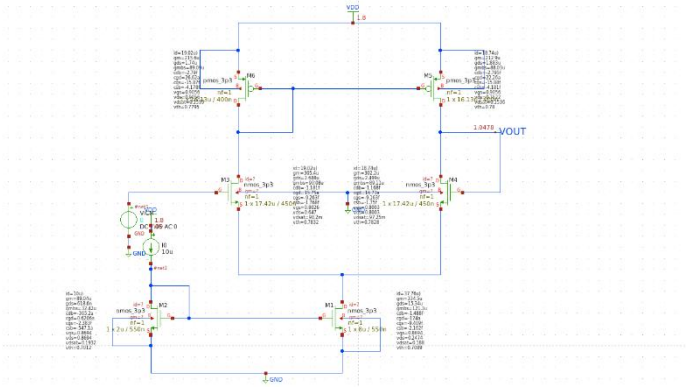
Part 4: Closed-Loop OTA Simulation

1. OP simulation

1) Schematic of the OTA



2) DC OP For Each Transistor



Schematic

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model	pmos_3p3.12	pmos_3p3.12	nmos_3p3.12
id	1.82861e-05	1.81641e-05	1.81641e-05
gm	0.000210397	0.000209201	0.00030474
gmbs	8.69514e-05	8.64814e-05	9.23255e-05
gds	1.68567e-06	1.74376e-06	2.53333e-06
vgs	0.902139	0.902139	0.774434
vth	0.779532	0.779734	0.767329
vds	0.902138	0.830995	0.774433
vdsat	0.151361	0.151213	0.0918029

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm3.m0	m.x1.xm1.m0	m.x1.xm2.m0
model	nmos_3p3.12	nmos_3p3.9	nmos_3p3.9
id	1.82861e-05	3.64502e-05	1e-05
gm	0.000306293	0.000309144	8.90372e-05
gmbs	9.28024e-05	0.000112406	3.24216e-05
gds	2.61338e-06	3.89723e-05	6.18586e-07
vgs	0.775432	0.86944	0.86944
vth	0.767504	0.708974	0.701212
vds	0.70329	0.194555	0.869433
vdsat	0.0922059	0.187947	0.193168

DC OP parameters

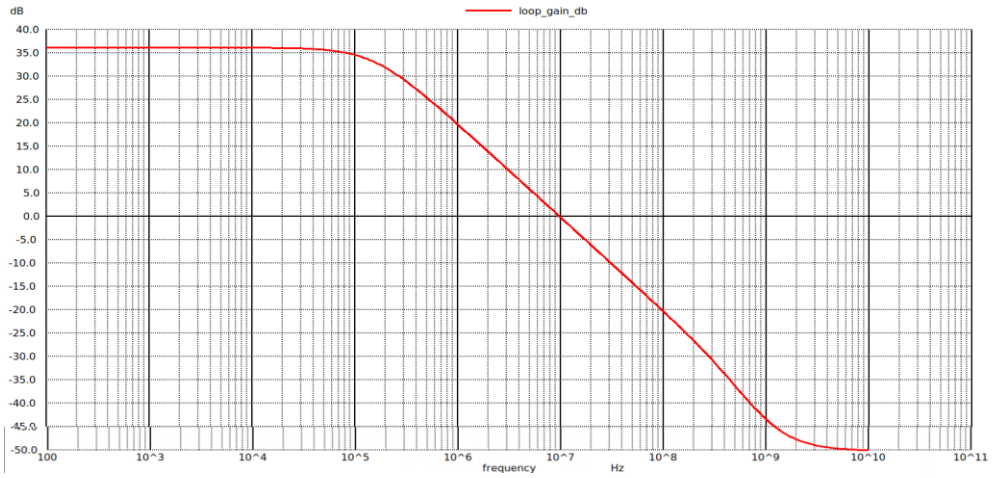
Comments on OP simulation:

Comment:

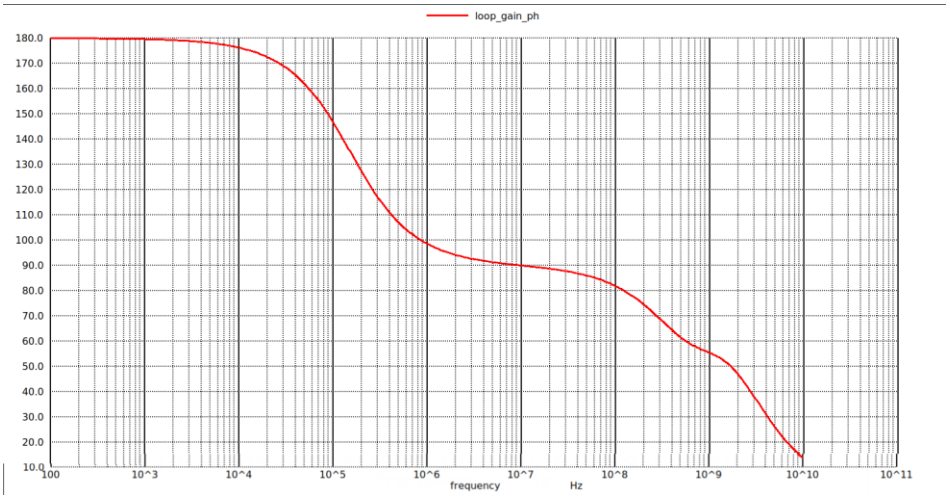
- the current and gm in the input pair is not exactly equal, that's because Negative feedback circuits inherently exhibit static gain error, which leads to mismatch in the input pair.

- $\boldsymbol{\Delta}gm1$=306.29u−304.74u=1.55uS, Mismatch = 0.5%
- $\boldsymbol{\Delta ID}$1=18.28u−18.16u=0.12uA, Mismatch = 0.65%

2. Loop Gain



loop gain bode plot (magnitude)



loop gain bode plot (phase)

```
gain               =  6.461535e+01 at=  1.000000e+02
bw                 =  1.538918e+05
gbw = 9.943773e+06
gain_crossover_freq =  9.937795e+06
phaseatzerogain    =  9.001850e+01
pm = 8.998150e+01
```

- ## Compare Between Loop Gain and Open Loop:

	OPEN LOOP	LOOP GAIN
Av	36.24dB	36.24dB
GBW	10M	9.94M

Comments on Compare Between Loop Gain and Open Loop:

Comment:

- Gain is **Equal** because **Beta** is approximately Equal to 1. But **GBW** in Loop Gain is **lower** due to:

  1. **Parasitic capacitances** and **resistances** in the circuit introduce additional poles and zeros, which reduce the high-frequency response and lower the measured **GBW** in loop gain.
  2. $GBW_{loop} \approx \beta \cdot GBW_{open\text{-}loop}$, since the feedback factor β is not exactly ideal and slightly less than 1, the loop gain is proportionally reduced, leading to a slightly lower **GBW** compared to the open-loop case.

- ## Hand analysis results

Avd = $gm(ro5 /\!/ ro3)$ = 65.1 = 36.27 dB, ***BW*** = $\frac{1}{2\pi Rout * CL}$ = 156.86 KHz
GBW = $Avd * BW$ = 10.02MHz, **AoL** = 65.1, **LG** = β AoL, β = 1 ∴***LG*** = 65.1= 36.27 dB
Acl= $\frac{AoL}{1+\beta AoL}$ = 0.984, **PM**=90°, because we have one dominant pole.

	Simulation	Hand Analysis
AoL	36.24dB	36.27dB
BW	153.8k	156.86k
GBW	10M	10.02M
LG	36.24dB	36.27dB
PM	90°	90°
Avcl	0.984	0.984

3. Specs Achieved

Technology	Specs	Achieved
open loop DC Voltage gain	>=34dB	36.24 dB
CMRR	>=74dB	≈ 78.32dB
Phase margin	>=70°	90°
CM input range-low	<=1v	0.92 v
CM input range-high	>=1.5v	1.72 v
GBW	>=10MHz	10.04 MHz