وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Cadence and Master Micro Tools
Lab 07
gm/ID Design Methodology

Intended Learning Objectives

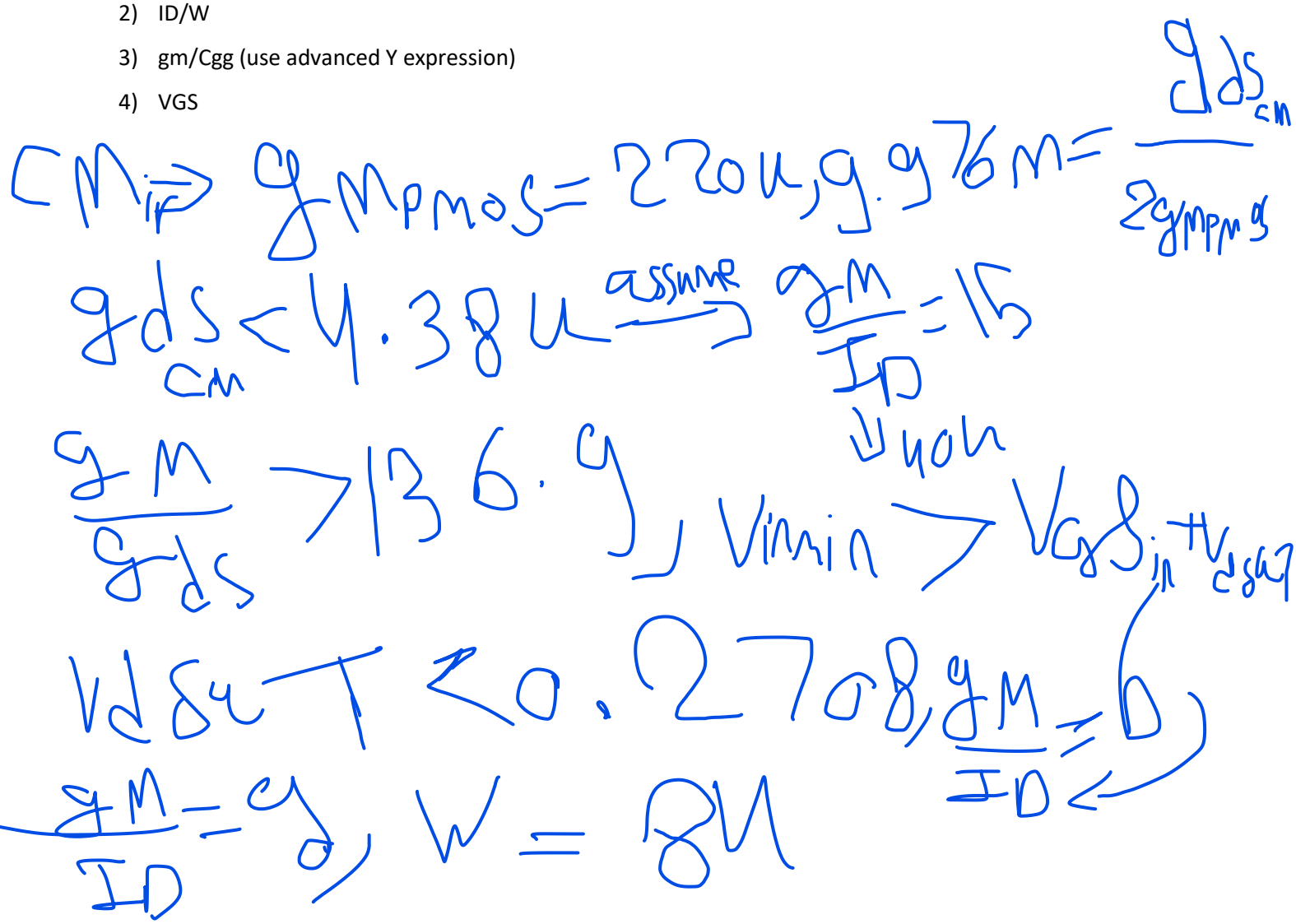
In this lab you will:

- Design and simulate a 5T OTA.
- Learn how to plot and use the gm/ID design charts.
- Learn how to simulate the open-loop characteristics of the 5T OTA.
- Learn how to simulate the closed-loop characteristics of the 5T OTA.

Part 1: gm/ID Design Charts

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.28u, 0.4u:0.4u:2u

1) gm/gds
2) ID/W
3) gm/Cgg (use advanced Y expression)
4) VGS



Part 2: OTA Design

Use the gm/ID methodology to design a diff input single-ended (SE) output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

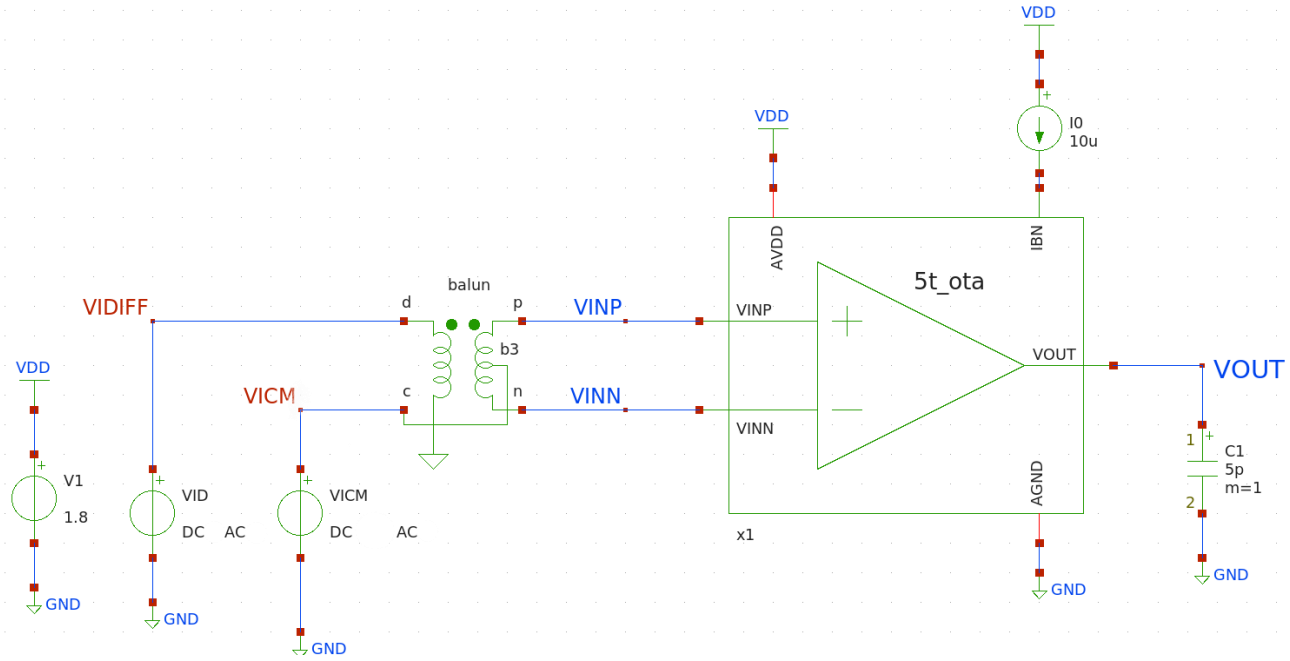
Technology	0.18um CMOS
Supply voltage	1.8V
Load	5pF
Open loop DC voltage gain	>= 34dB
CMRR @ DC[1]	>= 74dB
Phase margin	>= 70°
CM input range – low	<= 1V
CM input range – high	>= 1.5V
GBW	>= 10MHz

Report the following:

1) Detailed design procedure and hand analysis. You need to explain why you chose the architecture that you implemented.
2) Use the Sizing Assistant (SA) or the design charts in ADT to size the transistors.
3) A table showing W, L, g_m, I_D, g_m/I_D, V_{DSsat}, $V_{ov} = V_{GS} - V_{TH}$, and $V^* = 2I_D/g_m$ of all transistors (as calculated from gm/ID curves).

[1] CMRR is gm/gds higher than Avdc. CMRR = Avdc + 40dB means gm/gds = 100 which is quite reasonable.

Part 3: Open-Loop OTA Simulation[2]



Create a testbench for the OTA as shown above.

NOTE: The IB connection (sinking or sourcing) in the test bench may differ from the one shown above, depending on the type of your input pair (PMOS/NMOS).

Report the following:

1) Schematic of the OTA with DC node voltages clearly annotated.
   - Use VICM at the middle of the CMIR.
   - Is the current (and gm) in the input pair **exactly** equal?
   - What is DC voltage at VOUT? Why?

   ➔ Note: The code below shows how to save the OP parameters of every transistor in a loop, courtesy of Eng. Sheriff Shamardn and Eng. Youssef Wael. You just need to number your transistors as M1, M2, … and set the x stop value in the loop according to your design.

```
save all
dowhile x <= 5
save @m.xm{$num}.m0[id]
save @m.xm{$num}.m0[vgs]
save @m.xm{$num}.m0[vds]
```

[2] An OTA can be simulated without closing the loop if it is perfectly matched (zero offset voltage). For this 5T OTA in open loop, the output node DC level will follow the diode connected node. For two-stage OTA, the systematic offset voltage may drive the output to one of the rails. Also, when simulating mismatch (Monte Carlo simulation), open-loop simulation cannot be used. You must close the loop in the cases of random and systematic offset, so that the offset voltage is automatically adjusted by the feedback action and the dc bias is correctly set.

```
save @m.xm{$num}.m0[vdsat]
save @m.xm{$num}.m0[vth]
save @m.xm{$num}.m0[gm]
save @m.xm{$num}.m0[gds]
save @m.xm{$num}.m0[gmbs]
save @m.xm{$num}.m0[cgs]
save @m.xm{$num}.m0[cgd]
save @m.xm{$num}.m0[csb]
save @m.xm{$num}.m0[cdb]
let x = x + 1
set num = {$&x}
end
op
write 5t_ota_tb_op.raw
echo \"       === Calculated Parameters ===\"
let x = 1
dowhile x <= 6
 set num = {$&x}
 let gmid = @m.x1.xm{$num}.m0[gm]/@m.x1.xm{$num}.m0[id]
 let Vstar = 2/gmid
 let ro = 1/@m.x1.xm{$num}.m0[gds]
 echo \"M{$num}: gm/id = $&gmid S/A, Vstar = $&Vstar V, ro = $&ro ohms\"
 let x = x + 1
end
.endc
```

➔ Hint: An alternative way is to print the OP parameters of all transistors in ngspice terminal (save command is NOT required). Example (you can add additional OP parameters):

```
show m : id : gm : gds : gmbs: vgs : vth : vds
```

2) Diff small signal ccs:
   - Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use VICM in the middle of the CMIR.
   - Plot diff gain (in dB) vs frequency.
   - Compare simulation results with hand calculations in a table.
3) CM small signal ccs:

- Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- Set VICMAC = 1 and VIDAC = 0.
- Use VICM in the middle of the CMIR.
- Plot CM gain in dB vs frequency.
- Compare simulation results with hand calculations in a table.

4) CMRR:

➔ NGspice Hint: To run two AC analyses and alter VIDAC and VICMAC during simulation, and get access to each simulation data, use ac(simulation_number).v(node_name) courtesy of Eng. Youssef Wael.

```
.control
save all

* === DIFFERENTIAL MODE ===
alter VID AC = 1
alter VICM AC = 0
ac dec 10 1 10g

* === COMMON MODE ===
alter VID AC = 0
alter VICM AC = 1
ac dec 10 1 10g

* === EXTRACT RESULTS ===
let vod = ac1.v(VOUT)
let vocm = ac2.v(VOUT)
let cmrr_freq = vdb(vod) - vdb(vocm)
write 5t_ota_tb_ac.raw
.endc
```

- Use VICM at the middle of the CMIR.
- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.
- Compare simulation results with hand calculations in a table.

5) Diff large signal ccs:

- Use VICM at the middle of the CMIR.
- Use DC sweep (**not parametric sweep**) VID = -VDD:1m:VDD. You must use a small step (1mV) because the gain region is very small (steep slope).
- Plot VOUT vs VID.

- From the plot, what is the value of Vout at VID = 0? Why?
- Plot the derivative of VOUT vs VID. Compare the peak with Avd.

6) CM large signal ccs (GBW vs VICM):
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use **parametric** sweep (**not DC sweep**) VICM = 0:10m:VDD.
   - Plot GBW vs VICM.
   - Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW[3].

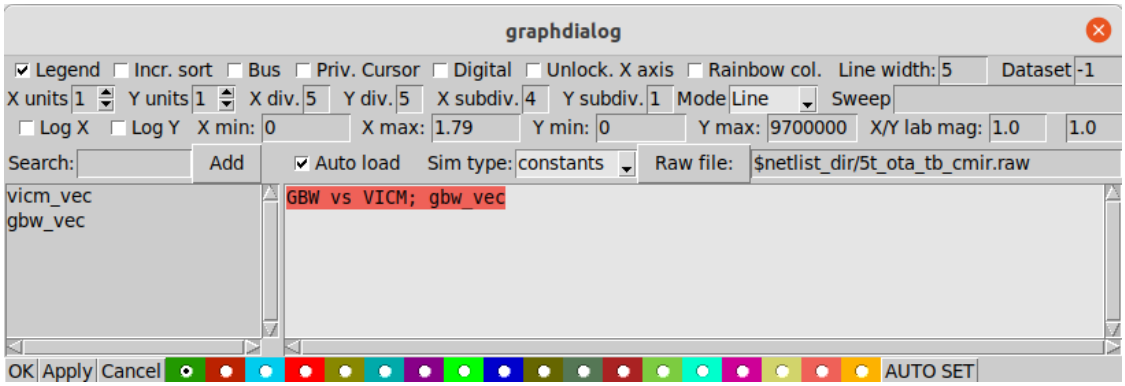
➔ NGspice Hint: To save the GBW values from each parametric sweep, define a vector and fill the vector with the GBW values each iteration. To define a VICM or GBW as a voltage or frequency vector, use the settype command. Example

```
.control
save all
* === DIFFERENTIAL GAIN vs VICM SWEEP ===
let vicm_start = 0
let vicm_stop = 1.8
let vicm_step = 20m
let num_points = (vicm_stop - vicm_start) / vicm_step

* Pre-allocate vectors
let vicm_vec = vector(num_points) *0
let gbw_vec = vector(num_points) *0

* Define vectors type
settype voltage vicm_vec
setscale vicm_vec
settype frequency gbw_vec

let vicm_val = vicm_start
let i = 0

while vicm_val le vicm_stop
  * Set CM voltage and enable differential input
  alter VICM DC = vicm_val

  * AC to get DC gain and BW
  ac DEC 10 1 10G
  meas AC gain MAX vmag(VOUT)
  let stop_band=gain*0.707
```

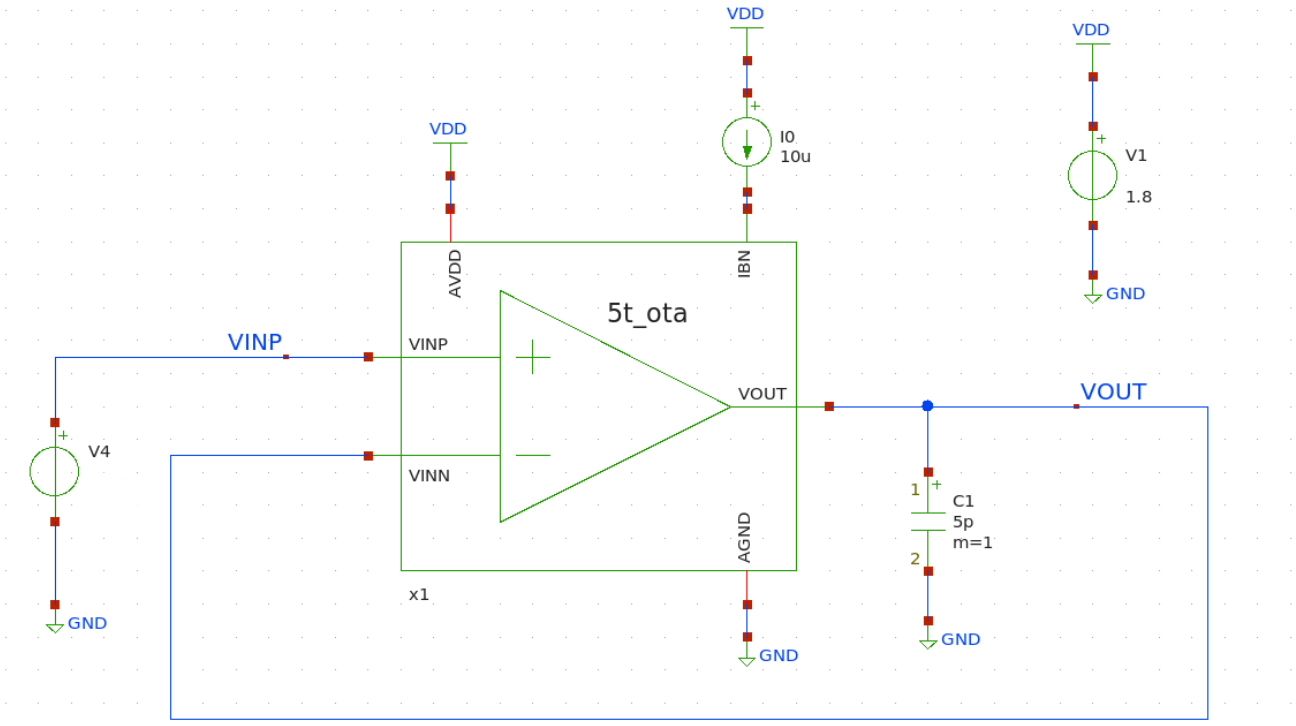
[3] If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).

```
  meas AC bw WHEN vmag(VOUT)=stop_band

  * Store results in pre-allocated vectors
  let vicm_vec[i] = vicm_val
  let gbw_vec[i] = gain * bw

  let vicm_val = vicm_val + vicm_step
  let i = i + 1
end

* === MEASUREMENTS ===
meas AC max_gbw max f(gbw_vec)
let limit_gbw = 0.9*max_gbw
meas AC min_vincm find v(vicm_vec) when f(gbw_vec)=limit_gbw RISE=1
meas AC max_vincm find v(vicm_vec) when f(gbw_vec)=limit_gbw FALL=1
let CMIR=max_vincm-min_vincm

print min_vincm max_vincm CMIR
write 5t_ota_tb_cmir.raw gbw_vec
.endc
```

➔ Xschem Hint: To access these vectors in the waveform viewer, change Sim type to constant and load the Raw file



PART 4: Closed-Loop OTA Simulation

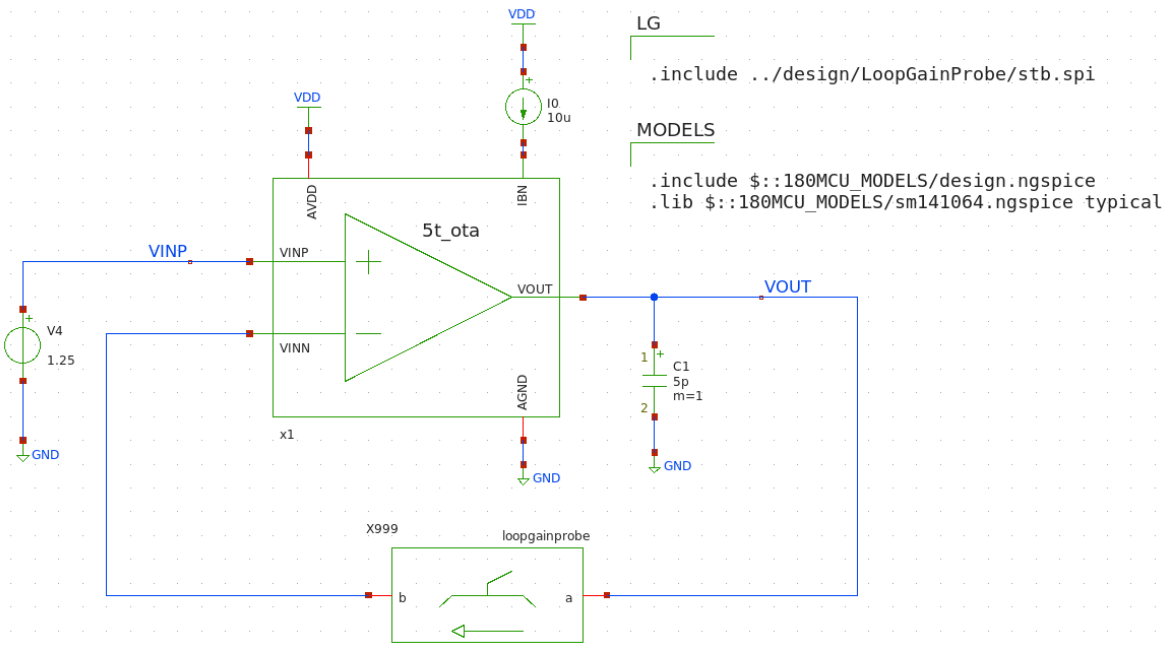


Create a testbench as shown above. Report the following:

1) Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration. Use VIN = CMIR-low + 50mV.
   - Is the current (and gm) in the input pair exactly equal[4]? Why?
   - Calculate the mismatch in I_D and gm.

[4] For the case of the OTA in closed-loop unity-gain buffer connection, the output will follow the input. The output voltage deviates from its CM level (the voltage at the mirror node for the 5T OTA) in order to match the input voltage. Since the gain is finite, there will be a non-zero differential input voltage that will cause an imbalance between the two sides of the differential pair. This imbalance behaves exactly like mismatch. To avoid this imbalance, we may close the loop using Vin equal to the voltage at the mirror node. Any other Vin will introduce mismatch between the gm's of the input pair, and you will have to use Avcm and CMRR equations that consider mismatch.

2) Loop gain:



➔ Xschem Hint: To add loopgainprobe

1- Download the following folder to your machine into the same folder as your schematic.

https://drive.google.com/file/d/1iPvl3exgq31yQiewNZOAw1eGU9cuFpbV/view?usp=sharing

2- Press "Shift + I" → current dir → LoopGainProbe→ loopgainprobe.sym

- Use VICM in the middle of the CMIR.
- Plot loop gain in dB and phase vs frequency.

➔ NGspice Hint: The code exists inside the folder itself to access it adjust the directory with an include command. Example (Adjust according to your directory)

.include LoopGainProbe/stb.spi

- Compare DC gain and GBW with those obtained from open-loop simulation. Comment
- Compare simulation results with hand calculations in a table.

Lab Summary

- In Part 1 you learned:
  - How to plot and use the gm/ID design curves.
- In Part 2 you learned:
  - How to design and OTA that meets desired specifications.
- In Part 3 you learned:
  - How to simulate the small-signal differential gain of a 5T OTA in open-loop configuration.
  - How to simulate the small-signal common-mode gain of a 5T OTA in open-loop configuration.
  - How to simulate the large-signal differential characteristics of a 5T OTA in open-loop configuration.
  - How to simulate the large-signal common-mode characteristics of a 5T OTA in open-loop configuration.

- In Part 4 you learned:
    - How to simulate the small-signal differential gain of a 5T OTA in closed-loop configuration.
    - How to simulate the small-signal common-mode gain of a 5T OTA in closed-loop configuration.
    - How to simulate the large-signal differential characteristics of a 5T OTA in closed-loop configuration.
    - How to simulate the large-signal common-mode characteristics of a 5T OTA in closed-loop configuration.

Acknowledgements

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