Department of Electronics and Electrical Communications

Faculty of Engineering-Cairo University

Electronics Project

PRESENTED TO: ENG. MOUSTAFA RADY

Name	Sec.	B.N.	ID
محمد جبر عبدالمنعم محمد نافع	3	40	9230752
امير اشرف لولى عباس	1	36	9230242
رؤى عبدالعظيم احمد عبدالعظيم محمد	2	10	9230366
محمد نصر حسن على	4	9	9230816
نورالدين محمد محمد عبدالمناف	4	28	9230962
هدى ايهاب السيد ابراهيم	4	33	9230974

Table of Contents

Table of Figures

Q1

In this part of the project, a CMOS amplifier is designed using $65nm$ TSMC technology to meet specific performance requirements. The amplifier must achieve a minimum open-loop gain of $80\ dB$ and an open-loop bandwidth of $1\ MHz$ while driving a $500\ fF$ load capacitance. Special attention is given to optimizing the total current consumption and silicon area to ensure an efficient design.

The design process includes transistor sizing, biasing, and verification of proper operation through simulation. Key performance metrics such as open-loop gain and power dissipation are evaluated. In addition, the operating points of all transistors are extracted, including $V_{gs}, V_{ds}, V_{th}, I_D, g_m, and\ r_o$, to ensure that each device operates in the intended region.

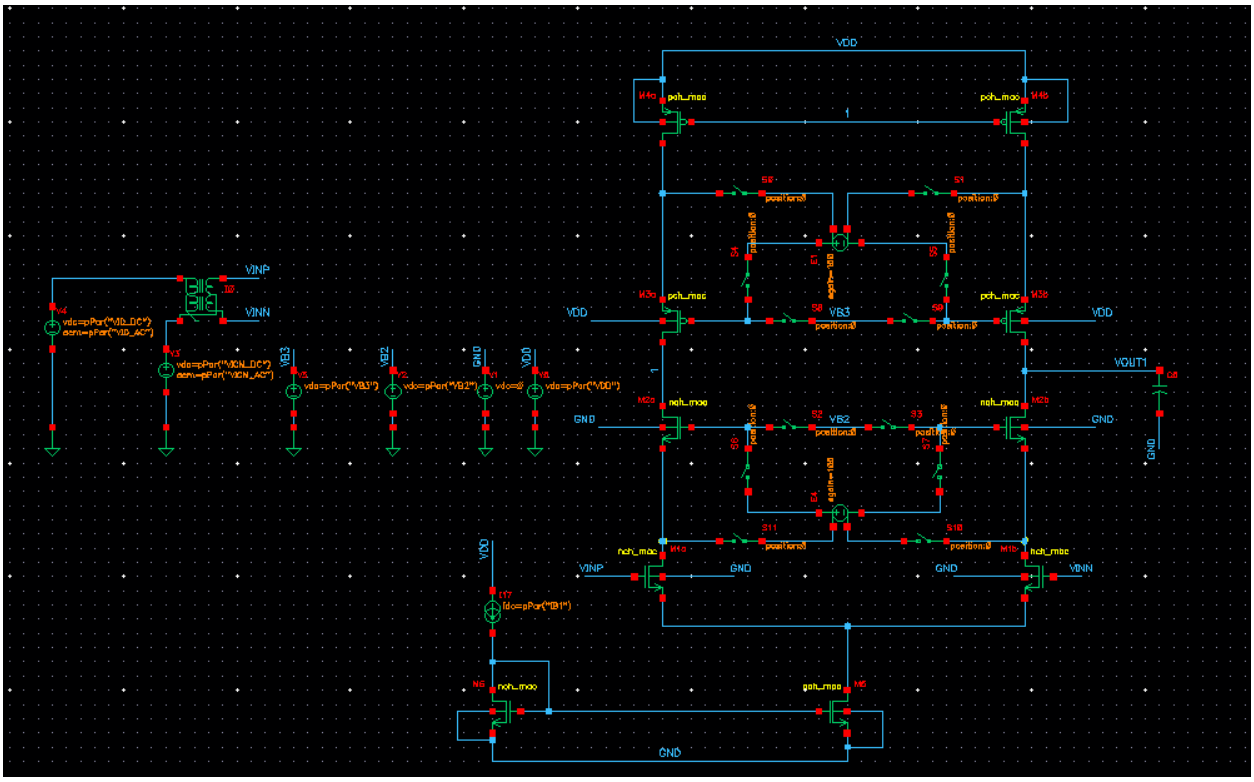


Figure 1: Main schematic

Input pair : (M1a and M1b)

Cascode NMOS : (M2a and M2b)

Cascode PMOS : (M3a and M3b)

Active load : (M4a and M4b)

Current source : (M5)

I-V transistor : (M6)

Telescopic gain boosting amplifier design

We use current equal $5.5mA$ for one branch in our design

Input pair

For input pair transistors we use short length ($L = 0.1\mu m$), and a large efficiency ($\frac{g_m}{I_D} = 16$) as we need a high g_m from input pair because it contribute in G_m calculations for gain. This give us a good GBW also.

$$\because \frac{g_m}{I_D} = 16\,, \qquad \therefore V^* = \frac{2}{g_m/I_D} = \frac{2}{16} = 125mV$$

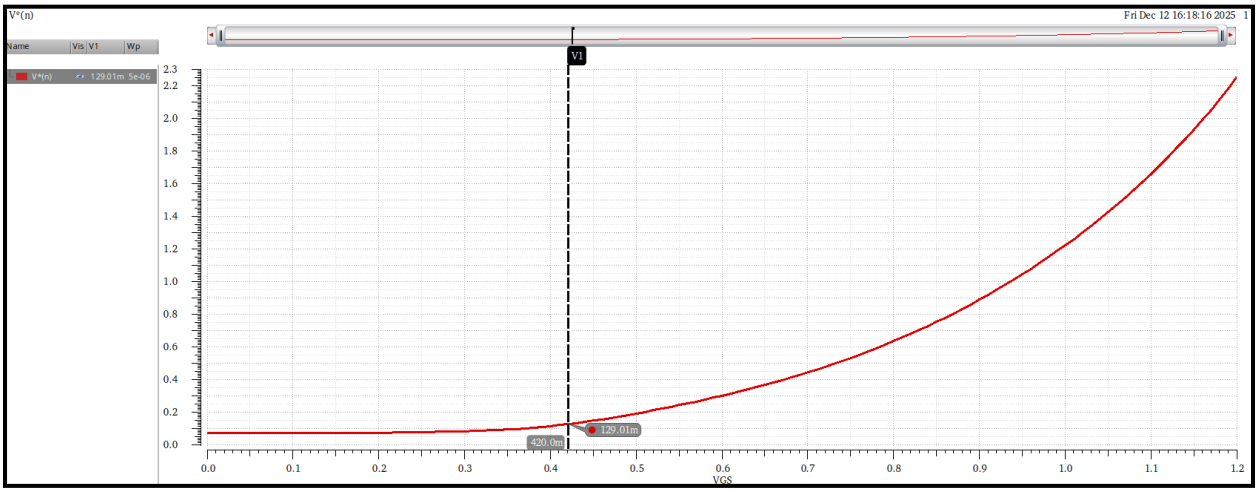


Figure 2: Vgs of input pair

$\therefore V_{gs} \approx 430mV$

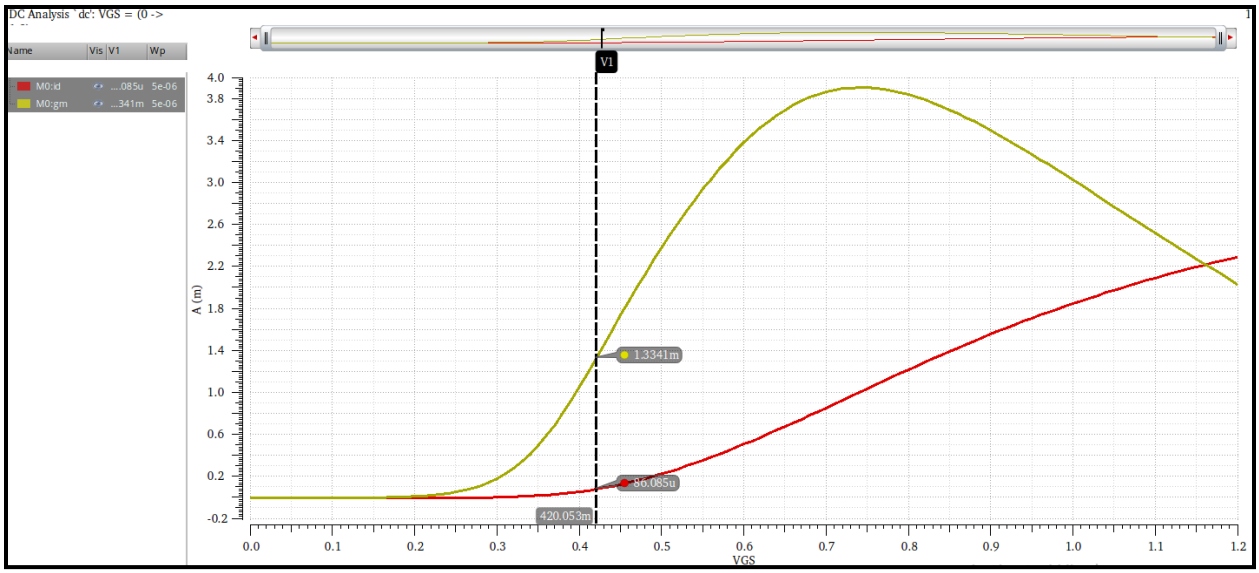


Figure 3: ID and gm of input pair

$\therefore I_D \approx 86\mu A\,,\quad g_m = 1.3341mS$

W	ID
5 μm	$I_D = 86\ \mu A$
??	$I_{DQ} = 5.5\ mA$

$$\therefore W = \frac{5 \times 5.5}{86} = 320\mu m$$

$\because g_m$ is also proportional to W (I_D) as long as V_{ov} is constant

$$\therefore g_m = \frac{1.3341 \times 5.5}{86} = 85.32mS$$

Cascode transistors

For cascode transistors we use short length ($L = 0.1\mu m$), and a moderate efficiency ($\frac{g_m}{I_D} = 14$) as we need a high g_m from cascade transistors because it contribute in R_{out} calculations for gain.

$$\because \frac{g_m}{I_D} = 14\,, \qquad \therefore V^* = \frac{2}{g_m/I_D} = \frac{2}{14} \approx 145mV$$

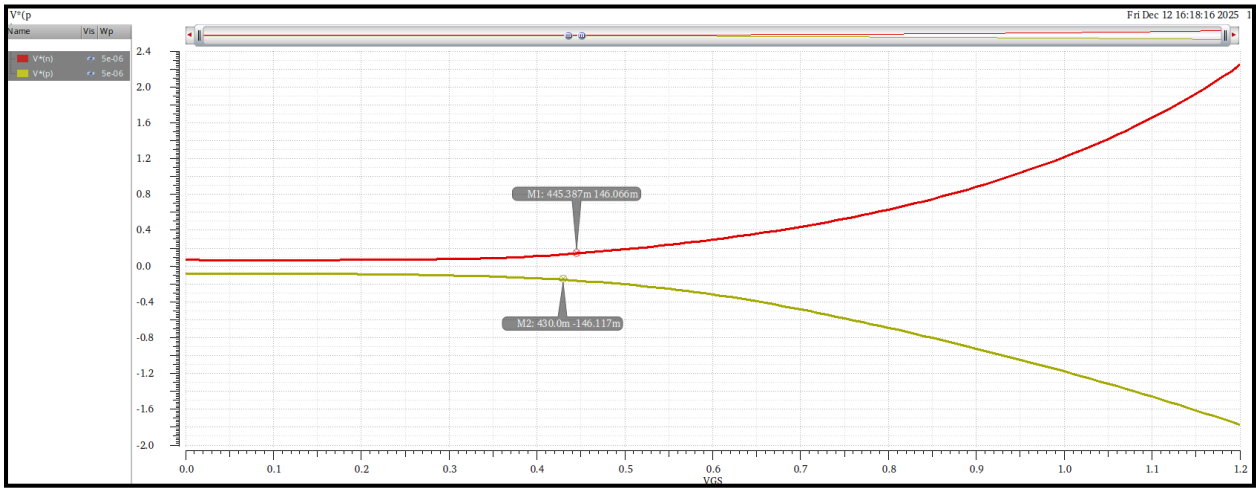


Figure 4: Vgs of cascn and cascp

$$\therefore V_{gs-cascn} \approx 445mV\,, \qquad V_{gs-cascp} \approx 430mV$$

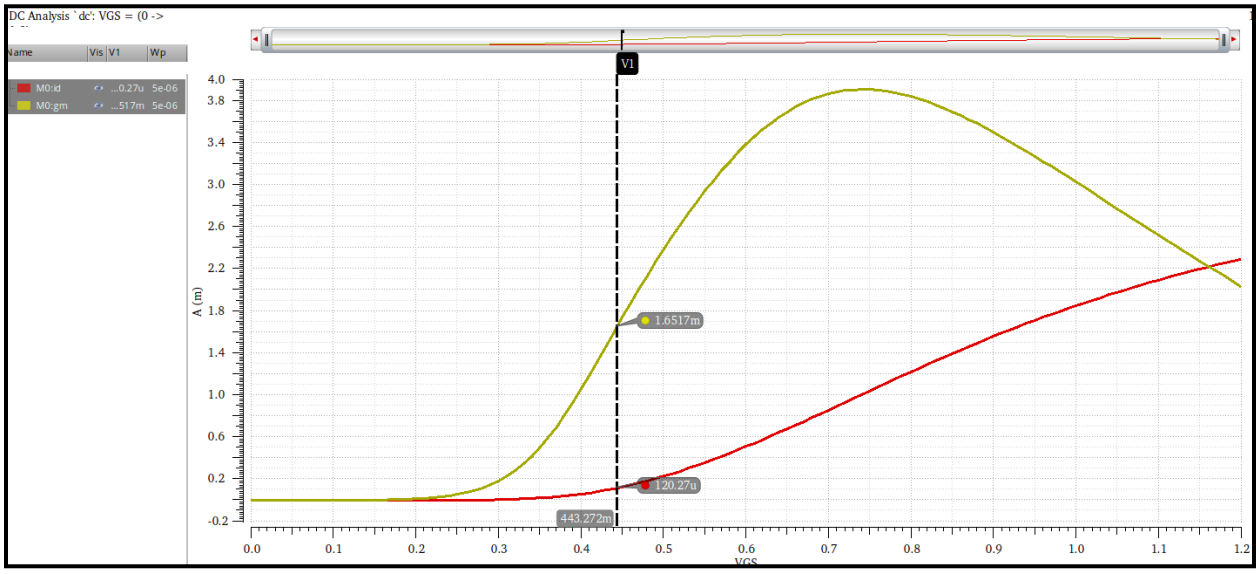


Figure 5: ID and gm for cascode NMOS

$$\therefore I_D \approx 120\mu A\,, \quad g_m = 1.6517mS$$

W	ID
5 μm	$I_D = 120\ \mu A$
??	$I_{DQ} = 5.5\ mA$

$\therefore W = \frac{5 \times 5.5}{120} \approx 230 \mu m$

$\because g_m$ is also proportional to W (I_D) as long as V_{ov} is constant

$\therefore g_m = \frac{1.6517 \times 5.5}{120} = 75.7 mS$

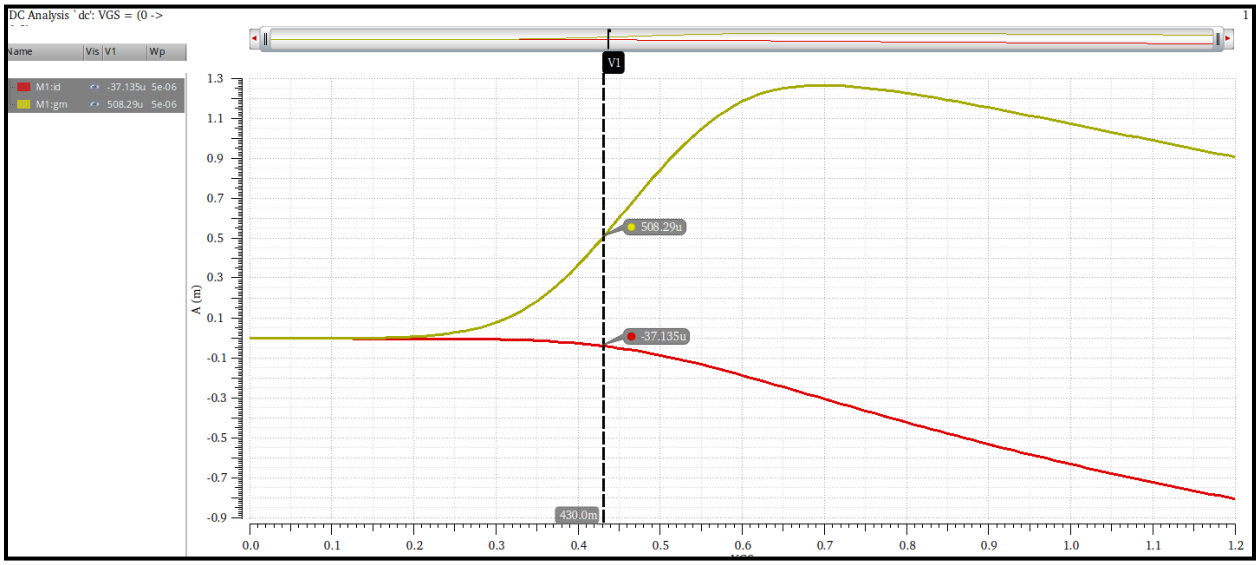


Figure 6: ID and gm for cascode PMOS

$\therefore I_D \approx 40 \mu A\ ,\quad g_m = 0.51 mS$

W	ID
5 μm	$I_D = 40\ \mu A$
??	$I_{DQ} = 5.5\ mA$

$\therefore W = \frac{5 \times 5.5}{40} \approx 688 \mu m$

$\because g_m$ is also proportional to W (I_D) as long as V_{ov} is constant

$\therefore g_m = \frac{0.51 \times 5.5}{40} = 70.1 mS$

Active load or current mirror

For input pair transistors we use short length ($L = 0.1\mu m$), and a moderate efficiency ($\frac{g_m}{I_D} = 12$) as we don't need a high g_m from current mirror because it doesn't contribute in calculations for gain. But his r_o contribute in gain through R_{out}.

$$\because \frac{g_m}{I_D} = 12\,, \qquad \therefore V^* = \frac{2}{g_m/I_D} = \frac{2}{12} \approx 165mV$$

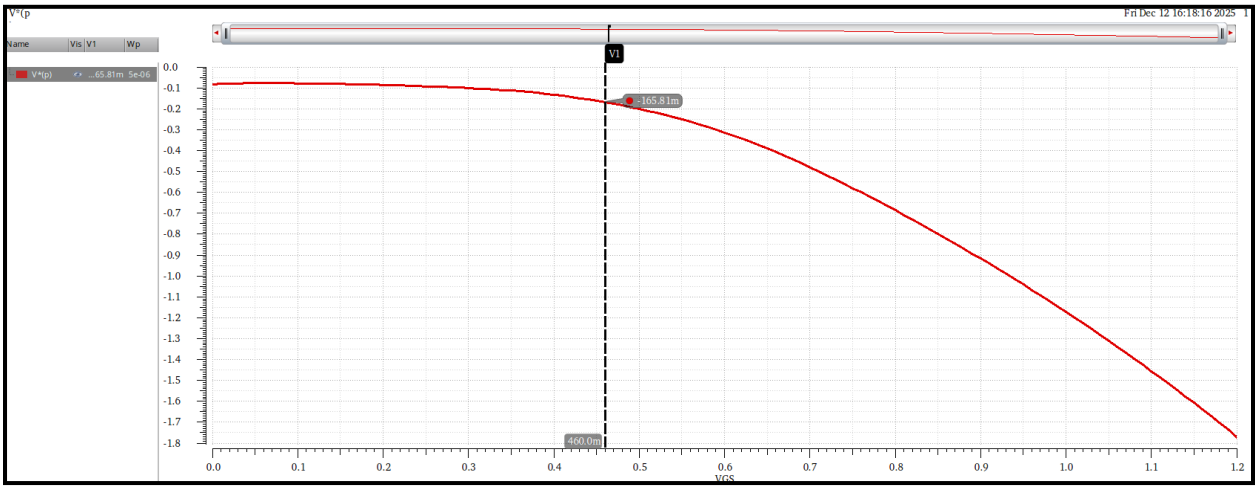


Figure 7: Vgs of active load

$\therefore V_{gs} \approx 460mV$

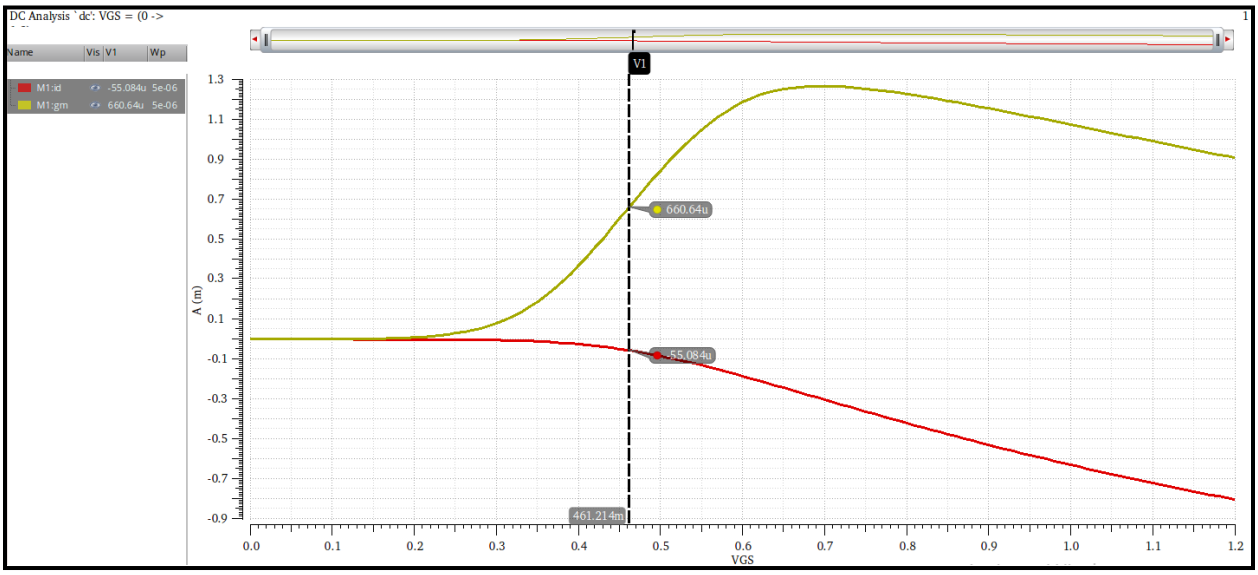


Figure 8: ID and gm of active load

$\therefore I_D \approx 55\mu A\,, \quad g_m = 0.66mS$

W	ID
5 μm	$I_D = 55\ \mu A$
??	$I_{DQ} = 5.5\ mA$

$\therefore W = \frac{5 \times 5.5}{55} \approx 500 \mu m$

$\because g_m$ is also proportional to W (I_D) as long as V_{ov} is constant

$\therefore g_m = \frac{0.66 \times 5.5}{55} = 66 mS$

Current source

For input pair transistors we use relatively long length ($L = 0.2 \mu m$), and a small efficiency ($\frac{g_m}{I_D} = 8$) as we don't need a high g_m from current mirror because it doesn't contribute in calculations for gain.

$$\because \frac{g_m}{I_D} = 8\,, \qquad \therefore V^* = \frac{2}{g_m/I_D} = \frac{2}{8} \approx 250 mV$$

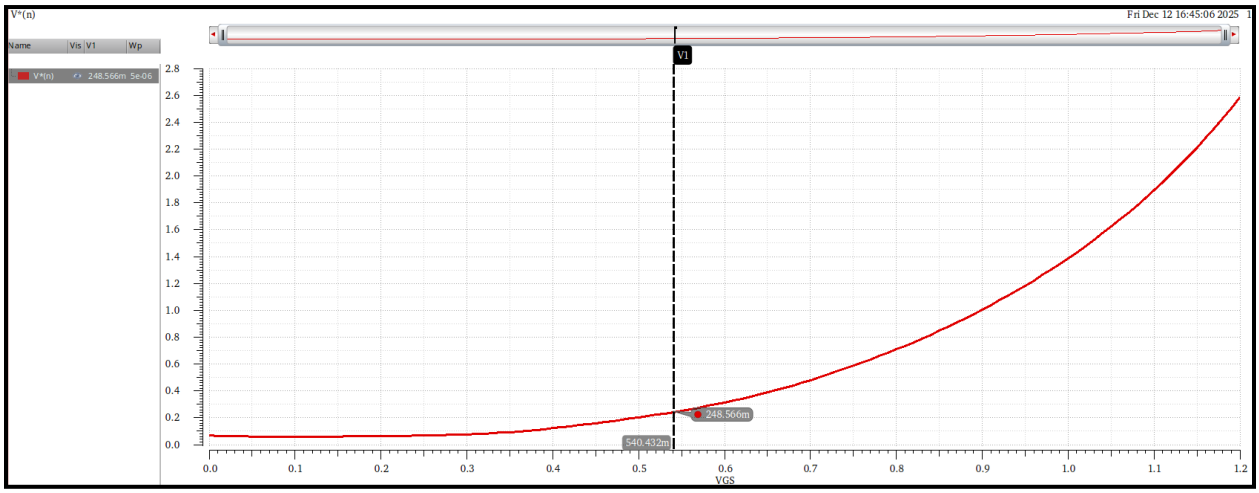


Figure 9: Vgs of current source

$\therefore V_{gs} \approx 540 mV$

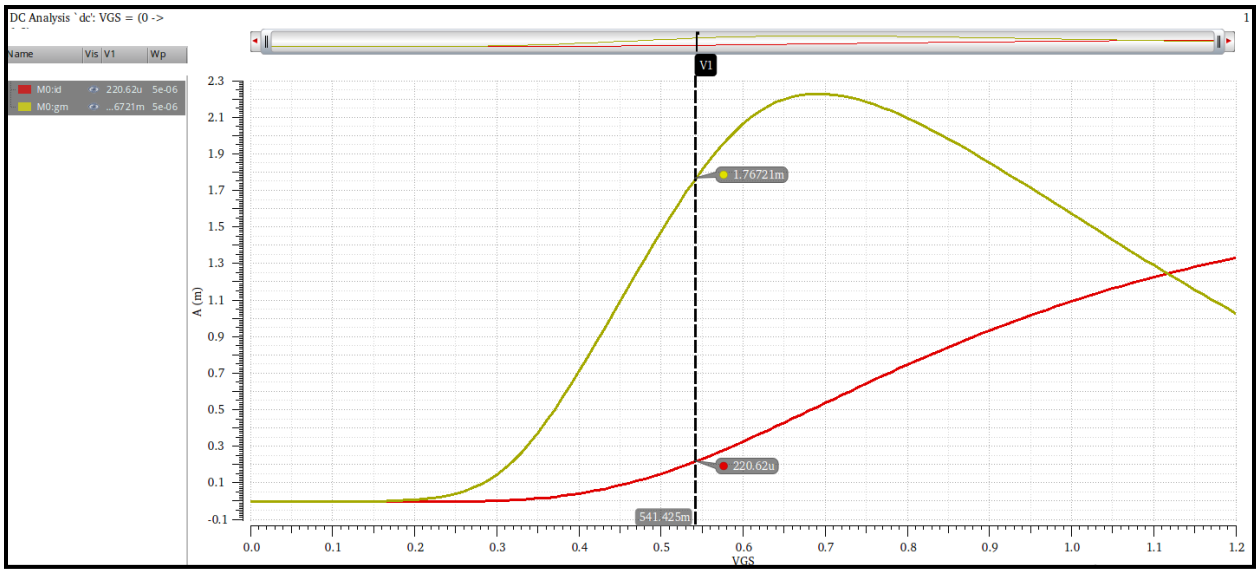


Figure 10: ID and gm of current

$\therefore I_D \approx 220\mu A\,,\quad g_m = 1.76721mS$

W	ID
5 $\boldsymbol{\mu m}$	$I_D = 220\ \mu A$
??	$I_{DQ} = 11\ mA$

$$\therefore W = \frac{5 \times 11}{220} \approx 250\mu m$$

$\because g_m$ is also proportional to W (I_D) as long as V_{ov} is constant

$$\therefore g_m = \frac{1.76721 \times 11}{220} = 88.3mS$$

Final design :

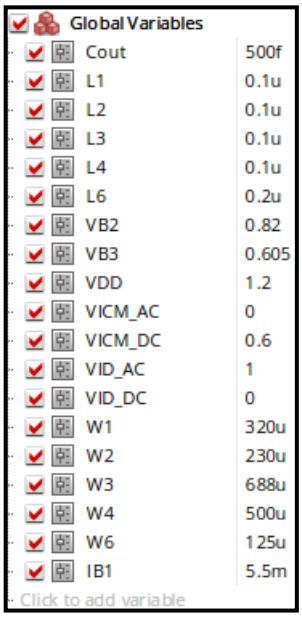
	W	L
Input pair	$320\mu m$	$0.1\mu m$
Cascode NMOS	$230\mu m$	$0.1\mu m$
Cascode PMOS	$688\mu m$	$0.1\mu m$
Active load	$500\mu m$	$0.1\mu m$
Current source	$250\mu m$	$0.2\mu m$

$V_{B2} = V_{gs-cascn} + V_{IP}^{*} + V_{CS}^{*} = 0.445 + 0.125 + 0.25 = 0.82V$

$V_{B3} = V_{DD} - V_{AL}^{*} - V_{gs-cascp} = 1.2 - 0.165 - 0.43 = 0..605V$

And assuming $V_{ICM-DC} = 0.6V$

After simulation we get that $Gain = 75.94\ dB$ and $BW = 1.55MHz$.



ITI:IC_project_Q1:1	BW	1.55M
ITI:IC_project_Q1:1	max_gain	75.94

Note that $W_6 = 0.5 \times W_{CS}$

After tuning the parameters to achieve the specifications we get that

Global Variables	
Cout	500f
L1	0.1u
L2	0.1u
L3	0.15u
L4	95n
L6	0.18u
VB2	0.9
VB3	0.5
VDD	1.2
VICM_AC	0
VICM_DC	0.65
VID_AC	1
VID_DC	0
W1	290u
W2	235u
W3	650u
W4	500u
W6	100u
IB1	5.5m
Click to add variable	

ITI:IC_project_Q1:1	BW	1.009M
ITI:IC_project_Q1:1	max_gain	80.04

$\because Gain\ boosting = 40\ dB\ ,\quad \therefore Main\ amplifier\ gain = 80.04 - 40 = 40.04\ dB$

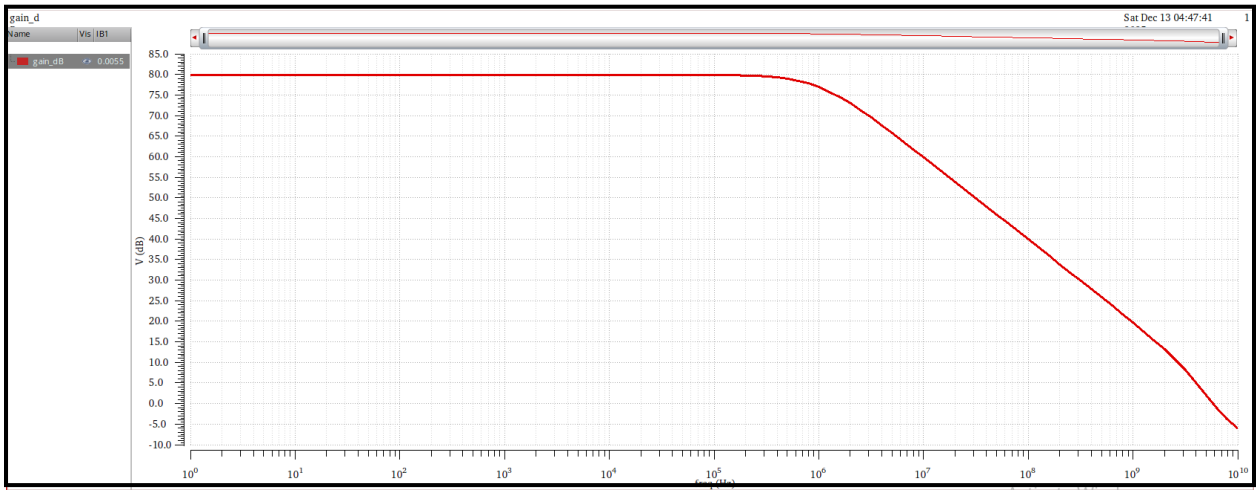


Figure 11: Gain in dB

The dissipated power equal $\mathbf{2 \times V_{DD} \times I_{B1} = 2 \times 1.2 \times 5.5 = 13.2mW}$

Operating points

Input pair

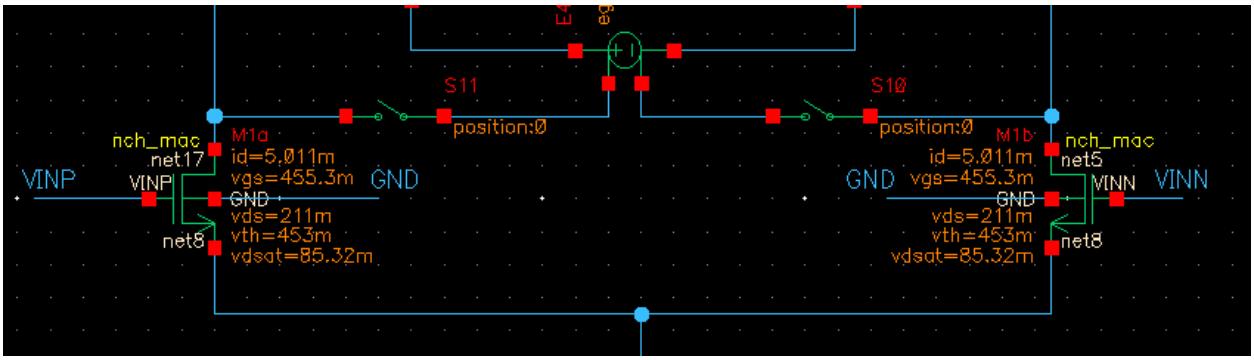


Figure 12: Input pair OP

Cascode transistors

Cascode NMOS

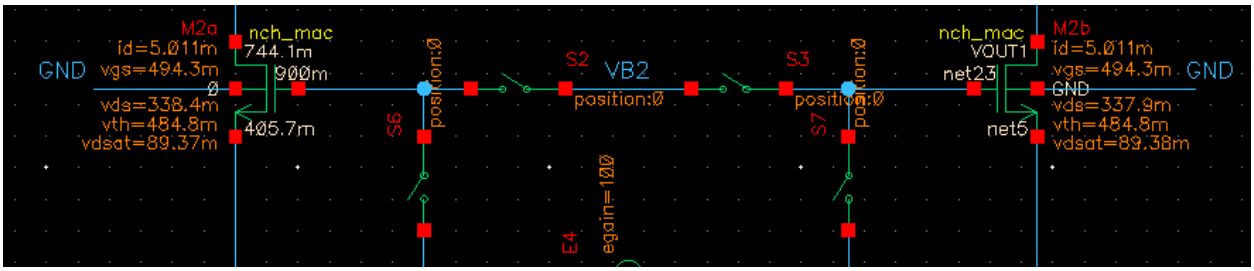


Figure 13: Cascode NMOS OP

Cascode PMOS

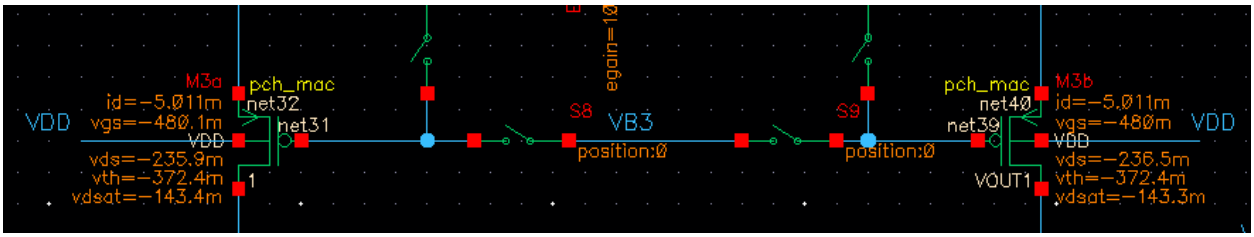


Figure 14: Cascode PMOS OP

Active load or current mirror

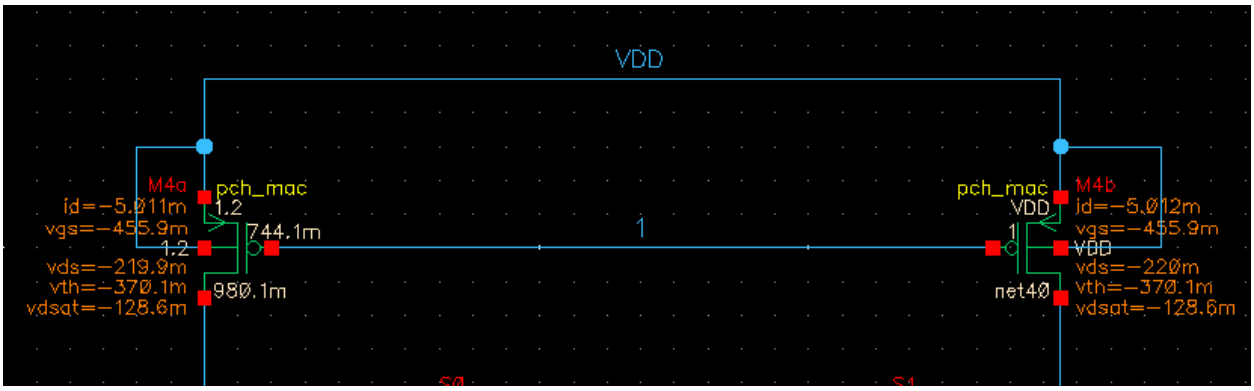


Figure 15: Active load OP

Current source

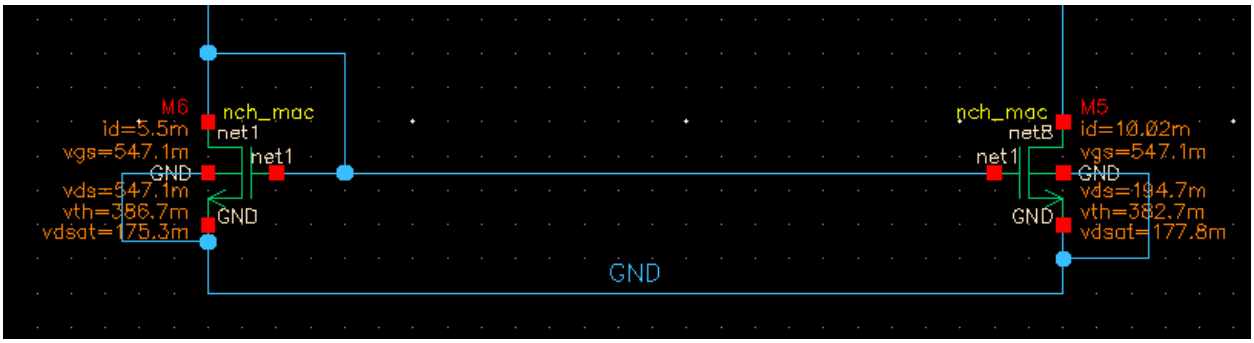


Figure 16: Current source OP

Final design and operating points

	M1a	M1b	M2a	M2b	M3a	M3b
L	$0.1\mu m$	$0.1\mu m$	$0.1\mu m$	$0.1\mu m$	$0.15\mu m$	$0.15\mu m$
W	$290\mu m$	$290\mu m$	$235\mu m$	$235\mu m$	$650\mu m$	$650\mu m$
ID	$5.011mA$	$5.011mA$	$5.011mA$	$5.011mA$	$5.011mA$	$5.011mA$
Vgs	$455.3mV$	$455.3mV$	$494.3mV$	$494.3mV$	$480.1mV$	$480.1mV$
Vds	$211mV$	$211mV$	$338.4mV$	$338.4mV$	$235.9mV$	$235.9mV$
Vth	$453mV$	$453mV$	$484.8mV$	$484.8mV$	$372.4mV$	$372.4mV$
Vdsat	$85.32mV$	$85.32mV$	$89.37mV$	$89.38mV$	$143.4mV$	$143.3mV$
Region	2	2	2	2	2	2
gm	$77.07mS$	$77.07mS$	$73.92mS$	$73.91mS$	$59.5mS$	$59.51mS$
ro	186.8Ω	186.8Ω	258Ω	257.7Ω	231.6Ω	232Ω

	M4a	M4b	M5	M6
L	$95nm$	$95nm$	$0.18\mu m$	$0.18\mu m$
W	$500\mu m$	$500\mu m$	$200\mu m$	$100\mu m$
ID	$5.011mA$	$5.011mA$	$5.022mA$	$5.5mA$
Vgs	$455.9mV$	$455.9mV$	$547.1mV$	$547.1mV$
Vds	$219.9mV$	$220mV$	$194.7mV$	$547.1mV$
Vth	$370.1mV$	$370.1mV$	$382.7mV$	$386.7mV$
Vdsat	$128.6mV$	$128.6mV$	$177.8mV$	$175.3mV$
Region	2	2	2	2
gm	$62mS$	$62mS$	$75.47mS$	$43.97mS$
ro	142.6Ω	142.6Ω	77.11Ω	684.1Ω

$$\therefore Total\ Area = Area_{IP} + Area_{cascn} + Area_{cascp} + Area_{AL} + Area_{CS}$$

$$= 2 \times 0.1 \times 290 + 2 \times 0.1 \times 235 + 2 \times 0.15 \times 650 + 2 \times 0.095 \times 500 + 0.18 \times 200$$

$$= 58 + 47 + 195 + 95 + 36 = 431\mu m^2$$

Another design for Q1

Note that we use a boosting with value equal 50 linear (34 dB)

Sizing

Input pair and cascode NMOS and current source

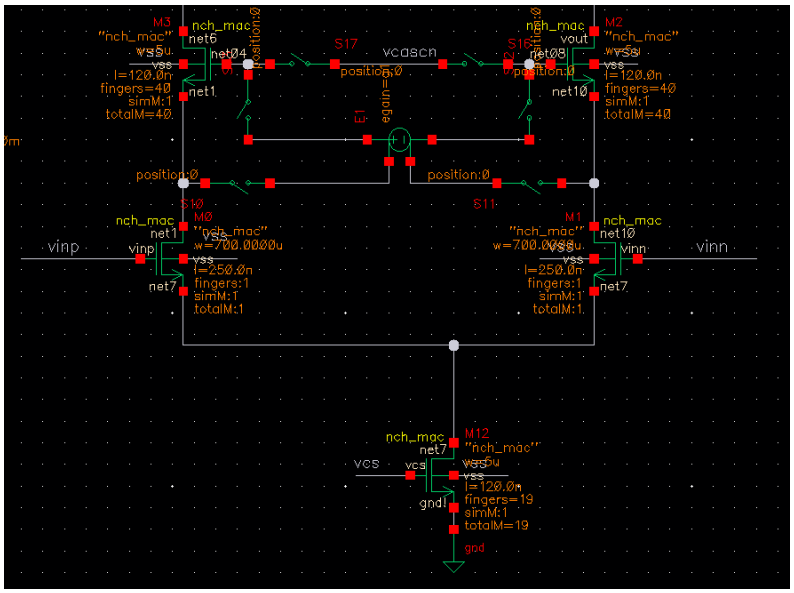


Figure 17: IP and cascn and CS sizing

Cascode PMOS and active load sizing

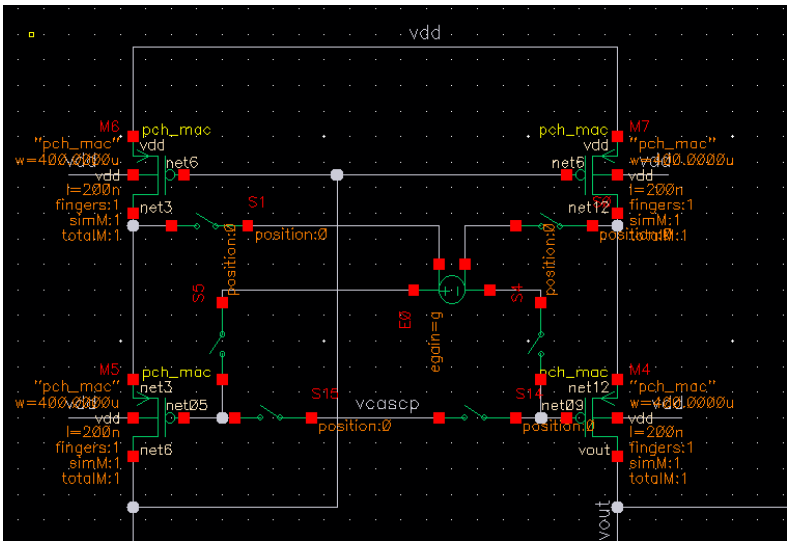


Figure 18: cascp and AL sizing

Operating points

Input pair and cascode NMOS and current source

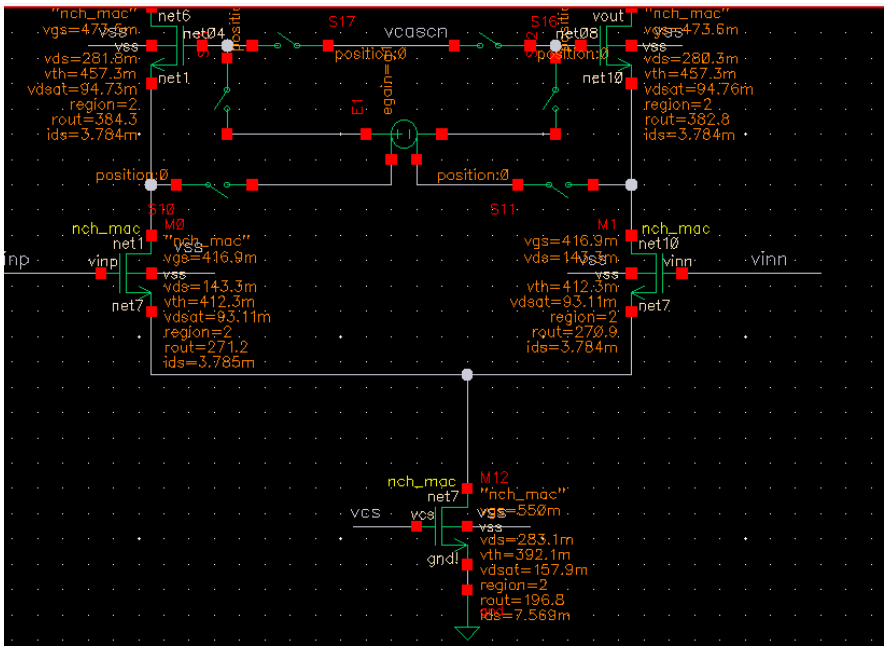


Figure 19: IP and cascn and OPs

Cascode PMOS and active load sizing

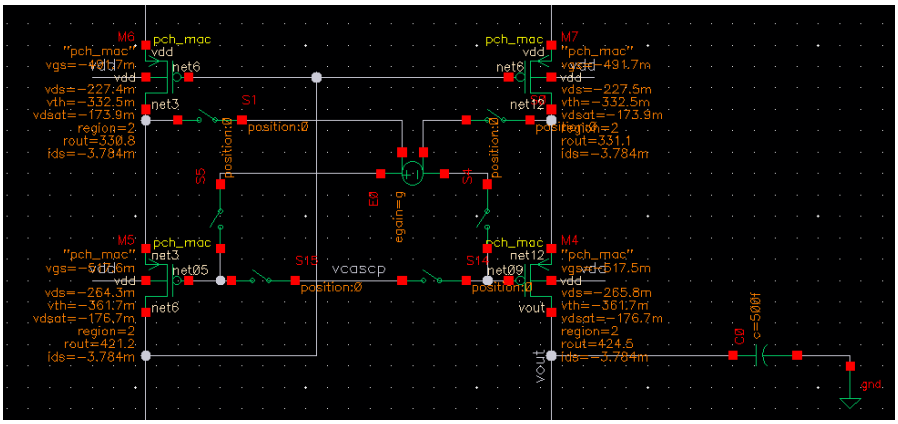


Figure 20: cascp and AL OPs

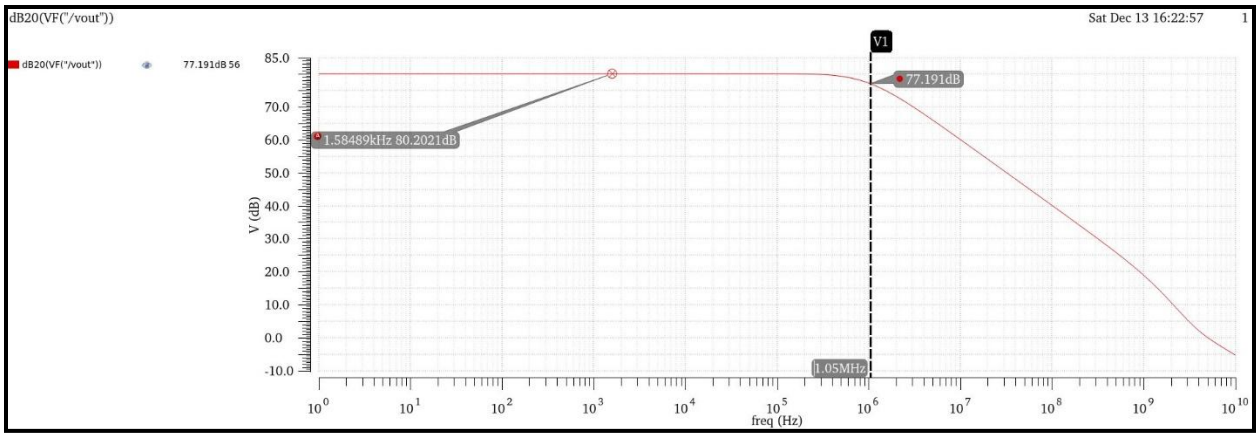


Figure 21: Gain in dB and 3-dB bandwidth

Project:P1_1:1	Gain	80.2	> 80		pass
Project:P1_1:1	BW	1.05M	> 1M		pass

Figure 22: Specifications verification

The dissipated power equal $2 \times V_{DD} \times I_{B1} = 2 \times 1.2 \times 3.785 = 9.084mW$

Q2

This part of the project focuses on the design and simulation of an analog function generator capable of producing square, triangular, and sine waveforms over a frequency range from $100\ kHz$ to $10\ MHz$. The system is composed of three main stages: an astable multi-vibrator for square wave generation, a integrator for triangular wave generation, and a low-pass filter to obtain a low-distortion sine wave.

The values of resistors and capacitors are selected based on analytical calculations to cover the required frequency range. The complete circuit is simulated using operational amplifier models with finite gain and bandwidth to represent non-ideal behavior. Output waveforms are analyzed at the minimum and maximum frequencies, and signal quality is evaluated using Discrete Fourier Transform (DFT) and Total Harmonic Distortion (THD) analysis.

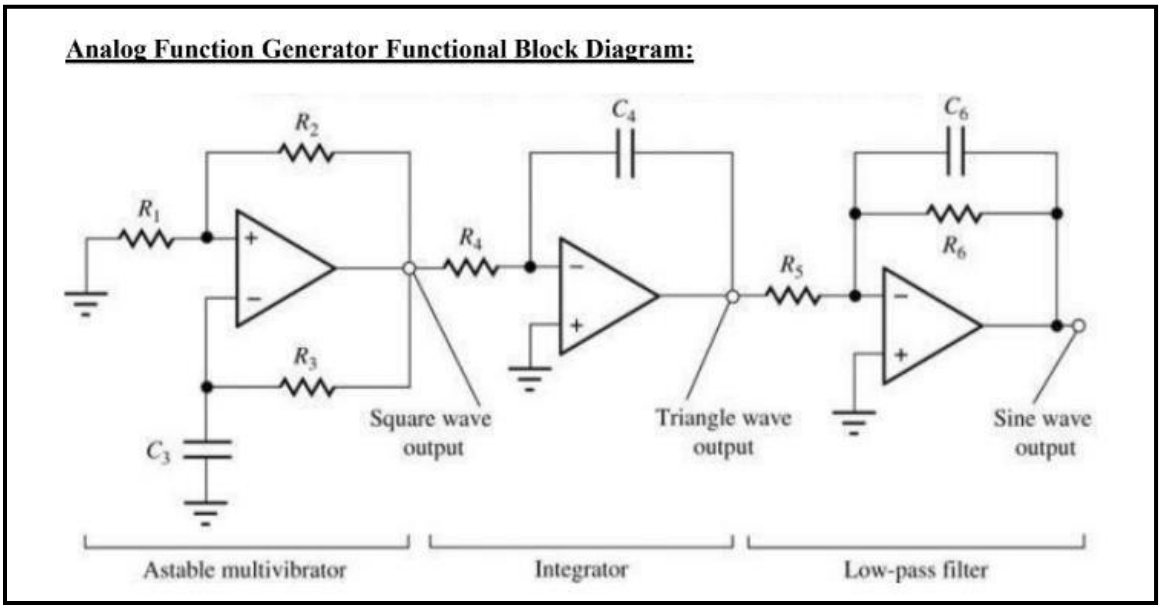


Figure 23: Function generator schematic

Hand Analysis

1st Stage (Astable Multi-vibrator)

$$v_{sq}(t) = \begin{cases} +V_{sat}, & 0 \le t < t_{\frac{1}{2}T} \\ -V_{sat}, & t_{\frac{1}{2}T} \le t < T \end{cases} \quad , \qquad \alpha = \frac{R_1}{R_2 + R_1}$$

$$\because T = 2R_3C_3 \ln\left(\frac{1+\alpha}{1-\alpha}\right), \qquad \therefore f_{op} = \frac{1}{T} = \frac{1}{2R_3C_3 \ln\left(\frac{1+\alpha}{1-\alpha}\right)}$$

Choosing $R_1 = 35K\Omega$ & $R_2 = 30\ K\Omega$ such that $\alpha = 0.462$. This makes the Natural Log at the denominator equal to 1 removing the dependency of frequency on R1 and R2.

To operate in the required frequency range:

$$Let\ C_3 = 50\ pF\ , \quad \therefore R_3\ is\ from\ 1\ K\Omega\ (\max freq)\ to\ 100K\Omega\ (\min \text{freq})$$

2nd Stage (Ideal Integrator)

$$H_{int}(s) = \frac{V_{tri}(s)}{V_{in}(s)} = -\frac{1}{R_4C_4s} \ , \qquad \therefore f_{c1} = \frac{1}{2\pi R_4C_4} . \frac{V_{in}}{V_{out}}$$

$f_{c1}\ must\ be\ less\ than\ the\ least\ f_{op}$

$$\therefore R_4C_4 > \frac{1}{2\pi f_{op-min}} (1)$$

$$\because V_{\text{out}}(t) = -\frac{1}{R_4C_4}\int V_{\text{in}}(t)dt + V_{\text{out}}(0)$$

$Since\ V_{\text{out}}(0) = 0, using\ V_{\text{in}}(t) = -V_{sat}\ and\ integrating\ from\ 0\ to\ t_{\frac{1}{2}T}$

we get that $R_4C_4 = \frac{V_{sat}\ t_{\text{high}}}{V_{\text{out}}}$

$To\ obtain\ R_4C_4\ value\ that\ saturates\ integrator\ output\ use\ V_{\text{out}} = V_{sat}\ and\ maximum\ t_{\text{high}}$

$$\therefore R_4C_4 = t_{\text{high}}, so\ we\ need\ R_4C_4 > t_{\text{high}}\ (2)$$

Using this Relation we estimate the best Gain between the Low and High frequencies for the second stage is 1 (for Min Frequency) and 0.01 (For Max Frequency)

$$Let\ R_4 = 100K\Omega\ , \quad \therefore C_4 = 16pF$$

3rd Stage (Active Low Pass Filter)

$\because Z_f(s) = \frac{R_6}{1+sR_6C_6}$, $\therefore H_{LPF}(s) = -\frac{Z_f(s)}{R_5} = -\frac{R_6}{R_5} \times \frac{1}{1+sR_6C_6}$, $\therefore |H_{LPF}(0)| = \frac{R_6}{R_5}$

$\because f_{c2} = \frac{1}{2\pi R_6 C_6}$

$f_{c2}\ must\ be\ larger\ than\ the\ largest\ f_{op}$

$\therefore R_6C_6 < \frac{1}{2\pi f_{op-max}}$

Designing for the worst Case ($F_{min} = 100KHz$)

$Let\ R_6 = 100K\Omega$, $\therefore C_6 = 16pF$

And design for DC Gain of the LPF to equal to 2 to account for losses from the previous stage

$\therefore R_5 = \frac{1}{2}R_6 = 50K\Omega$

Initial Design Point Summary:

Stage 1: Astable Multivibrator	
R1	$35\ K\Omega$
R2	$30\ K\Omega$
R3	$1\ K\Omega\ to\ 100K\Omega$
C3	$50\ pF$
Stage 2: Ideal Integrator	
R4	$100\ K\Omega$
C4	$16\ pF$
Stage 3: Active Low Pass Filter	
R5	$50\ K\Omega$
R6	$100\ K\Omega$
C6	$16\ pF$

Design Iterations:

After testing the previous results at the minimum frequency it was found that the required frequency was not met exactly and the sine and triangular outputs were saturating, requiring fine tune the values of the capacitors

Stage 1: Astable Multivibrator	
R1	$35\ K\Omega$
R2	$30\ K\Omega$
R3	$1\ K\Omega\ to\ 100K\Omega$
C3	$41.5\ pF$
Stage 2: Ideal Integrator	
R4	$100\ K\Omega$
C4	$30\ pF$
Stage 3: Active Low Pass Filter	
R5	$50\ K\Omega$
R6	$100\ K\Omega$
C6	$30\ pF$

Peak to Peak Values attenuating at High Frequency

Testing this design at high frequencies we found the sine and triangular output die out at high frequencies with very low peak to peak values due to them being well inside the cut off range of the integrator and low pass filter characteristics.

The solution we proposed to this was to have variable resistors at each stage changing with the same value as Resistor R3 in the first stage, such that the cut off range for each stage changes by changing the frequency.

In the Simulator this can be easily done by giving each of them as variable R that can be changed for each run. In actual hardware though this can be done with switches and digital circuitry to connect different resistors at each stage depending on the required frequency. Or alternatively using transistors as variable resistors though this is a more complicated solution and probably unviable in our case due to the large resistor values used (Which can be fixed by using bigger capacitors instead but the complexity of using transistors remain).

Final Design Point Summary

Stage 1: Astable Multivibrator	
R1	$35\ K\Omega$
R2	$30\ K\Omega$
R3	R
C3	$41.5\ pF$
Stage 2: Ideal Integrator	
R4	R
C4	$30\ pF$
Stage 3: Active Low Pass Filter	
R5	$R/2$
R6	R
C6	$30\ pF$

Where R changes from $1\ K\Omega\ (\max freq)\ to\ 100K\Omega\ (\min \text{freq})$ depending on the required frequency.

Testing the oscillator

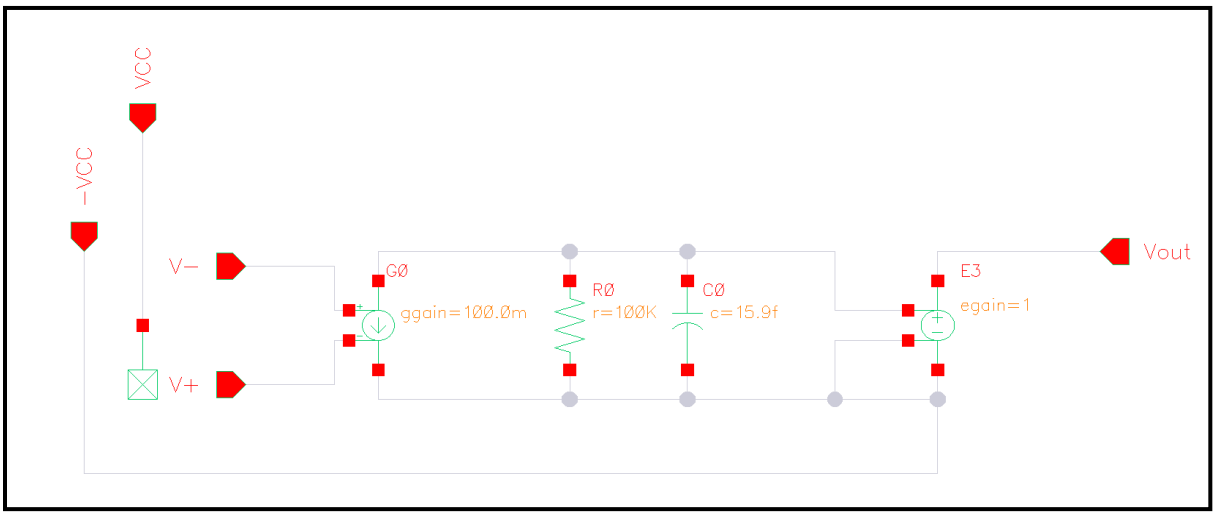


Figure 24: Behavioural Model of the Op-Amp

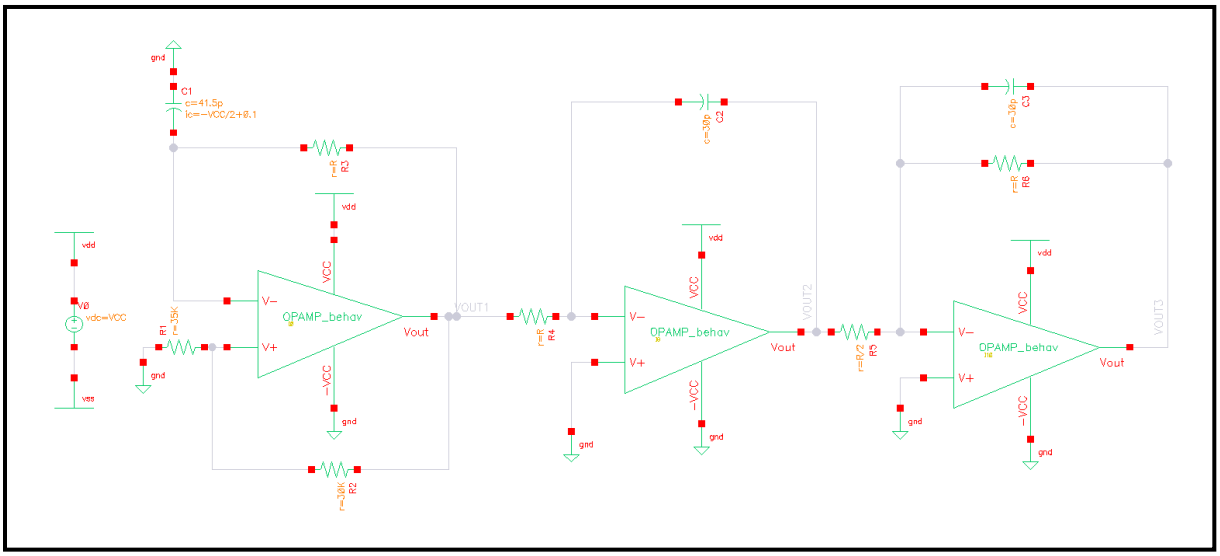


Figure 25: Final Schematic of Function Generator with chosen values

We are using $V_{DD} = 1.2$ like the real Op-Amp for the next part and R changes according to what was calculated in the previous part

Waveforms of the Three Stages

THD and DFT Output Setups

DFT

Discrete Fourier Transform gives the spectrum of the signal showing the contribution of each frequency component on the signal. It can be obtained easily on cadence using the calculator function for it with appropriate inputs and a number of samples high enough to capture the highest frequency

DFT 4096	expr	dB20(dft(VT("/VOUT3") 0.0003 0.0005 4096 "Rectangular" 1 "default" 1.0))

Figure 26: Output Setup for DFT in dB

THD

The THD or Total Harmonic Distortion is the ratio between the RMS value of all harmonic components (excluding the fundamental) to the RMS value of the fundamental frequency. It is a measure of the purity of the sinusoidal wave.

It can be calculated from the DFT of the signal according to the following equation:

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{H} V_h^2}}{V_1}$$

$$THD_{dB} = 20 \cdot log_{10}(THD), \qquad THD_{\%} = 100 \cdot THD$$

we will simply use the THD equation in virtuoso though giving it the fundamental frequency and a number of samples high enough that fulfills the Nyquist Criteria. we will make it work on a small sample of the signal at the middle of its operation such that it has settled in.

THD 100K	expr	dB20((thd(VT("/VOUT3") 0.0004 0.0006 4096 100000) / 100))
THD 10M	expr	dB20((thd(VT("/VOUT3") 0.0004 0.0006 4096 10000000) / 100))

Figure 27: Output Setup of THD in dB

Gain = 10,000 and Bandwidth = 100MHz (Original Case)

$G_m = 100m, \quad R_{out} = 100K\Omega, \quad C_{out} = 15.9fF$

Minimum Frequency (100KHz)

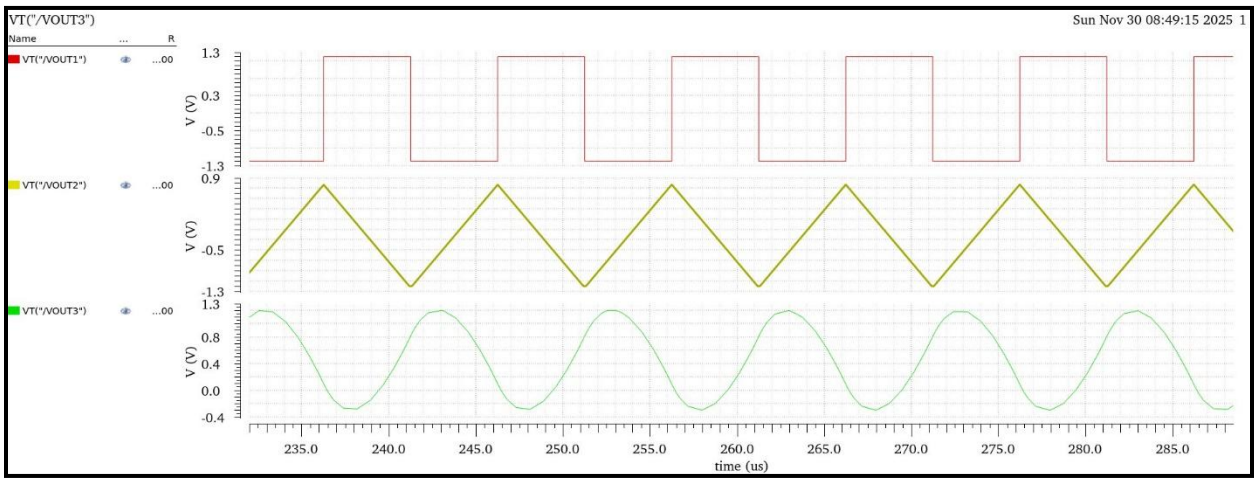


Figure 28: The 3 Outputs at Minimum Frequency (100KHz)

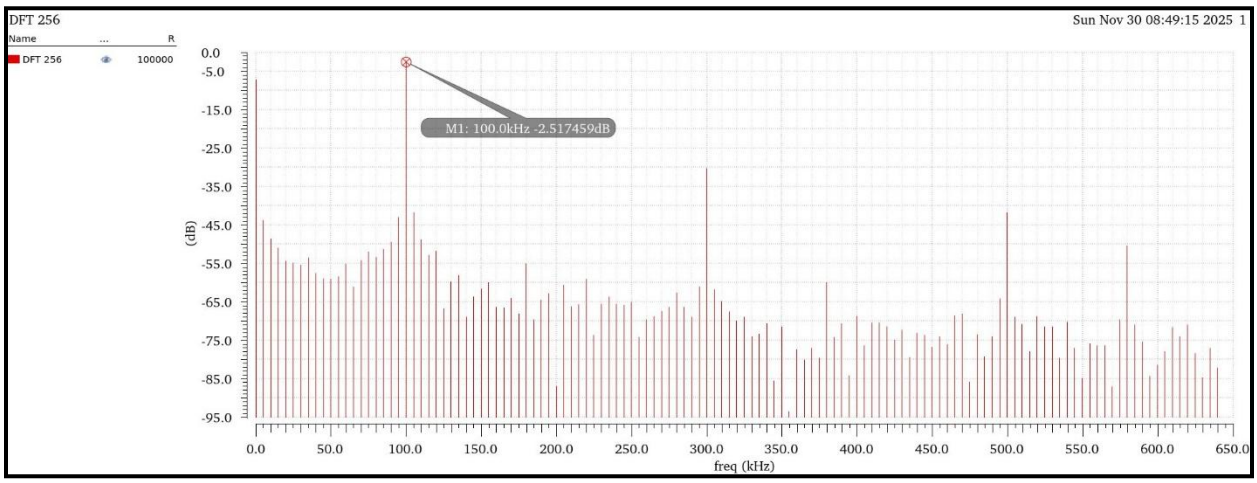


Figure 29: DFT of the Minimum Frequency (100KHz) in dB

THD 100K	-26.33

Figure 30: THD Value at Minimum Frequency in dB

Comment:

Outputs are as expected for the design with low THD

Maximum Frequency (10MHz)

According to Analytical results the Maximum Frequency should be obtained at $R = 1K\Omega$, but in reality it wasn't exactly achieved and need to be a bit lower than that ($R = 960\Omega$).

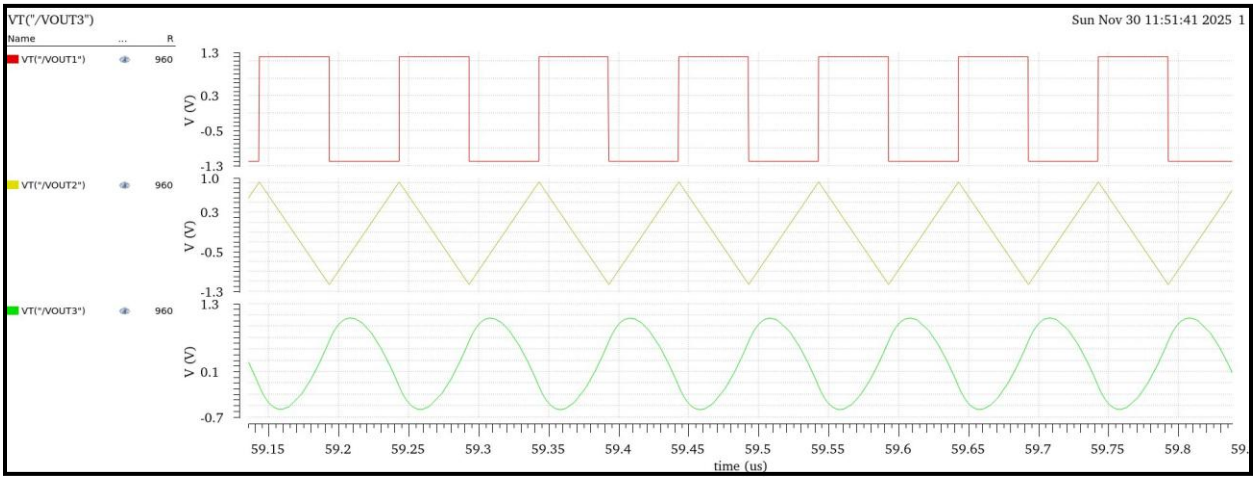


Figure 31: The 3 Outputs at the Maximum Frequency (10MHz)

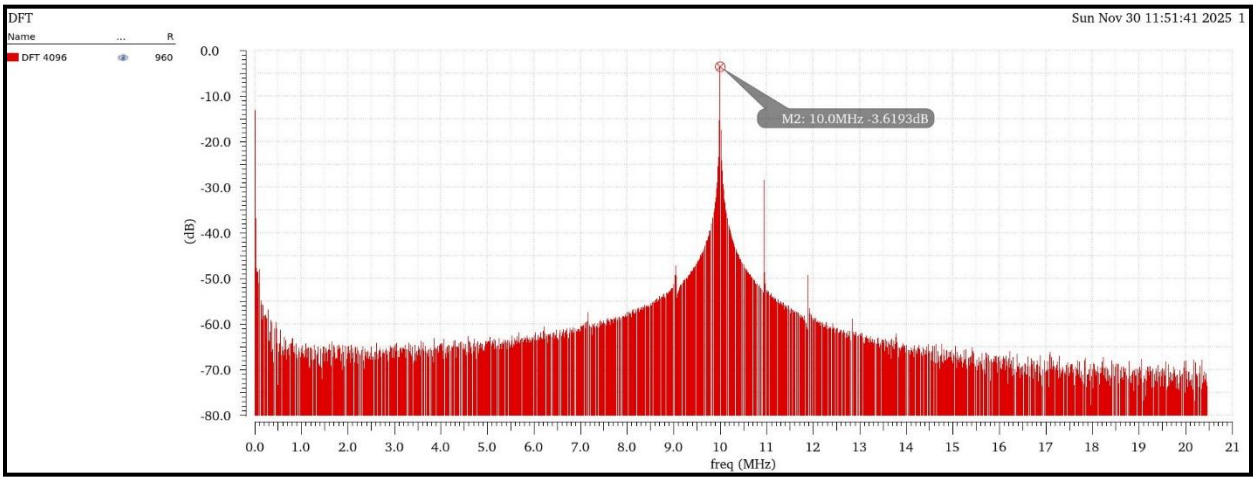


Figure 32: DFT of the Maximum Frequency (10MHz) in dB

THD 10M	-2.871

Figure 33: THD Value at Maximum Frequency (10MHz) in dB

Comment:

Outputs are as expected for the design with relatively low THD

Gain = 1000 and Bandwidth = 100MHz

$Gain = G_m \times R_{out}$, changing either in the behavioral model changes the gain as needed. we changed G_m to avoid changing Bandwidth as well.

$G_m = 10m, \quad R_{out} = 100K\Omega, \quad C_{out} = 15.9fF$

Minimum Frequency (100KHz)

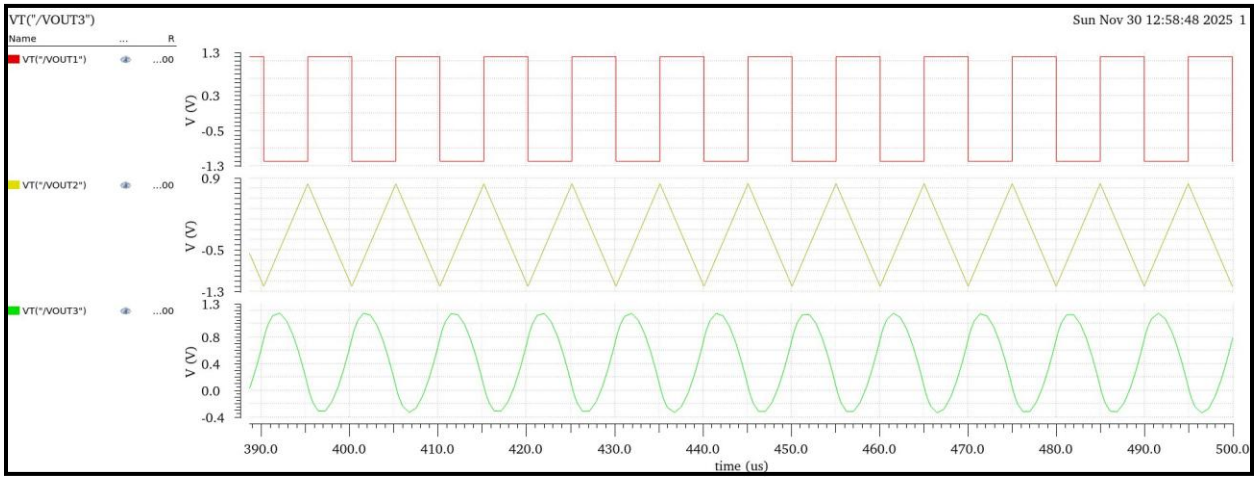


Figure 34: The 3 Outputs at Gain = 1000 at Minimum Frequency

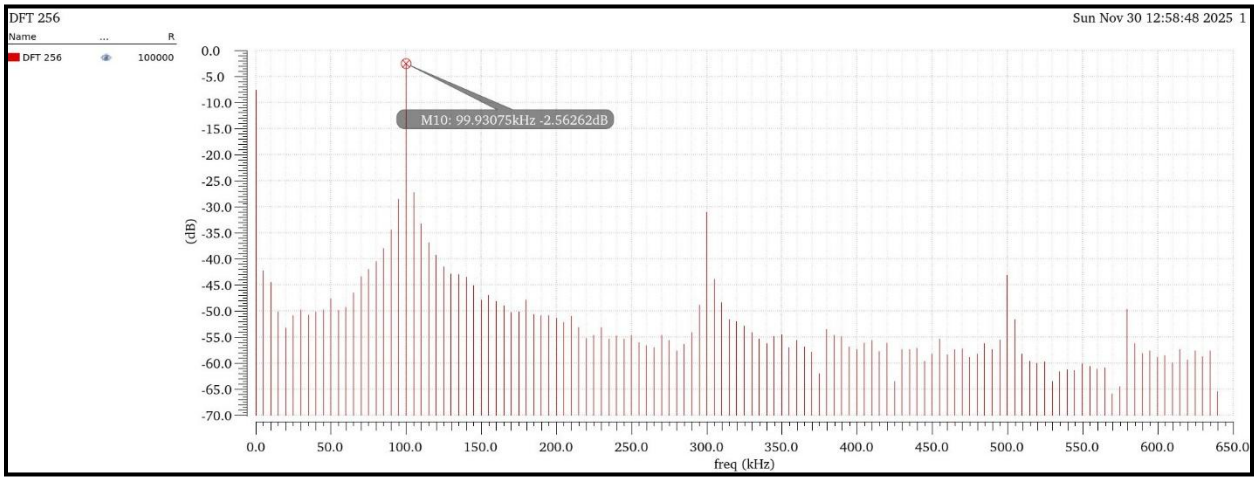


Figure 35: DFT at Gain = 1000 at Minimum Frequency

THD 100K	-21.98

Figure 36: THD at Gain = 1000 at Minimum Frequency

Comment:

Visually the signal looks at the same though it took a longer time to settle (Not Visible in the Graph) and THD is a little bit Higher.

Maximum Frequency (10MHz)

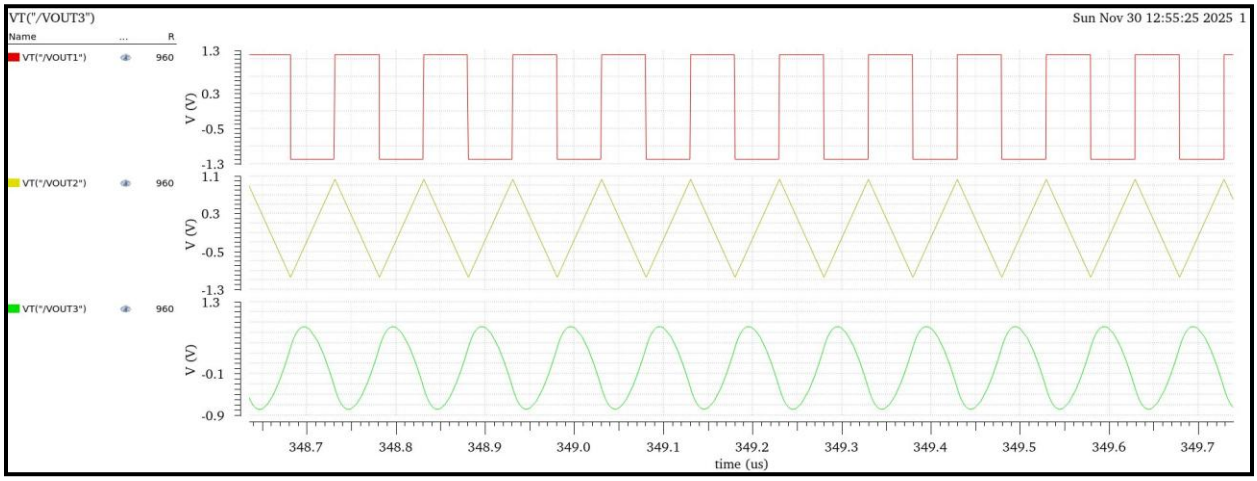


Figure 37: The 3 Outputs at Gain = 1000 and Maximum Frequency

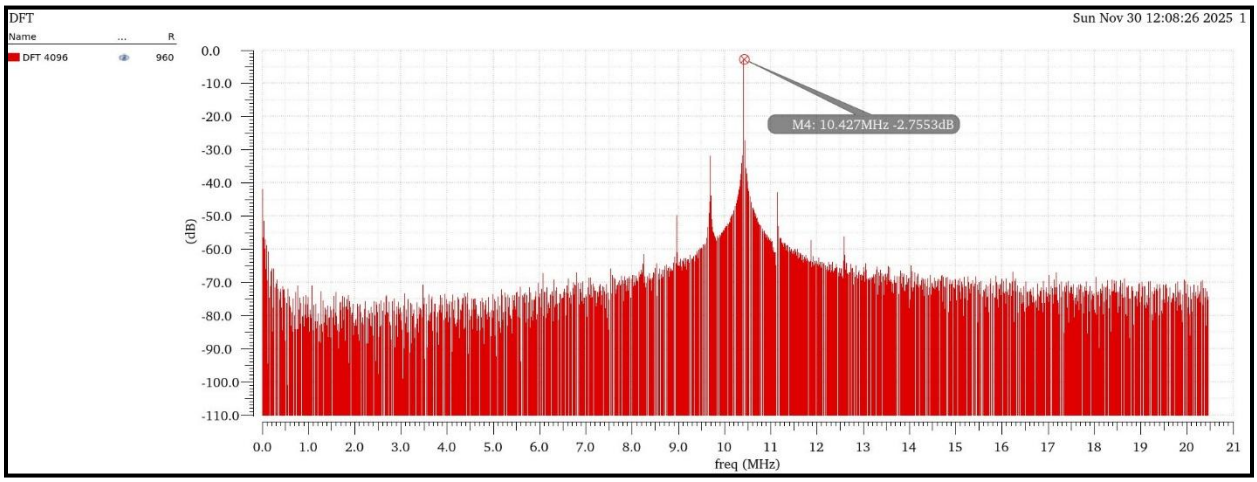


Figure 38: DFT at Gain = 1000 and Max Frequency

THD 10M	27.25

Figure 39: THD at Gain 1000 at Maximum Frequency

Comment:

THD is significantly higher as other frequency components gain higher powers as an effect of lowering the gain of the Op-Amp.

Gain = 100 and Bandwidth = 100MHz

$G_m = 1m, \quad R_{out} = 100K\Omega, \quad C_{out} = 15.9fF$

Minimum Frequency (100KHz)

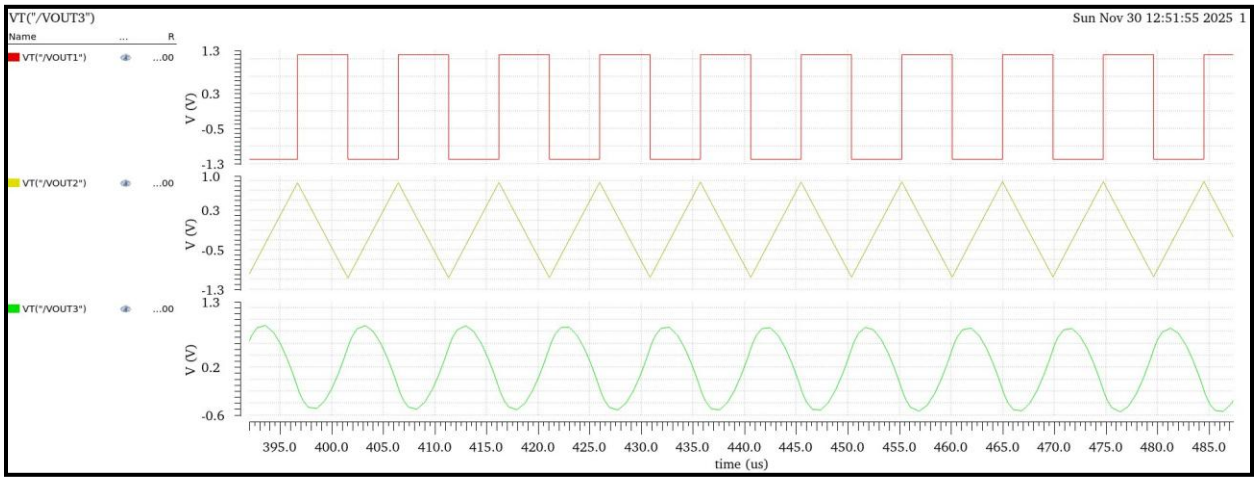


Figure 40: The 3 Outputs at Gain = 100 and Min Frequency (100KHz)

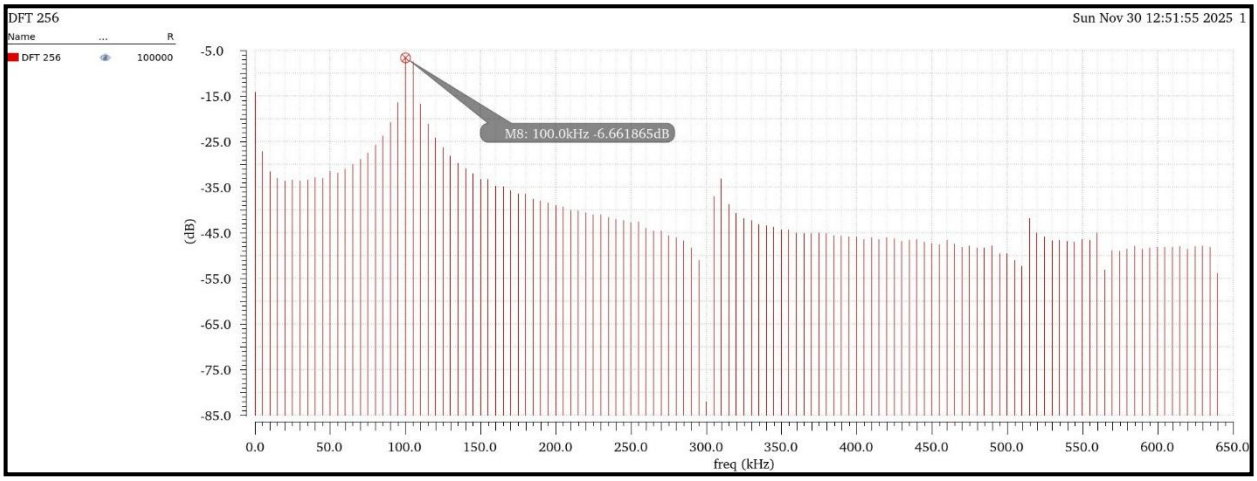


Figure 41: DFT at Gain = 100 and Min Frequency (100KHz)

THD 100K	-6.644

Figure 42: THD at Gain = 100 and Min Frequency (100KHz) in dB

Comment:

THD is Significantly Lower due to the bigger shift in frequency and the existence of other frequency components close to the Fundamental as evident in the DFT. as the Op-Amp grows further away from its ideal state.

Maximum Frequency (10MHz)

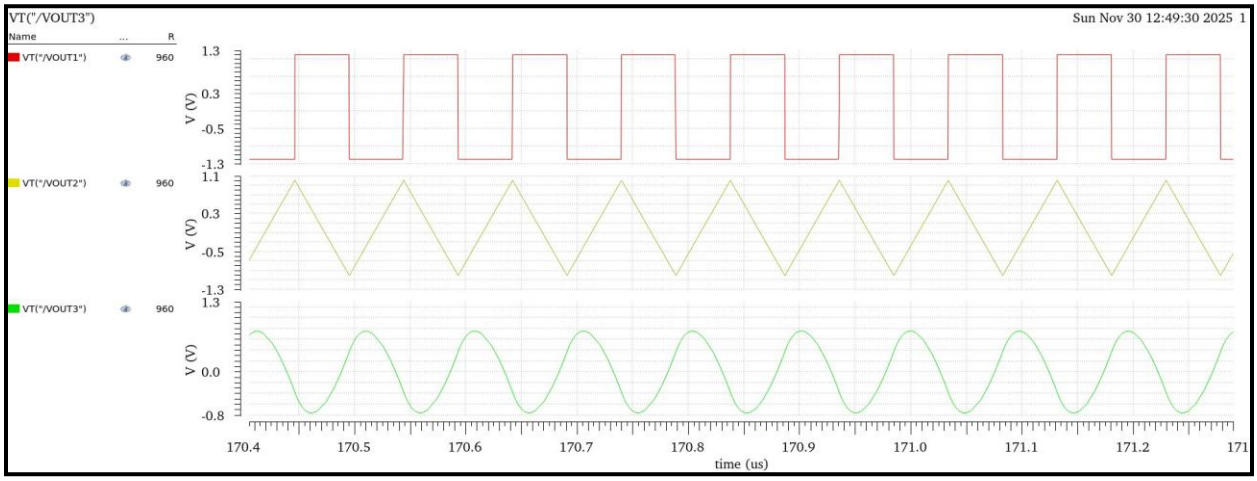


Figure 43: The 3 Outputs at Gain 100 at Max Frequency (10MHz)

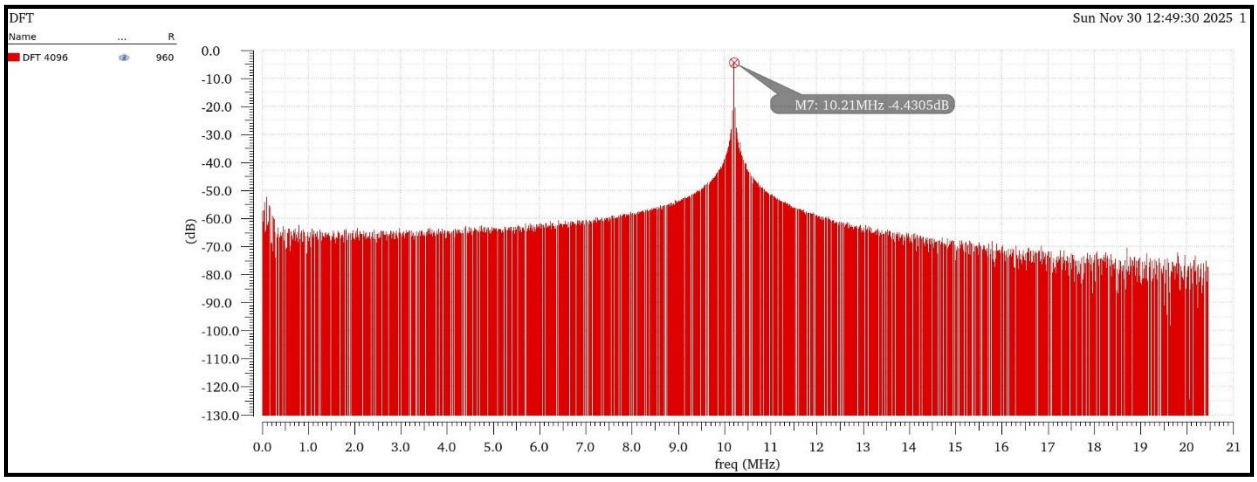


Figure 44: DFT at Gain = 100 and Max Frequency (10MHz) in dB

THD 10M	36.67

Figure 45: THD at Gain = 100 at Max Frequency (10MHz) in dB

Comment:

Similar to the min frequency the THD is significantly larger due to the same reasons.

Gain = 10,000 and Bandwidth = 1MHz

$G_m = 100m, \quad R_{out} = 100K\Omega, \quad C_{out} = 1.59pF$

Minimum Frequency (100KHz)

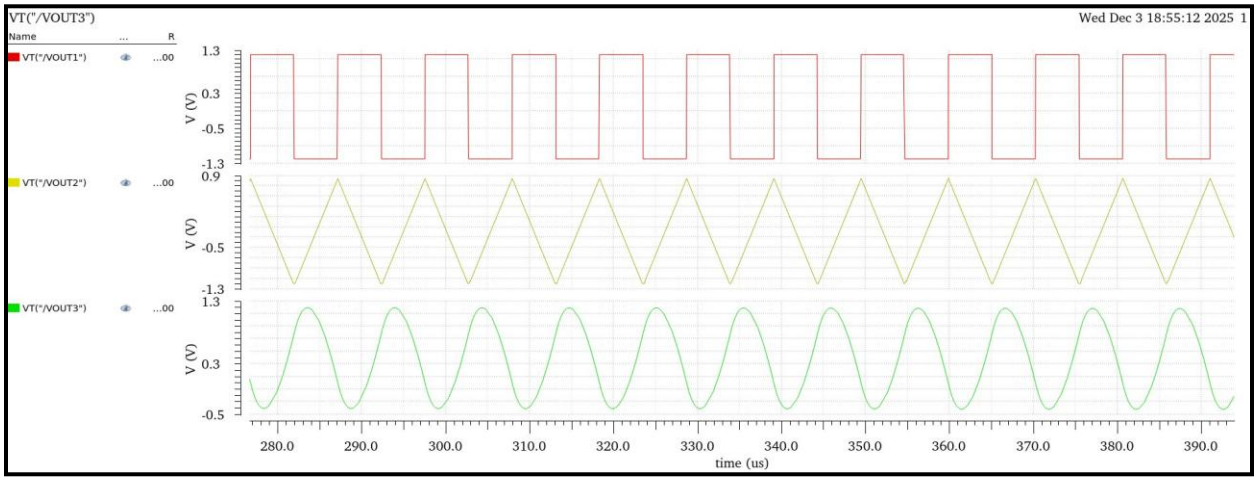


Figure 46: The 3 Outputs at BW 1MHz at Min Frequency (100KHz)

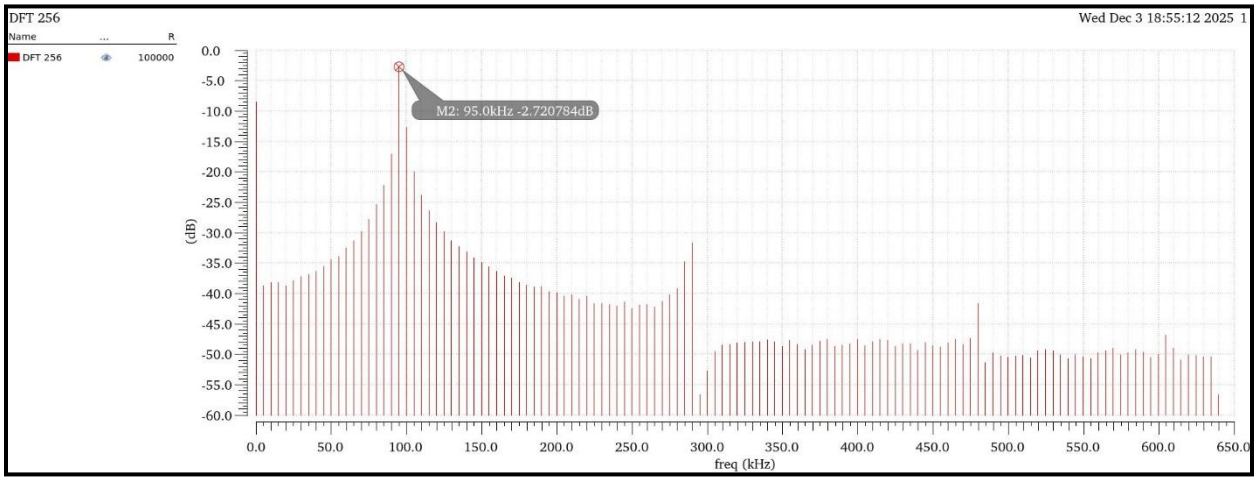


Figure 47: DFT at BW 1MHz and Min Frequency (100KHz) in dB

THD 100K	-1.644

Figure 48: THD at BW = 1MHz and Min Frequency (100KHz) in dB

Comment:

All 3 outputs look relatively good but their average frequency is less than the expected 100KHz to about 95KHz as seen from the DFT. This is also evident from the THD which is considerably lower.

Maximum Frequency (10MHz)

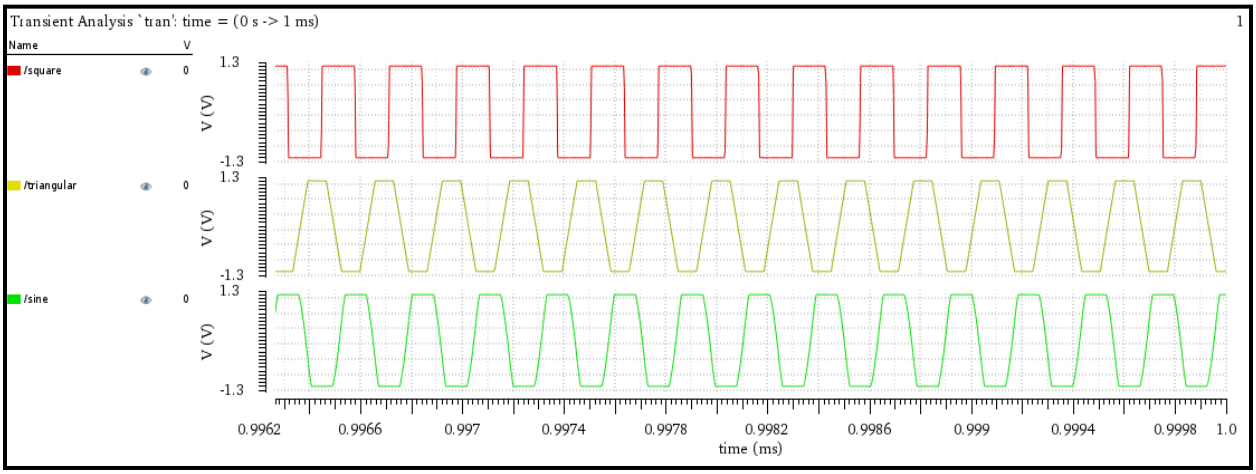


Figure 49: The 3 Outputs at BW 1MHz and Max Frequency Setting

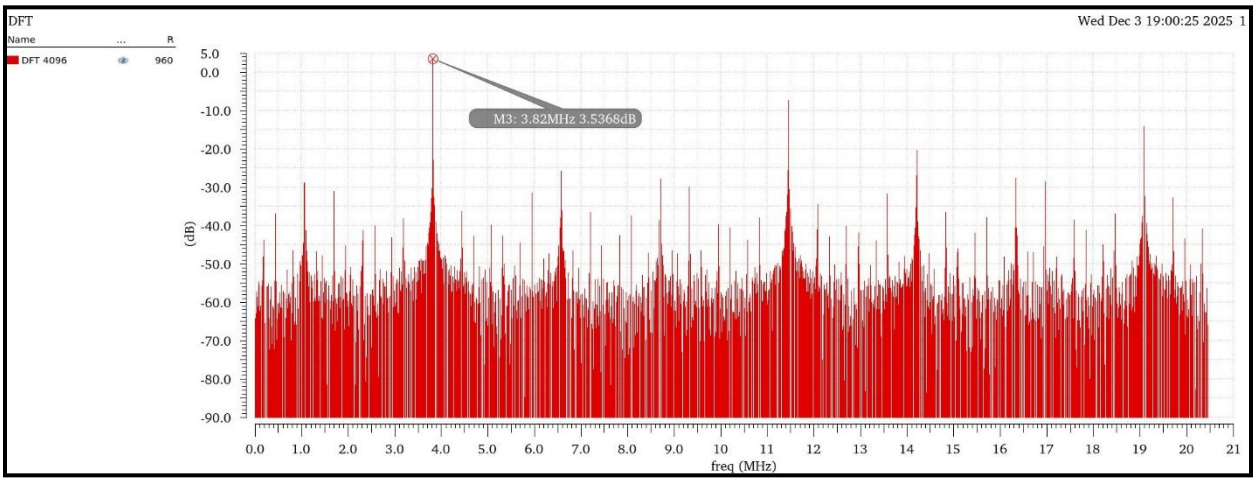


Figure 50: DFT at BW 1MHz and the Max Frequency Setting

THD 10M	65.79

Figure 51: THD of 10MHz sine wave at BW 1MHz and Max Frequency Setting

Comment:

Square wave f_{out}=3.7MHz; due to limited BW. The input frequency (10 MHz) exceeds the op-amp BW (1 MHz), so high-order harmonics are heavily attenuated. Only the fundamental component within the BW passes. The op-amp cannot reproduce the high slew-rate required for a 10 MHz triangular wave. The waveform degrades to a lower frequency than the intended; causes higher peak to peak which causes saturation in sine and triangular outputs.

Gain = 10,000 and Bandwidth = 1KHz

$G_m = 100m, \quad R_{out} = 100K\Omega, \quad C_{out} = 1.59nF$

Minimum Frequency (100KHz)

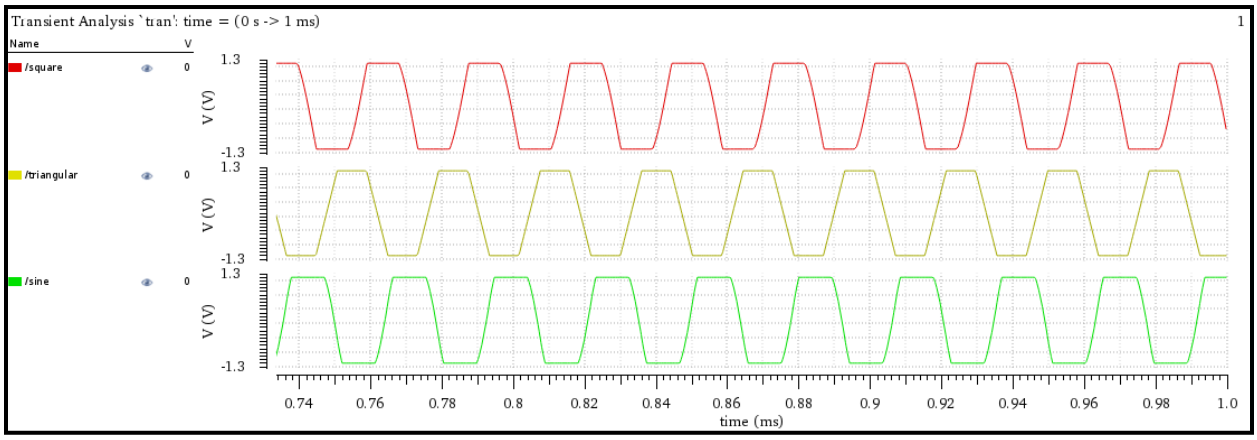


Figure 52: The 3 Outputs at BW 1KHz at Min Frequency Setting

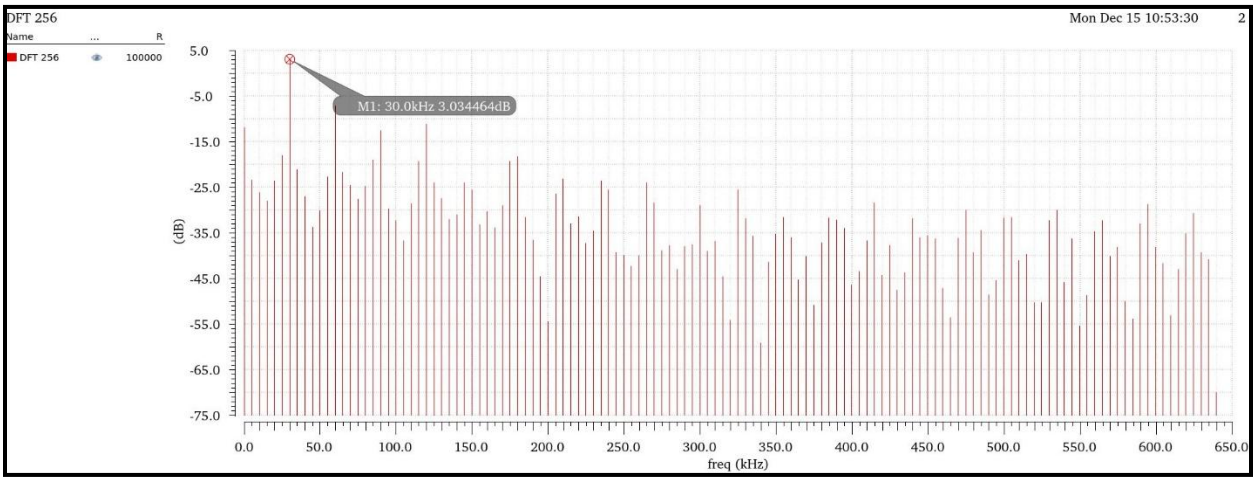


Figure 53: THD at BW = 1KHz and Min Frequency Setting in dB

THD 100K	29.87

Figure 54: DFT at BW 1KHz and Min Frequency Setting in dB

Similar to the previous case, the required frequency is higher than the Op-Amp Bandwidth the higher harmonics are heavily attenuated causing the output frequency (30KHz) to be much less than what is expected (100KHz) and output saturates as the Op-Amp can no longer handle the high slew rate required.

THD is higher as it is measured at a frequency different from the fundamental frequency given to the function similar to previous cases.

Maximum Frequency (10MHz)

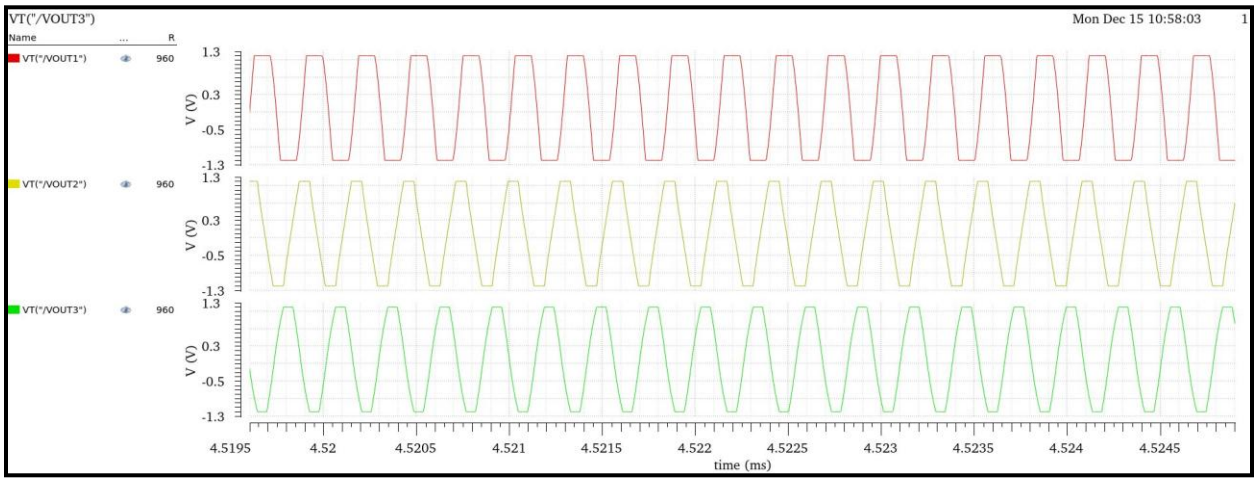


Figure 55: The 3 Outputs at BW 1KHz and Max Frequency Setting

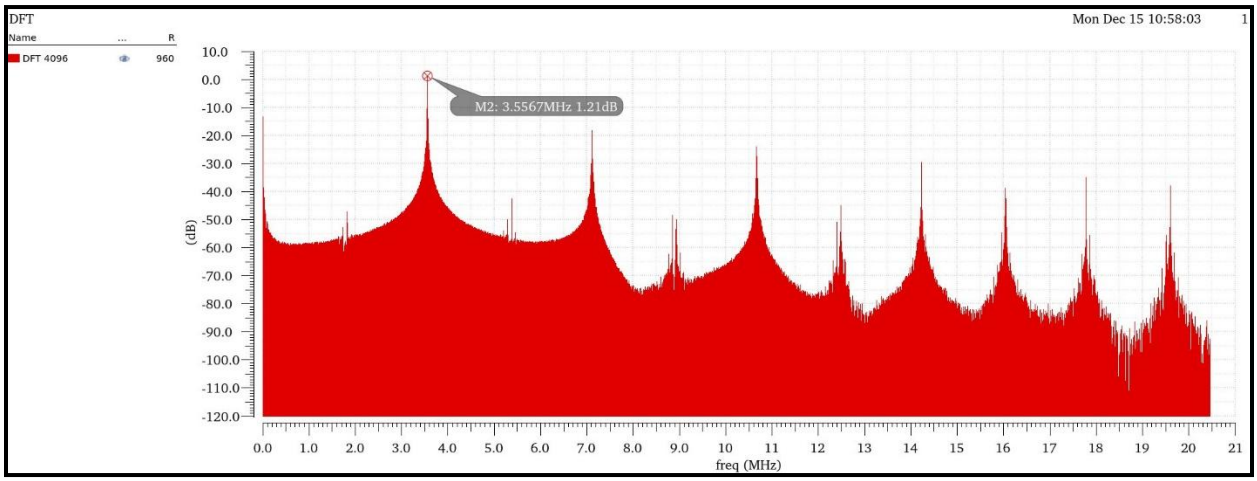


Figure 56: DFT at BW 1MHz and the Max Frequency Setting

THD 10M	68.37

Figure 57: THD of 10MHz sine wave at BW 1KHz and Max Frequency Setting

We notice a similar result in this case to the previous case due to the same reasons, but the additional higher frequency settings required a much higher build up time for the circuit, thus at the beginning it apparently doesn't seem to oscillate until we increase the simulation time we can see oscillations at all the outputs after some time.

A simulation trick we found to avoid this was to add initial conditions on the capacitors at the other two stages to decrease the build up time and view oscillations much faster.

Bonus part

<u>We add a two CMOS inverter stage to act as a buffer output stage to reduce output resistance and act as Op-Amp</u>

<u>Note that this design use the first design of Q1 but we shifted down V_{B2} to positive $300mV$ and V_{B3} to negative 100mV</u>

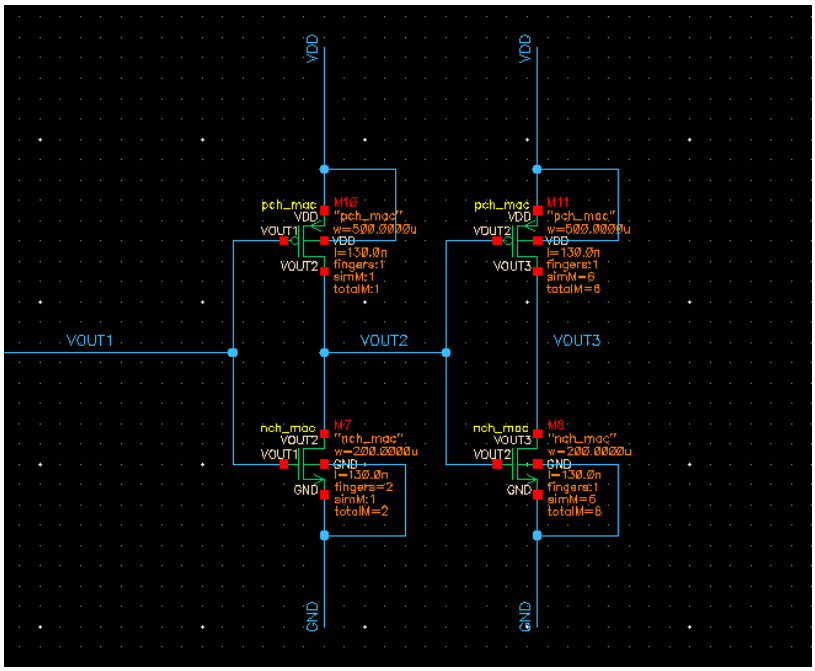


Figure 58: sizing for 2 CMOS inverters output stage

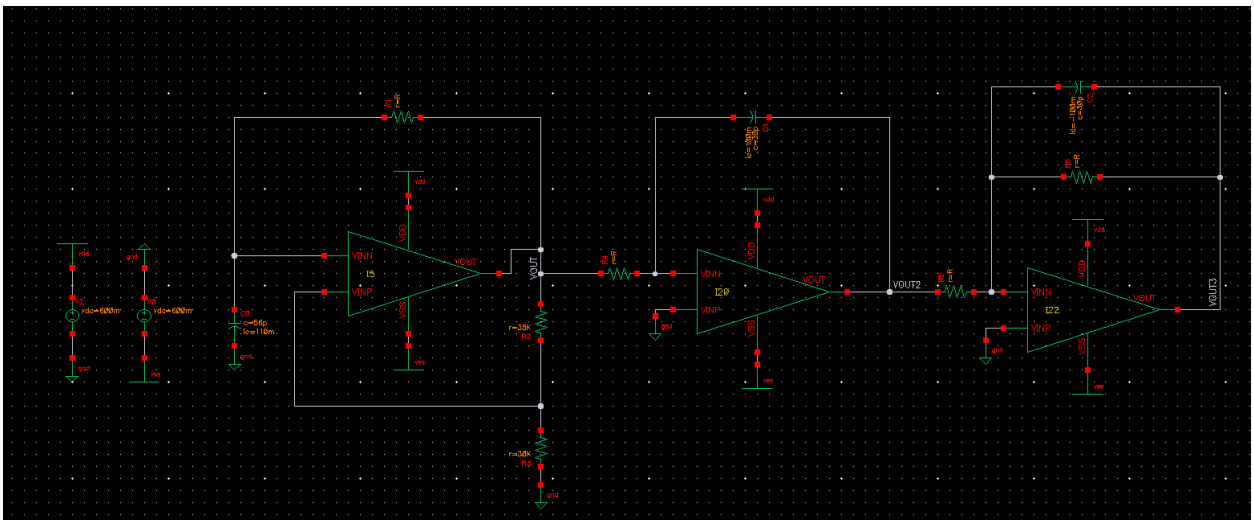


Figure 59: Schematic using real Op-Amp

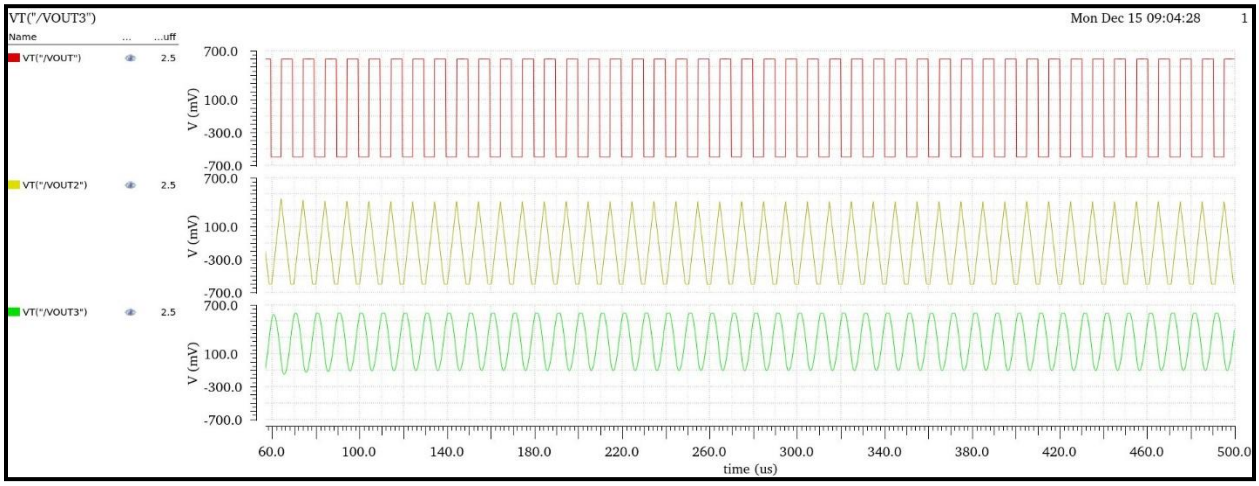


Figure 60: Waveforms of the Three Stages

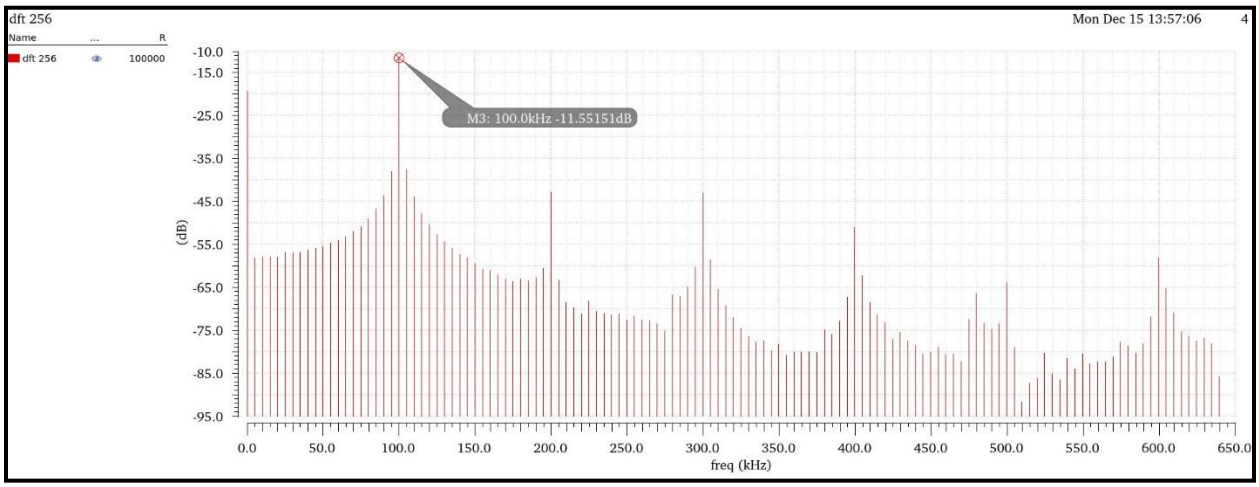


Figure 61: DFT of real Op-Amp

THD 100k	-24.34

Figure 62: THD of real Op-Amp

The usage of a CMOS buffer at the output proved to be the best choice for this OTA. When designed correctly the outputs seem to be as good as the ideal case albeit we can observe it settles at a different DC Level than the zero level like the ideal case or what seems to be an analog level in higher frequencies.

Another design

Note that this design use the second design of Q1

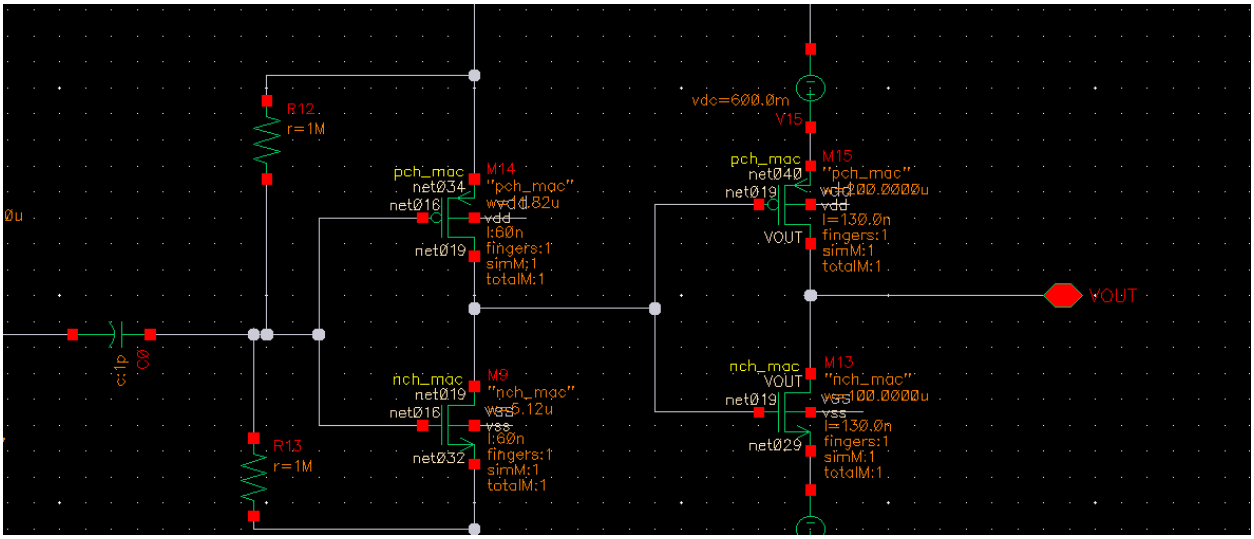


Figure 63: sizing for 2 CMOS inverters output stage

Waveforms of the Three Stages

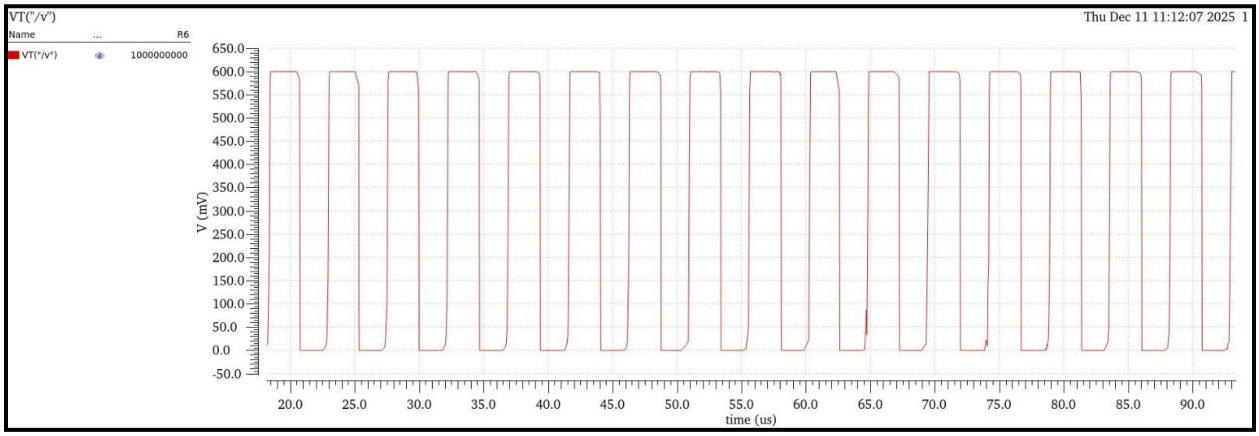


Figure 64: Square wave

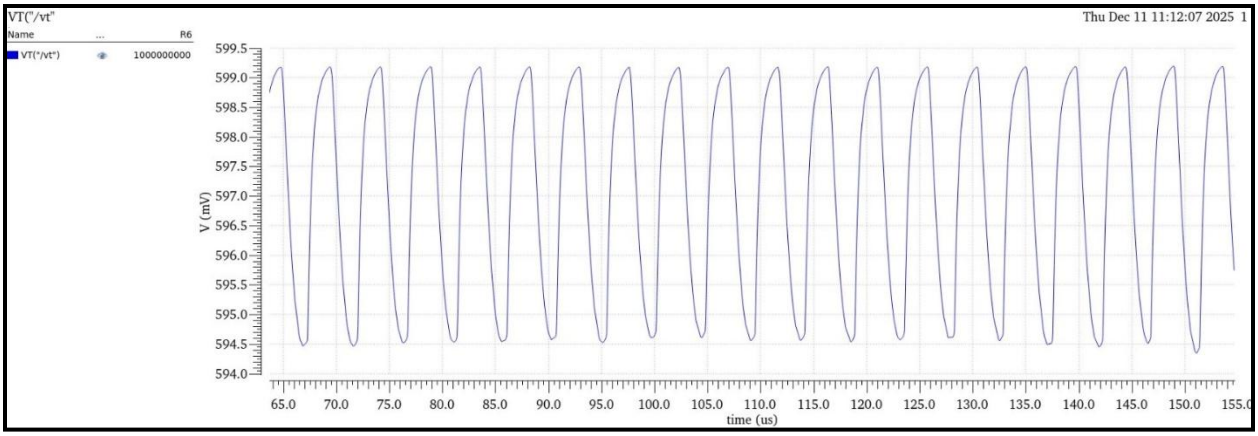


Figure 65: Triangle wave

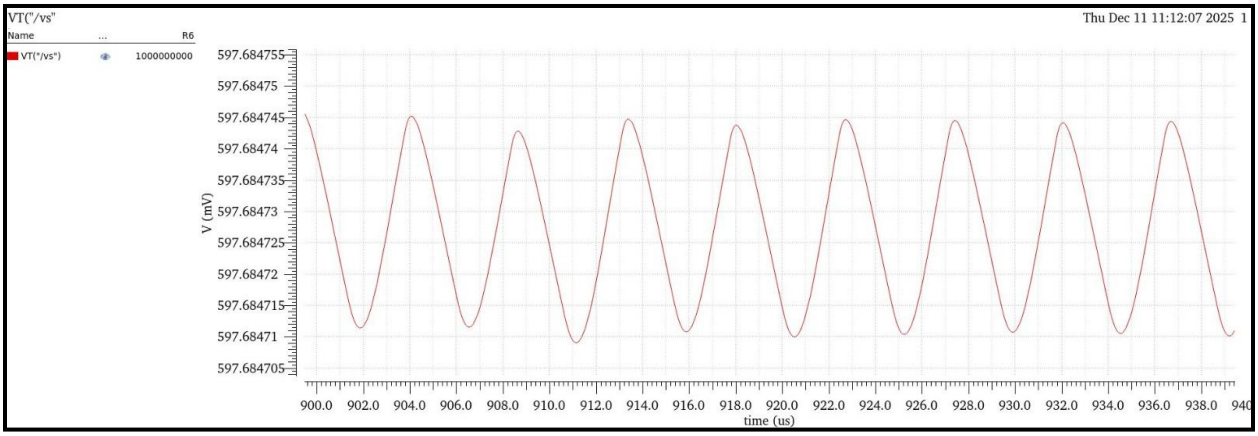


Figure 66: Sinusoidal wave