PIN diodes and switches

Caverly diode model is shown in Figure 1 [1, 2], with parameter description in Table 1:

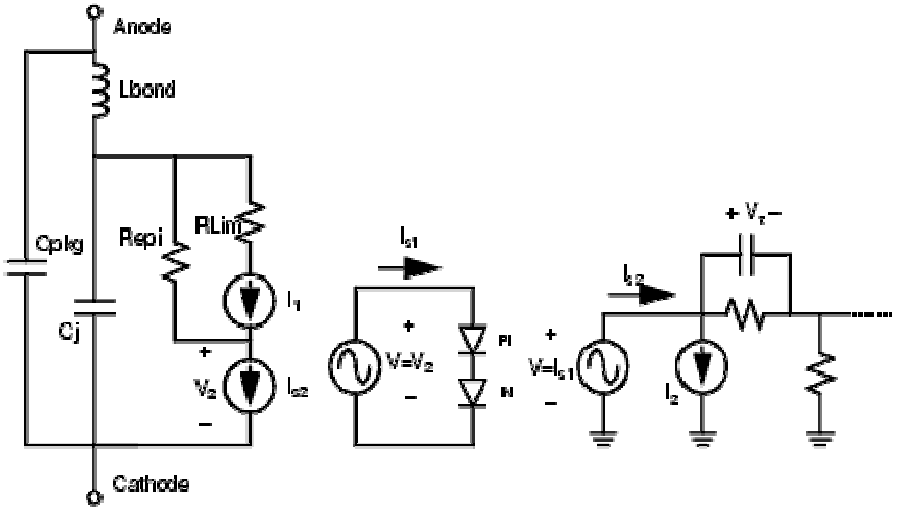


Figure 1

Name	Description	Unit Type	Default
I_S	Reverse saturation current	Current	1e-6 mA
I_{KNEE}	Knee param for current dependent tau	Current	1e6 mA
N	Ideality factor	Scalar	1
R_{LIM}	Minimum series resistance	Resistance	0.001 Ohm
R_{EPI}	Epi leakage resistance	Resistance	1000 Ohm
C_J	Reverse capacitance	Capacitance	0.1 pF
C_{PKG}	Package capacitance	Capacitance	0.1 pF
TAU	Storage time	Time	57 ns
W	I region width in micrometers	None	6.0 µm
B	Ratio of electron to hole mobility	Scalar	3.0
L_{BOND}	Bond wire inductance	Inductance	0.1 nH

Table 1

There are two nonlinear elements in the model, I_1 and I_2. I_1 accounts for the nonlinear series resistance:

$$I_1 = \frac{2 \cdot V_1 \cdot V_\tau}{V_m}$$

Equation 1

$$V_{\mathrm{m}} = \frac{W^2}{0.1 \cdot \tau}$$

Equation 2

I_2 accounts for the current-dependent storage time:

$$I_2 = \frac{V_2^2}{I_{\mathrm{KNEE}}}$$

Equation 3

The voltages V_1, V_2, and V_τ are shown in the figure.

The diodes represent the PI junction and the IN junction. Their current parameters are both I_S, but their ideality factors differ. They are, respectively, N_{PI} and N_{IN}, given by

$$N_{\mathrm{PI}} = \frac{2 \cdot N}{(1+B)}$$

Equation 4

$$N_{\mathrm{IN}} = \frac{2 \cdot N \cdot B}{(1+B)}$$

Equation 5

The resulting I/V characteristic for the complete PIN diode, consisting of the PI and NI junctions in series, is a conventional diode I/V characteristic having the ideality factor

$$N_{\mathrm{PIN}} = N_{\mathrm{PI}} + N_{\mathrm{IN}} = 2 \cdot N$$

Equation 6

Critical parameters for a forward-biased PIN diode are W and τ. W can be found from curves of the RF resistance, R_{d}, as a function of DC current, I_{d}. The relation is:

$$R_d = \frac{W^2}{\mu \cdot \left(1 + \frac{1}{B}\right) \cdot \tau \cdot I_d}$$

Equation 7

$$W = \sqrt{R_d \cdot \mu \cdot \left(1 + \frac{1}{B}\right) \cdot \tau \cdot I_d}$$

Equation 8

where μ = electron mobility ≈ 1200 cm^2/Vs in silicon. In reverse bias, the model treats the junction as a constant capacitance, C_J. A slightly modified version of the Caverly model is given in Appendix 1.

Composing the model for MWO simulation

Avago Technologies surface mount RF PIN switch diode series HSMP-389x is to be used in an AWR Microwave Office simulation. Since Caverly diode model has been identified as the best one to use, required parameters are formulated in this section (see Table 1 for full list).

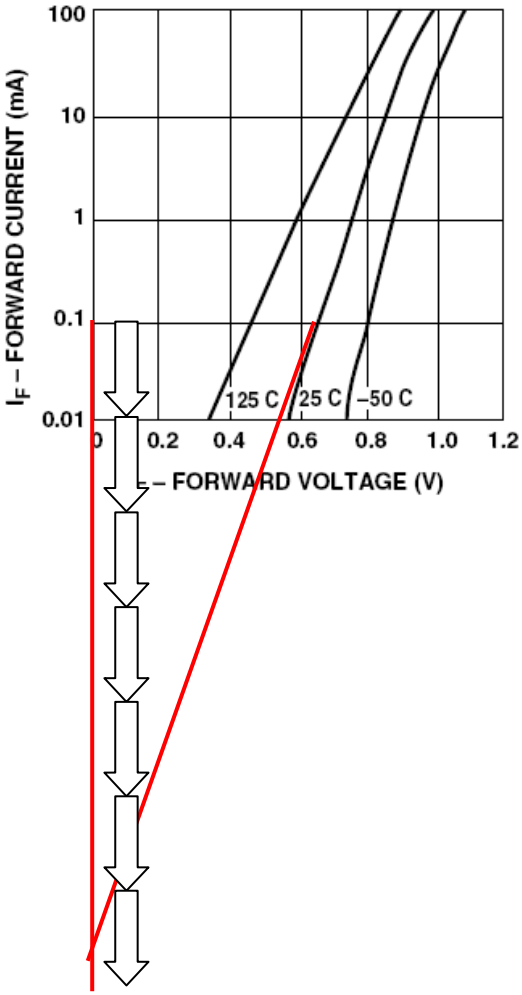
Reverse saturation current, I_S

Diode DC V/I characteristic can be expressed as

$$I(V) = I_S\left(e^{\frac{q \cdot V}{n \cdot k \cdot T}} - 1\right)$$

Equation 9

where *q* is the charge of an electron, *k* is the Boltzmann's constant, *T* is temperature, *n* is the ideality factor, and I_S is the saturation current. With the forward voltage set to 0 V, datasheet graph can be extended to calculate I_S.



Knee parameter for current dependent τ

Since current-dependence is not mentioned, use the default value.

Ideality factor

Ideality factor depends on the diode structure, and can vary from $N = 1.2$ to $N = 2.0$. With the average of $N = 1.6$, we have $N_{PIN} = 2 \cdot N = 3.2$.

Minimum series resistance

For minimum series resistance use $R_S = 3.8\ \Omega$, as quoted for Series Resistance ($I_F = 1$ mA, $f = 100$ MHz).

EPI leakage resistance

As no value is given in the datasheet, use the default value.

Reverse capacitance

Datasheet gives C_T = 0.25 pF (Total Capacitance, 25° C, 5 V), and Maximum Total Capacitance $C_{T,MAX}$ = 0.30 pF (V_R = 5 V, f = 1 MHz). Use the average of these two values: $C_{T,AVG}$ = 0.275 pF.

Package capacitance

Set to zero as above capacitance gives total measured value. Had the measurement been for a die, packaged later on, then C_{PKG} should be used. L_{BOND} should be used if a bond wire is present to connect the die to the track.

Storage time

Use the value given in the data sheet (carrier lifetime), τ = 200 ns (I_F = 10 mA, I_R = 6 mA, T = 25° C).

Intrinsic region width

With Figure 2, and Equation 8:

$$W = \sqrt{R_d \cdot \mu \cdot \left(1 + \frac{1}{B}\right) \cdot \tau \cdot I_d}$$

$$W = \sqrt{0.6 \cdot 0.12 \cdot \left(1 + \frac{1}{3}\right) \cdot 200\,\text{ns} \cdot 100\,\text{mA}} \approx 44\,\mu\text{m}$$

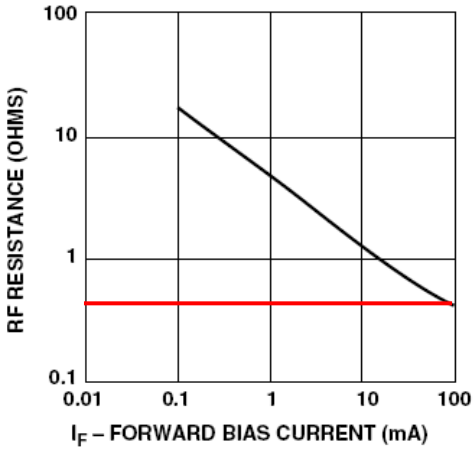


Figure 2

Ratio of electron to hole mobility

Use the default value of B = 3 (for silicon diodes).

Bond wire inductance

Set to zero, as a chip diode is used.

Parameter effect on switch performance

Consider the circuit shown in Figure 3 (zoom in for more detail). Note:

- All transmission lines were for physical accuracy: 50 Ω, 1 mm long.
- All DC block capacitors (circled in solid red) are 100 pF, so that at the centre-band frequency (centre in between Rx and Tx filters) f_c = 947.5 MHz, the rule of thumb is satisfied: $X_c < 2\ \Omega$ (or SRF @ centre frequency), where $X_c = 1/(2 \cdot \pi \cdot f_c \cdot C) = 0.6\ \Omega$.
- All RF choke inductors (circled in dashed red) are 100 nH, so that at the centre-band frequency (centre in between Rx and Tx filters) f_c = 947.5 MHz, the rule of thumb is satisfied: $X_L > 500\ \Omega$, where $X_L = 2 \cdot \pi \cdot f_c \cdot L = 595\ \Omega$.
- Assuming that the control voltages (Vc_1 and Vc_2) are +/- 5 V, resistors R_1 (quantity 2) and R_2 control the biasing of the four diodes, as well as the currents flowing and voltages established.
- Assume that Vc_1 = -5 V and Vc_2 = +5 V. Figure 4 shows circuit voltage and current labels.
- Two instances of R1 are kept at the same value for simplicity (and potential symmetry of the solution).

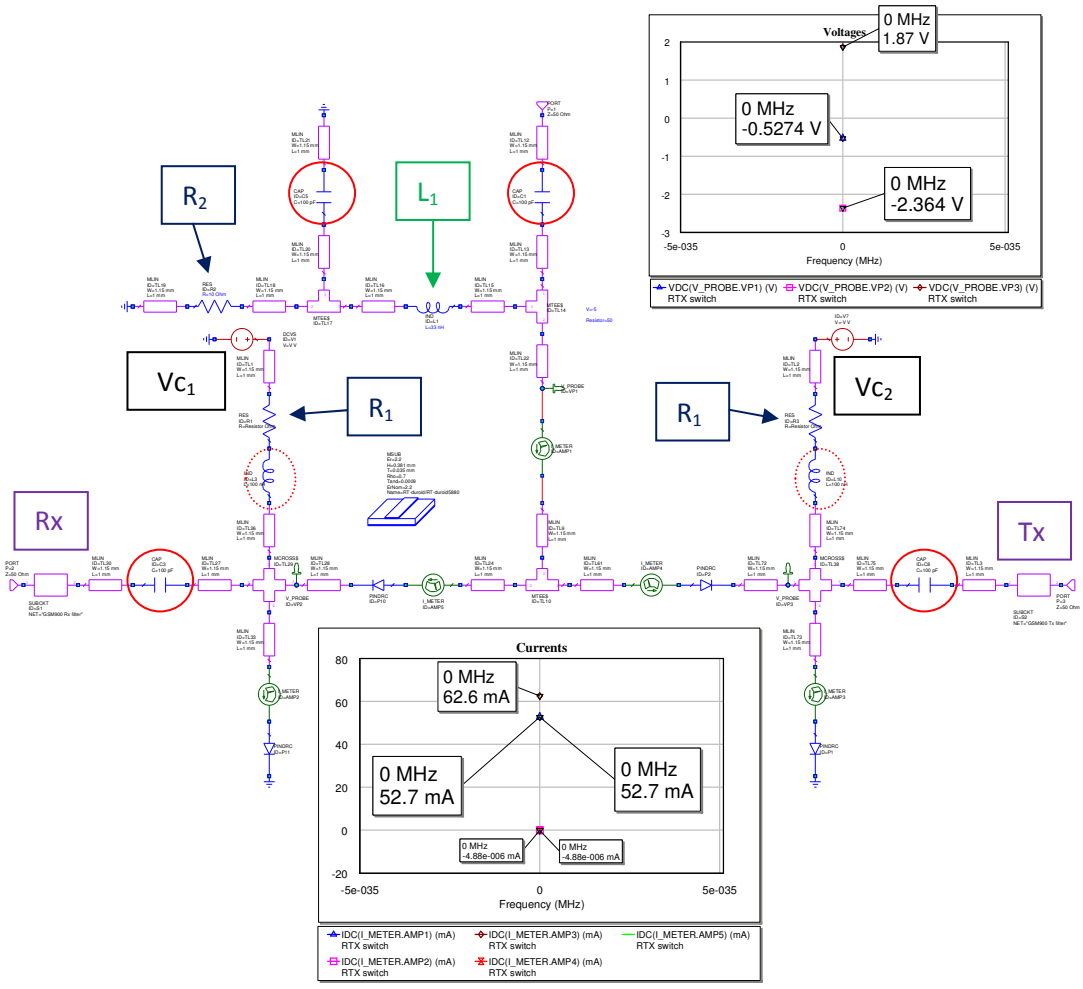

R2
L1
Vc1
R1
R1
Vc2
Rx
Tx
Voltages
0 MHz
1.87 V
0 MHz
-0.5274 V
0 MHz
-2.364 V
Frequency (MHz)
VDC(V_PROBE.VP1) (V)
RTX switch
VDC(V_PROBE.VP2) (V)
RTX switch
VDC(V_PROBE.VP3) (V)
RTX switch
Currents
0 MHz
62.6 mA
0 MHz
52.7 mA
0 MHz
52.7 mA
0 MHz
-4.88e-006 mA
0 MHz
-4.88e-006 mA
Frequency (MHz)
IDC(I_METER.AMP1) (mA)
RTX switch
IDC(I_METER.AMP3) (mA)
RTX switch
IDC(I_METER.AMP5) (mA)
RTX switch
IDC(I_METER.AMP2) (mA)
RTX switch
IDC(I_METER.AMP4) (mA)
RTX switch

Figure 3

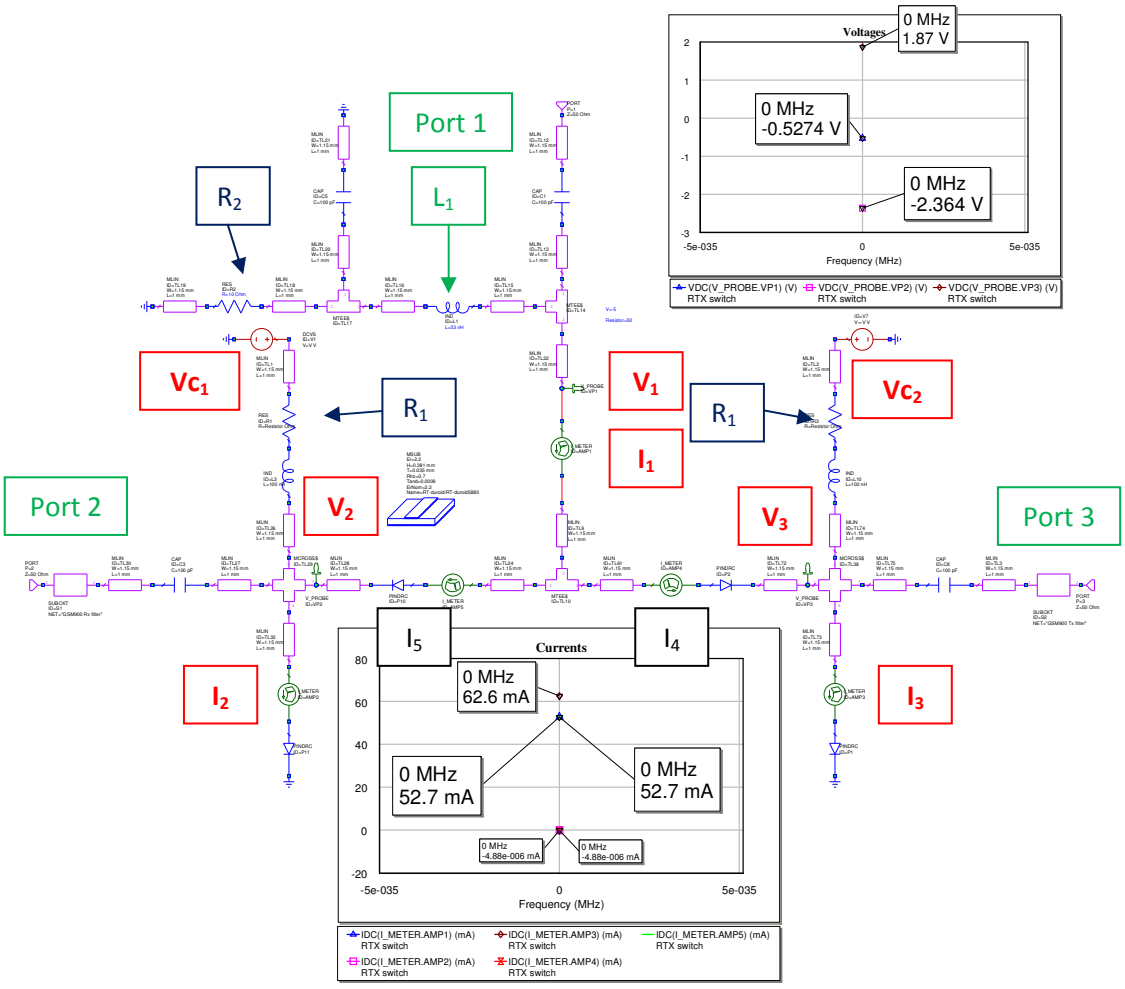


Figure 4

- With Vc2 positive, RHS shunt diode (Diode 3) is forward biased. Voltages and currents developed depend on the value of R1 and the diode IV curve (exponential). By measurement, we see that V3 = 1.87 V and I3 = 62 mA. Since R2 = 50 Ω, we also have (5 V – 1.87 V)/50 Ω = 62.6 mA. Current and voltage developed do not depend only on the value of R1, but also on the diode characteristic. The nonlinear equation has to be solved for every different case.

- With Vc1 negative, LHS shunt diode (Diode 2) is reverse biased. Its non-ground end will be at some negative voltage, the result of R1 and IV characteristic. From measurement we have V2 = -2.364 V and I1 = 0 mA. Current through R1 is then (-5 V + 2.364)/50 = 52.7 mA.

- The common point of LHS series diode (Diode 1) and RHS series diode (Diode 4) are ultimately connected to ground (near R2). Since voltage at the other end of Diode 4 is 1.87 V, Diode 4 will be reverse biased. Similarly, since voltage at the other end of Diode 1 is -2.364 V, Diode 1 is forward biased.

- Current I1 can only go through Diode 1 (forward biased), therefore we must have I1 = I2. With R2 = 10 Ω, V1 can be calculated as 0 V – 52.7 mA * 10 Ω = -0.527 V. This is confirmed by nonlinear simulation.

- We can now also calculate the forward and reverse voltages across each of the four diodes. Diode 1 : -0.527 – -2.364 = 1.84 V. Diode 2 = -2.364 – 0 = -2.364 V. Diode 3 = 1.87 V, Diode 4 = -0.527 – 1.87 V = -2.4 V. Due to symmetric resistor choice, the voltage conditions are also symmetric.

- Voltages across diodes will determine the currents flowing through them. This in turn will determine their RF insertion loss and isolation. In general, the more current the better the insertion loss is. The details can be found out from the particular diode data sheet.

- Ports 2 and 3 are well matched as they look into a DC blocked followed by an ON of OFF PIN diode. Port 1 however has the extra Bias-T-like branch. Therefore L1 was set to 33 nH to control the matching of the both input and output return loss of the ON arm. L1 does not affect the response of the OFF arm.

- Overall RF response is shown below in Figure 5 while the response of the filters by themselves is shown in Figure 6

- Parameter choice discussed here is mainly for illustration purposes, other values could have been used as well to obtain different performance tradeoffs. DC blocks have effectively no effect on RF performance. Changing diode current and voltage has no effect on matching, only on insertion loss and isolation performance of the switch/diodes.

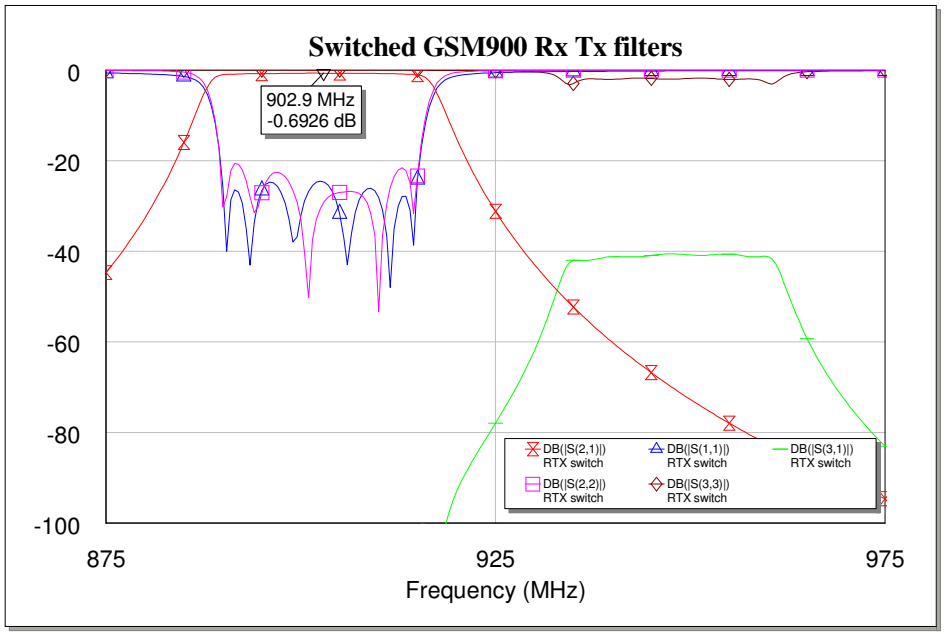


Figure 5

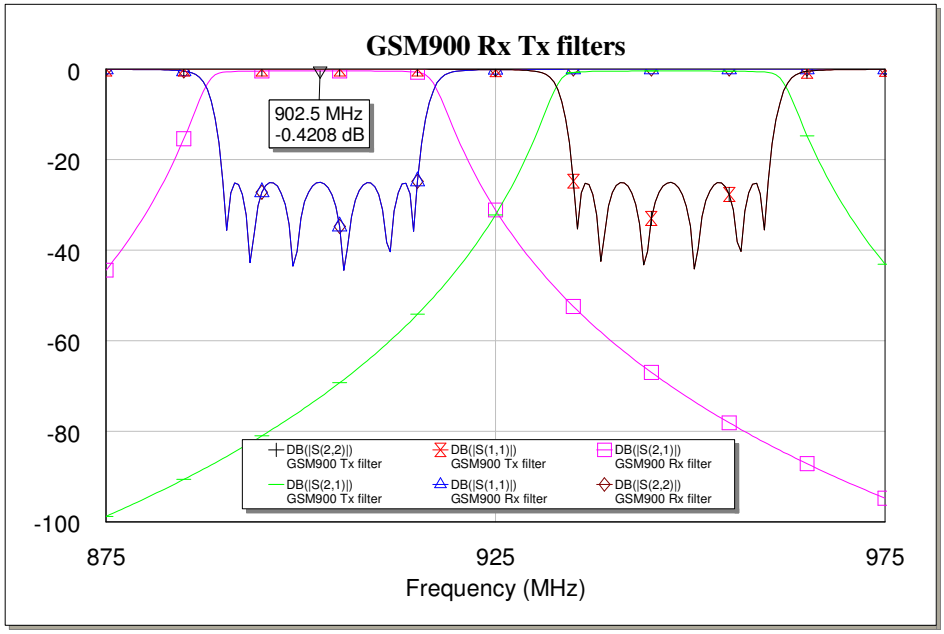


Figure 6

Appendix 1: Improved Caverly model

The same model was also considered by Kyhala and Andersson [3]. They improved it since the junction capacitance in the original model did not depend on bias or frequency, and the operation under reverse bias was not as accurate in simulating the intermodulation products. Model is shown in Figure 7.

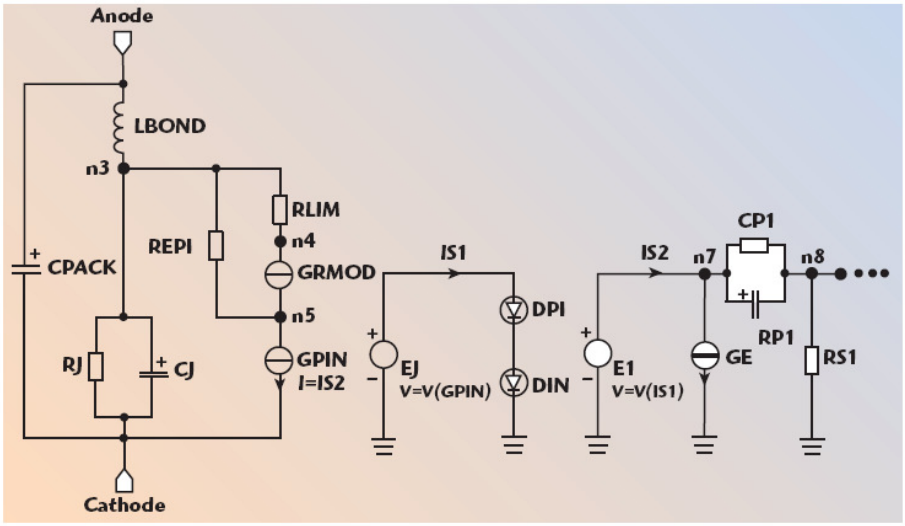


Figure 7

The following are component values:

L_{BOND}: describes package characteristics
C_{PACK}: also describes package characteristics
R_P: junction parallel resistance
R_{EPI}: zero-bias resistance
R_{LIM}: minimum series resistance

Controlled-current sources are described as:

Voltage E_J is equal to the voltage across the current source G_{PIN}.

Voltage E_1 is equal to the value of the current I_{S1}.

Current G_E:

$$\text{Current } G_E = \frac{V(G_E)^2}{I_{KNEE}}$$

$V(G_E)$ is the voltage across the current source G_E and I_{KNEE} is a model parameter (current-dependent lifetime knee current).

For improving model convergence $V(G_E)$ has been limited according to ($\varepsilon = 10^{-12}$):

$$V(G_E)^2 \approx 0.25\left(V(G_E)+\sqrt{V(G_E)^2+4\varepsilon^2}\right)^2$$

Current $G_{PIN} = I_{S2}$.

Current G_{RMOD}:

$$\text{Current } G_{RMOD} = \frac{2 \cdot V(G_{RMOD}) \cdot V(R_{P1})}{V_M}$$

where $V(G_{RMOD})$ is the voltage across the current source G_{RMOD}, $V(R_{P1})$ is the voltage across resistor R_{P1} and

$$V_M = \frac{10 \cdot W^2}{\tau}$$

$V(R_{P1})$ accounts for conductance and should never be negative; it can be approximated by (with $\varepsilon = 10^{-12}$):

$$V(R_{P1})^2 \approx 0.5\left(V(R_{P1})+\sqrt{V(R_{P1})^2+4\varepsilon^2}\right)^2$$

Diodes DPI and DIN are SPICE-compatible diodes with parameters I_S, I_{KF}, N, B_V, I_{BV}, and R_S.

Emission coefficient η for the diodes is calculates as (with B and N as model parameters):

$$\eta(DPI) = \frac{N}{1+B}$$

$$\eta(DIN) = \frac{B \cdot N}{1+B}$$

The value of C_J (without bias dependence) is given as

$$C_J = C_{pt} \frac{1+\left(\frac{f}{f_r}\right)^2}{\frac{C_{pt}}{C_d}+\left(\frac{f}{f_r}\right)^2}$$

where

C_{pt} = parameter C_J for the PIN diode
f_r = dielectric relaxation frequency

The ratio C_{pt}/C_d is equal to the ratio W_d/W, where W_d is the diode depletion area width, and W is the I-region width.

References

[1] AWR Microwave Office 2007 (7.53 build 3723r Rev2) Help.

[2] R. Caverly et al, "Spice Modeling of Microwave and RF Control Diodes," *Midwest Symposium on Circuits and Systems Digest of Papers*, 2000.

[3] J. Kyhala and M. Andersson, "An Advanced PIN-diode Model," *Microwave Journal*, September 2005.

Version history

Version 1 (11 NOV 2008): First release.