Banana Pi BPI-F3 SpacemiT K1 RISC-V chip datasheet

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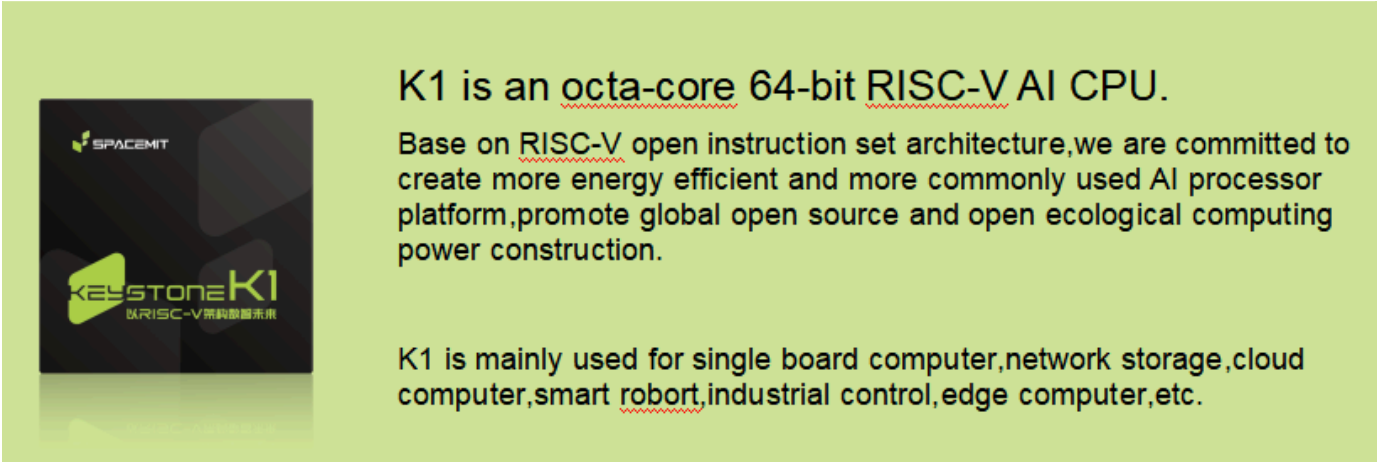
K1 Overview



SpacemiT K1 Open source SBC : Banana Pi BPI-F3

SpacemiT K1 Introduction

SpacemiT® Key StoneTM K1 is a high-performance and ultra low-power cpu that integrates Octa RISC-V cores with SpacemiT® Daoyi™ AI computing power deployment. K1 has the following features:

- Integrates SpacemiT® self-innovate X60™ RISC-V processor core which adheres to the RISC-V 64GCVB architecture and RVA22 standard.
- Extends 2.0TOPS AI computing power by exploring RISC-V customized instructions to realize CPU AI fusion computing power, and mainstream AI inference frameworks such as TensorFlow Lite, TensorFlow, and ONNX RunTime are supported.
- Achieves ultra low power consumption by implementing different granularities of power islands and various levels of power states to make K1 more competitive and the leading edge.
- Supports full-feature interfaces to enrich more innovatative applications and products.
- Compatible with mainstream OS to meet the needs of various application scenarios.
- Meets Industrial grade reliability standards

Feature Overview

- RISC-V Processor
  - -RISC-V SpacemiT® X60™ Dual-cluster Octa-core processors
  - -Adhere to the RISC-V 64GCVB architecture and RVA22 standard
  - -Cluster0

- •Quad-core with 2.0TOPS AI-Power
- •32K L1-Cache per core
- •512K L2-Cache
- •512KB TCM
- •Vector-256bit

- -Cluster1
  - •Quad-core
  - •32K L1-Cache per core
  - •512K L2-Cache
  - •Vector-256bit
- -DVFS with adaptive operating voltage from 0.6V to 1.05V

- DDR Memory
  - -Dual chip select 32-bit LPDDR4/LPDDR4x SDRAM with 2666Mbps operation and a total of up to 16GB of RAM
  - -Dual chip select 32-bit LPDDR3 SDRAM with 1866Mbps operation and a total of up to 4GB of RAM
- RCPU(Real-Time CPU)system
  - -R-I2C (×1)
  - -R-I2S (×2)
  - -R-UART (×2)
  - -R-CAN_FD (×1)
  - -R-IR_RX (×1)
  - -R-PWM (×10)
  - -R-SPI (×1)
- Peripheral Controller
  - -GPIO (×128)
    - •128 pins
    - •Pull-up/pull-down programmable
    - •104x 1.8V IO
    - •24x 1.8V/3.3V IO
  - -UART (×10)
    - •AP/BT/print
  - -I2C (×10)
    - •for camera, G-Sensor/ E-COMPASS/ Proximit-Sensor/ Light-Sensor/Gyro and Fingerprint/NFC, PMIC, touch etc.

- •8x I2C(I2C0/1/7 only for camera)+1x HDMI I2C+1x PWR I2C
- -SPI (×4)
  - •To support both master and slave mode
  - •For IMU, codec etc.
  - •Platform has 4 SPI (1x QSPI, 1x SPI LCD, 2x SPI)
- -USB (×3)
  - •USB 2.0 OTG
  - •USB 2.0 Host
  - •USB 3.0 (combo PCIE PortA)
- -PCIE (×3)
  - •PCIE PortA Gen2x1
  - •PCIE PortB Gen2x2
  - •PCIE PortC Gen2x2
- -GMAC (×2)
  - •10/100/1000 Mbps
  - •RGMII
- -SDIO (×1 for WIFI)
  - •compatible for 4-bit SDIO 3.0 UHS-I protocol, up to SDR104
- -SD (×1 for TF card)
  - •compatible for 4-bit SD 3.0 UHS-I protocol, up to SDR104
- -eMMC (×1)
  - •compatible for 8bit eMMC5.1, up to HS400 (200MHz)
- -MIPI CSI (CSI-2 v1.1) 4 lane(×2)
  - •4 Lane + 4 Lane mode
  - •4 Lane + 2 Lane mode
  - •4 Lane + 2 Lane + 2 Lane mode (triple sensor)
- -MIPI DSI (DSI v1.1) (×1)
  - •4 Lane DSI
- -PWM (×20)
- -CAN-FD (×1)
- -IR-RX (×1)

- Security System
  - -RISC-V PMP Security

- -Secure Boot
- -Secure eFuse 4K bits
- -Cryptographic engine (TRNG/AES/SM2/SM3/SM4/RSA/ECC/SHA2/HMAC)

- Debug System
  - -Two JTAGs for both CPU and MCU subsystem
  - -UARTs
  - -CPU/IO register snapshot after watchdog reboot
- Boot System
  - -Initial cpu boot from SPI-Nand/SPI-NorFlash/eMMC/SD
  - -128KB boot-ROM size
- Aided System
  - -Watchdog design for each CPU/MCU subsystem

Multimedia Features

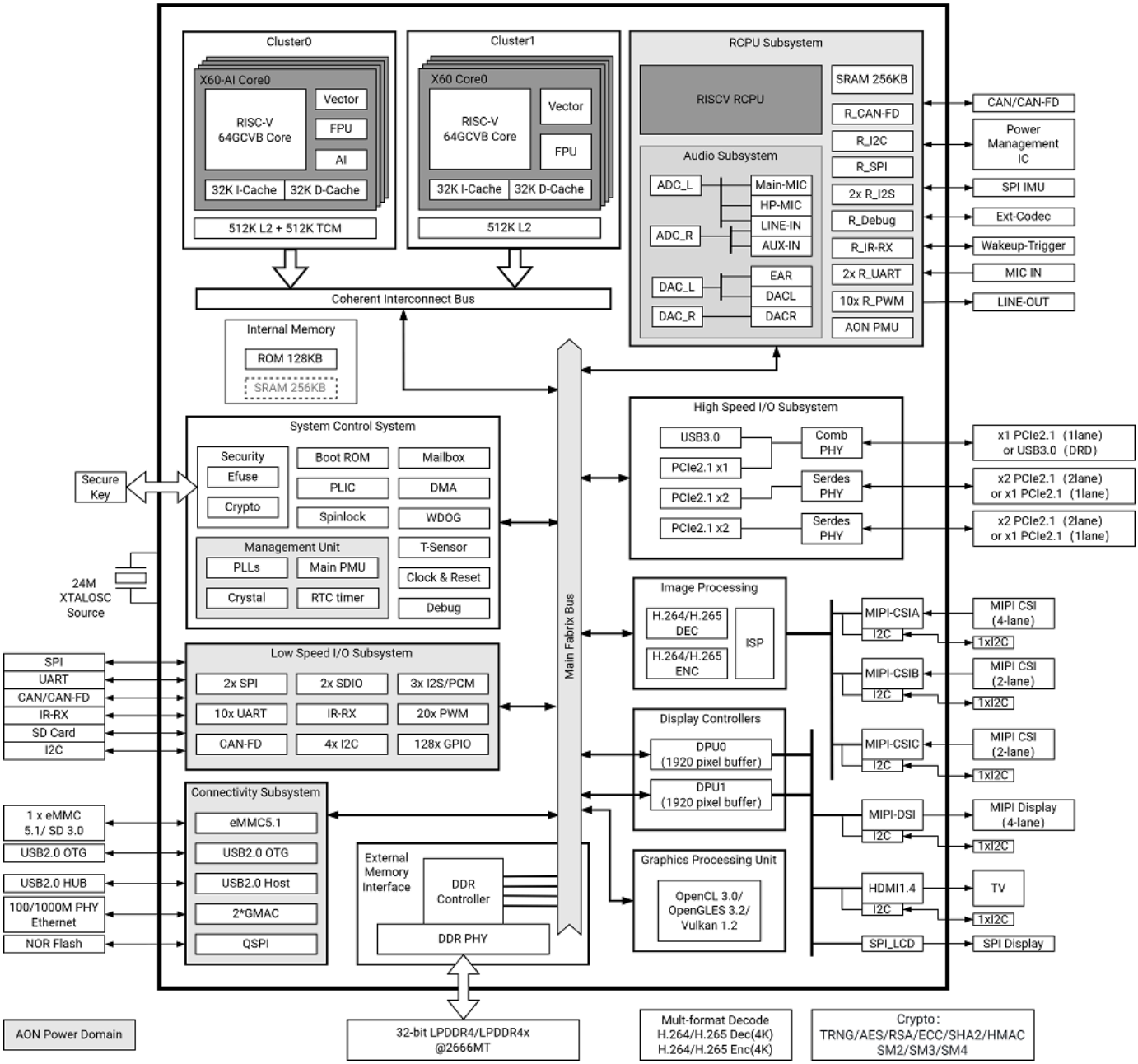
- GPU
  - -IMG BXE-2-32
  - -Support OpenGL ES 3.2
- VPU (video processing unit)
  - -H.265/H.264/VP8/VP9/MPEG4/MPEG2 decoder 4K@60fps
  - -H.265/H.264/VP8/VP9 encoder 4K@30fps
  - -Support simultaneously processing encoding 1080P@60fps and decoding 1080P@60fps
  - -Support simultaneously processing H264/H265 encoding 1080P@30fps and H264/H265 decoding 4K@30fps
- Display
  - -MIPI DSI 4-lane or SPI interface
  - -Support up to HD (1920x1080@60fps)
  - -Support up to 4-full-size-layer composer and maximum 8 layer composer by up-down layer reuse in rdma channel
  - -Support cmdlist mechanism, which can configure register parameters by HW
  - -Support concurrent write back, with both raw and afbc format, also support dither/crop/rotation in write back path
  - -Support advanced mmu (virtual address) mechanism, with nearly no page missing in 90/270 degree
- rotation
  - -Support color key and solid color
  - -Support both advanced error diffusion and pattern based dither for panel

- -Support both afbc/raw format image source
- -Color saturation/contrast enhancement
- -Support both video mode and cmd mode for panel
- -Support ddr frequency dynamic changing with embedded dfc buffer
- -HDMI 1.4

- Camera
  - -Dual-ISP
    - •16M (max.) 30fps Dual ISP
    - •One 4 Lane CSI + one 4 Lane CSI or 4 Lane + 2 lane + 2 lane
    - •RAW sensor, output YUV data to DRAM
    - •Hardware JPEG encoder(hardware, up to 23M is supported)
    - •Support YUV/EXIF/JFIF format
    - •AF/AE/AWB
    - •Face detection
    - •Digital zoom, panorama view
    - •PDAF
    - •PIP (picture in picture)
    - •Support HDR
    - •Continuous video AF
    - •HW 3D denoise
- Audio
  - -Integrated high quality audio codec and audio front-end
    - •ADC: 90dB SNR@20~20kHz
    - •DAC: 95dB SNR@20~20kHz
    - •Class-G: 95dB SNR@20~20kHz, 31mW@32-ohm, THD -90dB
    - •ClassAB: 95dB SNR@20~20kHz, 75mW@32-ohm, THD-90dB
    - •Line-out to support external Class-D audio amplifier (Class-D in PMIC: 95dB SNR@20 ~ 20kHz, 1W@4.2Vbat 10%THD + N, 8-ohm speaker)
  - -Three MICs input
  - -Stereo inputs path for noise cancellation
  - -Stereo headphone output
  - -Audio content sampling rates: 8kHz to 48kHz
  - -Microphone bias for headphone plug-in and hook-key detection
  - -Quad vocoders for adaptive multi-rate (AMR)
  - -Noise suppression and echo cancellation

- General
  - -Operation temperature: -40 ~ 85°C

Block Diagram



Specifications

CPU Subsystem

Overview

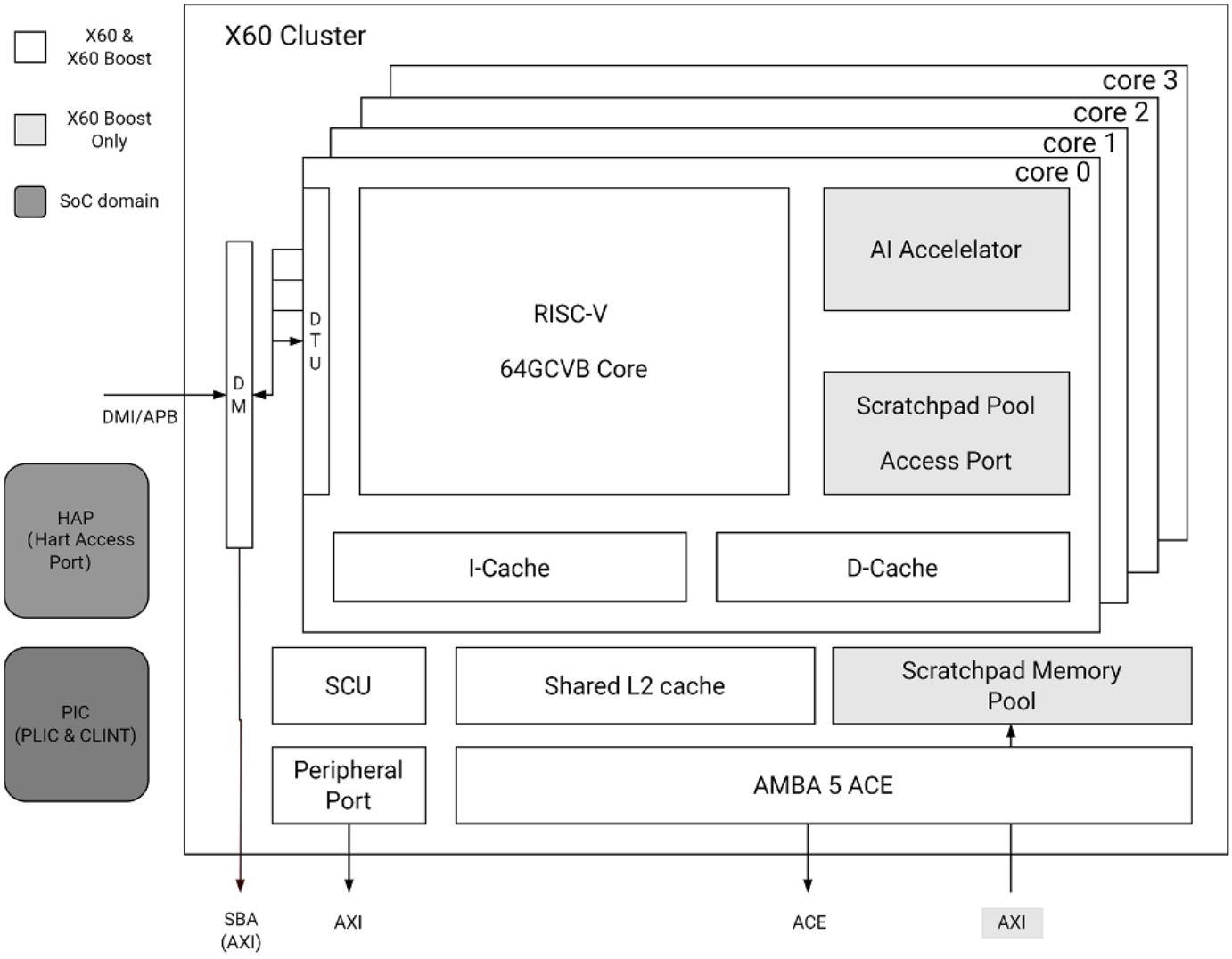
The CPU Subsystem of K1 consists of the following features:

- Two asymmetric CPU Clusters included: Cluster0 integrates Quad RISC-V SpacemiT® X60™Cores with 2.0TOPS AI-Power extension while Cluster1 includes Quad RISC-V SpacemiT® X60™ Cores without AI Capability

- Each High-Performance low-Power SpacemiT® X60™ CPU cores adheres to RISC-V 64GCVB architecture and RVA22 standard
- Support local interrupt controller CLINT and platform interrupt controller PLIC
- Adhere to RISC-V Debug V0.13.2 standard
- CPU critical infomation snapshot taken for debugging when Watchdog reset occurs
- Power-Islands and two-levels power strategies designed for each CPU core and cluster to achieve ultra power savings

SpacemiT® X60™ RISC-V Core

X60™ is an innovative, high-efficiency processor core with SpacemiT® Daoyi™ AI Innovation deployment, and it adheres to RISC-V 64GCVB and RVA22 standards. To meet current and future computational demands, it incorporates numerous DSA technologies and microarchitecture optimizations, and provides robust computing power for AI applications, machine learning, SLAM, ect. X60™ core has the following features:



- RISC-V 64GCVB and RVA22 standards
- Each core has 32KB L1-I Cache and 32KB L1-D Cache
- Each cluster has 512KB L2 Cache
- Cluster0 has 512KB TCM (Tight-Coupled Memory) for AI extention
- L1 Cache supports MESI consistency protocol, L2 Cache supports MOESI consistency protocol
- Vector Extension: RVV1.0/VLEN 256/128-bit x2 execution width

- AI customized instruciton explored and designed in Cluster0
- Support CLINT and PLIC with 256 interrupts in total
- Support RISC-V Performence PMU
- Support SV39 Virtual Memory
- Support 32 PMP entries adhering to RISC-V Security framwork
- Support RISC-V Debug Framework

Interrupt

The Platform Interrupt Controller consists of PLIC and CLINT, shared by two clusters. Exception handling (including exceptions and interrupts) is an important function of the processor, which is used to divert the on-the-fly exceptions to the corresponding core to process them. These events include hardware errors, instruction execution errors, user program requests and external interrupts for services, and so on.

The X60 implements the processor core Local Interrupt Controller (CLINT), a memory address mapped module for handling software interrupts and timer interrupts.

The Platform level Interrupt Controller (PLIC) is used to sample, arbitrate in priority, and then distribute external interrupt sources. In the PLIC model, both the machine mode and the supervisor mode of each core are valid interrupt targets. PLIC supports 256 external interrupt sources. Each interrupt supports both level and edge formats.

Debug and Trace

The debugging interface is the channel through which software interacts with the processor. The user can obtain the information of the CPU register and memory contents, including other on-chip device information, through the debugging interface. In addition, operations such as program downloading can also be done through the debugging interface.

The Debugging system consists of the debugging software, the debugging agent service, the debugger, and the debugging interface. Among those componets, the debugging software and debugging agent service program are interconnected through the network, the debugging agent service program and the debugger are connected through USB, and the debugger communicates with CPU through JTAG interface.

The JTAG memory assess method could be either progbuf or sysbus mode. The progbug mode is a normal JTAG method through CPU while the sysbus is the other method to access the on-chip resources bypassing CPU through SBA (System Bus Access) port.