Hao-Chun Liang

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Education

National Yang Ming Chiao Tung University — Sept. 2025 – Present
Master of Engineering - Institute of Pioneer Semiconductor Innovation | Digital IC Design — *Hsinchu, Taiwan*

National Tsing Hua University — Sept. 2021 – Jun. 2024
Bachelor of Engineering - Electrical Engineering | GPA 4.10/4.30 | Honor Graduation — *Hsinchu, Taiwan*

National Tsing Hua University — Sept. 2020 – Jun. 2021
Bachelor of Science - Physics | Transferred to the Department of Electrical Engineering — *Hsinchu, Taiwan*

Work Experience

Hardware and Algorithm Codevelopment - Affiliate Trainee — Jan. 2025 – Present
Accelerated AI Algorithms for Data-Driven Discovery — *Washington, U.S. (Remote)*

Graduate Research Assistant — Dec. 2024 – Present
National Yang Ming Chiao Tung University | Institute of Pioneer Semiconductor Innovation — *Hsinchu, Taiwan*

AI/Deep Learning Accelerator - Digital Design Intern — Nov. 2024 – Present
Acceleration R&D Division | Andes Technology Corporation — *Hsinchu, Taiwan*

General Physics Experiment Teaching Assistant — Sept. 2023 – Jan. 2024
National Tsing Hua University | College of Science — *Hsinchu, Taiwan*

Awards

Certificate of Outstanding Graduate Award (Top 8% of Class) — Jun. 2024
National Tsing Hua University | Electrical Engineering — *Hsinchu, Taiwan*

College of Science Elite Student Award (1st Place, Freshman Year) — Apr. 2021
National Tsing Hua University | College of Science — *Hsinchu, Taiwan*

Three Presidential Awards (Top 5% Each Semester) — Jun. 2024
National Tsing Hua University — *Hsinchu, Taiwan*

ADFP@TSMC N16 Cell-Based Chip Design Flow — Sep. 2024
Taiwan Semiconductor Research Institute | TSRI — *Hsinchu, Taiwan*

Transformer-Based Natural Language Processing — Dec. 2023
Deep Learning Institute | NVIDIA — *Hsinchu, Taiwan*

Papers

HiGTR: High-Performance FPGA for GNN-Based Track Reconstruction — July. 2025
Taiwan and Japan Conference on Circuits and Systems, TJCAS 2025 — *Second Author*

High-Performance FPGA for GNN-Based Track Reconstruction in HEP — June. 2025
VLSI Design/CAD Symposium 2025 — *Second Author*

Projects

Data-Driven Code Generation for RTL, C, AsciiDoc — Sep. 2025
Acceleration R&D Division | Andes Technology Corporation — *Hsinchu, Taiwan*

RISC-V Five-Stage Pipelined Featuring Stall and Forwarding Control — Jan. 2024
National Tsing Hua University — *Hsinchu, Taiwan*

Tunable Bandgap in Bilayer Graphene Dual-Gate FET Implementation — Nov. 2023
National Tsing Hua University — *Hsinchu, Taiwan*

FPGA-Based Tetris with Basys 3 Artix-7 — Jun. 2023
National Tsing Hua University — *Hsinchu, Taiwan*

High-Speed 128x16-bit ROM Macro with Sub-5ns Access Time — Jan. 2023
National Tsing Hua University — *Hsinchu, Taiwan*

Skills

Programming Languages: Verilog, Python, C/C++, Linux, Git
Design Tools: VCS, Verdi, SpyGlass, DC, PrimeTime, Hspice, Laker, Innovus, Calibre, Virtuoso, Caliber