Hao-Jyun Liang

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Education

National Yang Ming Chiao Tung University Sept. 2025 – Present
Master of Engineering - Institute of Pioneer Semiconductor Innovation | Digital IC Design *Hsinchu, Taiwan*

National Tsing Hua University Sept. 2021 – Jun. 2024
Bachelor of Engineering - Electrical Engineering | GPA 4.10/4.30 | Honor Graduation *Hsinchu, Taiwan*

National Tsing Hua University Sept. 2020 – Jun. 2021
Bachelor of Science - Physics | Transferred to the Department of Electrical Engineering *Hsinchu, Taiwan*

Work Experience

Hardware and Algorithm Codevelopment - Affiliate Trainee Jan. 2025 – Present
Accelerated AI Algorithms for Data-Driven Discovery *Washington, U.S.*

- Optimizing GPU algorithms for particle trajectory reconstruction at the HL-LHC in HEP experiments

Graduate Research Assistant Dec. 2024 – Present
National Yang Ming Chiao Tung University | Institute of Pioneer Semiconductor Innovation *Hsinchu, Taiwan*

- Intelligent computing, hardware-software co-acceleration and architectural design

AI/Deep Learning Accelerator - Digital Design Intern Nov. 2024 – Present
Acceleration R&D Division | Andes Technology Corporation *Hsinchu, Taiwan*

- CPU-related AI and Deep Learning accelerator.

General Physics Experiment Teaching Assistant Sept. 2023 – Jan. 2024
National Tsing Hua University | College of Science *Hsinchu, Taiwan*

- Exams management and demonstrations for general physics experiments.

Awards

Certificate of Outstanding Graduate Award Jun. 2024
National Tsing Hua University *Hsinchu, Taiwan*

- Top eight students in Department of Electrical Engineering at graduation, evidenced by cumulative major GPA

College of Science Elite Student Award Apr. 2021
National Tsing Hua University | College of Science *Hsinchu, Taiwan*

- Top one student in Department of Physics, evidenced by cumulative GPA during an academic year.

Three Presidential Awards Sept. 2020 – Jun. 2024
National Tsing Hua University *Hsinchu, Taiwan*

- Top 5% students in Department of EE and Physics, evidenced by cumulative GPA during semester.

Certificates

(ADFP - TSMC 16nm) Cell-Based Digital Chip Design and Implementation Sep. 2024
Taiwan Semiconductor Research Institute | TSRI *Hsinchu, Taiwan*

- Exploring key aspects of digital circuit design, providing a comprehensive overview of the digital design flow.

Building Transformer-Based Natural Language Processing Applications Dec. 2023
Deep Learning Institute | NVIDIA *Hsinchu, Taiwan*

- Successful development of Transformer-based natural language processing applications.

Projects

RISC-V Five-Stage Pipelined Featuring Stall and Forwarding Control Dec. 2023 – Jan. 2024
National Tsing Hua University *Hsinchu, Taiwan*

- Stall and forward logic are used to address data and control hazards, reducing NOP insertion by the compiler.
- Quicksort is used to compare CPU performance, showcasing the efficiency of hardware hazard control.

Tunable Bandgap in Bilayer Graphene Dual-Gate FET Implementation Mar. 2023 – Nov. 2023
National Tsing Hua University *Hsinchu, Taiwan*

- Bilayer graphene offers a tunable bandgap of up to 250 meV via a real-time external electric field to reduce costs.
- The dual-gate FET was fabricated with PDMS and tested by I-V measurements, showcasing its tunable bandgap.

FPGA-Based Tetris with Basys 3 Artix-7 May. 2023 – Jun. 2023
National Tsing Hua University *Hsinchu, Taiwan*

- Classic Tetris gameplay with custom music, elimination effects, and "T-spin" for an enriched user experience.
- Pre-game menu for player settings and main gameplay interface.

High-Speed 128x16-bit ROM Macro with Sub-5ns Access Time Dec. 2022 – Jan. 2023
National Tsing Hua University *Hsinchu, Taiwan*

- Pre-sim includes five process corners, and post-sim process at TT 25°C with R-C-CC extraction at CIC 0.18um.
- Focusing on balancing area, timing, with access time and power measured during waveform cycles.

Skills

Programming Languages: Verilog, Python, C/C++

Design Tools: VCS, Verdi, SpyGlass, DC, PrimeTime, Hspice, Laker, Innovus, Calibre, Virtuoso, Caliber