

Hao-Chun Liang

[Email](#) | [Linkedin](#) | 0982-955885

EDUCATION

National Yang Ming Chiao Tung University

Sep. 2025 – Jun. 2027 (Exp.)

M.Eng. in Institute of Pioneer Semiconductor Innovation (ICS & EDA Group)

Hsinchu, Taiwan

National Tsing Hua University

Sep. 2020 – Jun. 2024

B.S. in Electrical Engineering | GPA: 4.1/4.3 | Distinction Graduation

Hsinchu, Taiwan

- Transferred from Dept. of Physics (Top 1 of 65; College of Science Elite Student Award).

Coursework: IC Design Lab (A+), VLSI Testing, VLSI Design, Computer Architecture, Deep Learning

WORK EXPERIENCE

Digital IC Design Intern

Nov. 2024 – Aug. 2025

Andes Technology Corporation | Acceleration R&D Division

Hsinchu, Taiwan

Affiliate Trainee (Remote)

Nov. 2024 – Present

A3D3 Institute | University of Washington

Washington, U.S.

Graduate Research Assistant

Sep. 2025 – Jun. 2027 (Exp.)

National Yang Ming Chiao Tung University | Parallel Computing System Laboratory

Hsinchu, Taiwan

AWARDS & CERTIFICATES

Excellent Poster Award

Aug. 2025

Taiwan and Japan Conference on Circuits and Systems (TJCAS)

Kaohsiung, Taiwan

Cell-Based Digital Chip Design and Implementation (ADFP - TSMC 16nm)

Sep. 2024

Taiwan Semiconductor Research Institute (TSRI)

Hsinchu, Taiwan

Distinction Graduation (Top 5% of 116 in Professional Elective GPA)

Jun. 2024

National Tsing Hua University | Electrical Engineering

Hsinchu, Taiwan

College of Science Elite Student Award (Top 1 of 65)

Apr. 2021

National Tsing Hua University | College of Science

Hsinchu, Taiwan

Presidential Award (Received 3 times)

Sep. 2020 – Jun. 2024

National Tsing Hua University

Hsinchu, Taiwan

PUBLICATIONS

Real-Time GPU Kalman-Filter Tracking via Kernel Refactoring and INT8 Surrogates

Fast Machine Learning for Science Conference 2025, CERN | First Author

An Integrated FPGA Implementation of Complete GNN-Based Trajectory Reconstruction

Taiwan and Japan Conference on Circuits and Systems (TJCAS) 2025 | Second Author

A High-Performance Implementation of GNN-Based Trajectory Reconstruction on FPGA

VLSI Design/CAD Symposium 2025 | Second Author

Fine-Grained Image Recognition from Scratch with Teacher-Guided Data Augmentation

arXiv | Fifth Author

PROJECTS

Regfile Automatic Code Generation

Nov. 2024 – Aug. 2025

Andes Technology Corporation

Hsinchu, Taiwan

CUDA Pipeline Optimization for Particle Tracking at HL-LHC

Nov. 2024 – Present

A3D3 Institute | University of Washington

Washington, U.S.

UltraLightweight HDC-CNN for NeurIPS 2025 Weak Lensing Challenge

Oct. 2025 – Nov. 2025

NeurIPS FAIR Universe Challenge

Top-20 Ranking

NVIDIA NSYS/NCU Profile and Analysis of Token Reduction for ViT

Oct. 2025 – Nov. 2025

National Yang Ming Chiao Tung University | Parallel Computing System Laboratory

Hsinchu, Taiwan

SKILLS

Programming Languages: Python, C/C++, Verilog/SystemVerilog, HLS, CUDA, Perl, Shell

Domains: Efficient Machine Learning, Computer Architecture, Digital IC Design, RTL/C++ Codegen