Hao-Chun Liang

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RESEARCH INTERESTS

AI hardware–algorithm co-optimization; Efficient machine learning; FPGA architectures; GPU computing; Heterogeneous systems

EDUCATION

National Tsing Hua University, Hsinchu, Taiwan — September 2021 – June 2024
B.Sc. in Electrical Engineering, GPA: 4.10/4.30

National Yang Ming Chiao Tung University, Hsinchu, Taiwan — September 2025 – June 2027 (expected)
M.Sc. Candidate, Institute of Pioneer Semiconductor Innovation

ACADEMIC EXPERIENCE

Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
Research Assistant — November 2024 – Present

- Draft manuscripts and prepare figures for journal and conference submissions
- Participate in machine learning and digital IC design competitions
- Optimize high-level trigger systems for GPU-based trajectory reconstruction
- Coordinate weekly internal and external research meetings

Physics Department, National Tsing Hua University, Hsinchu, Taiwan
Teaching Assistant, General Physics Laboratory — September 2023 – January 2024

- Prepared quizzes, midterm, and final exam materials
- Guided students through laboratory experiments and ensured protocol compliance
- Evaluated lab reports, quizzes, and examinations

PROJECTS

RISC-V Five-Stage Processor on 32-Bit Integer ISA, Team Leader — December 2023 – January 2024

- Led timing optimization and stall/forward control-path implementation
- Executed full digital VLSI design flow across IF, ID, EXE, MEM, and WB pipeline stages
- Achieved 54% latency improvement with a 24% trade-off in performance on quicksort benchmark

Tetris System on Basys 3 Artix-7 FPGA Boards, Team Leader — May 2023 – June 2023

- Architected control/data-path separation with AXI interconnect under LUT, BRAM, and DSP constraints
- Implemented T-spin features and VGA output for full gameplay support

Custom High-Speed 128×16-bit ROM Macro, Team Leader — December 2022 – January 2023

- Designed control logic, X/Y decoders, pre-charge circuits, SRAM array, sense amplifiers, and multiplexers
- Achieved sub-5 ns access time in pre-simulation across process-voltage-temperature corners
- Validated sub-10 ns access at TT corner, 25 °C, in post-simulation

Bilayer Graphene Dual-Gate FET Manufacturing, Team Leader — March 2023 – November 2023

- Demonstrated tunable bandgap up to 250 meV via external electric field application
- Fabricated dual-gate FET using PDMS substrate and characterized performance through I–V measurements

SELECTED COURSEWORK

Master's Level

- IC Design Laboratory (A+)
- VLSI Testing (A+)
- Machine Learning (A)
- Data Structures (A+)

Bachelor's Level

- FPGA Laboratory (A)
- Digital Communication (A+)
- Computer Architecture (A-)
- VLSI (A)

AWARDS

Outstanding Graduate Award, National Tsing Hua University June 2024
College of Science Elite Student Award, National Tsing Hua University April 2021
Presidential Awards (Three Times), National Tsing Hua University Sep. 2020 – June 2024
Certificate in Cell-Based Digital Chip Design (ADFP TSMC 16nm), TSRI September 2024
Certificate in Transformer-Based NLP Applications, NVIDIA December 2023

PROFESSIONAL EXPERIENCE

AI/Deep Learning Accelerator Digital Design Intern, Andes Technology, Taipei, Taiwan November 2024 – Present

SKILLS

- **Programming:** Python, Perl, Verilog, C/C++
- **Tools & Frameworks:** Linux, Git, Vivado, ModelSim, MATLAB, TCL