

Hao-Chun Liang

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EDUCATION

National Yang Ming Chiao Tung University <i>M.Eng. in Institute of Pioneer Semiconductor Innovation (ICS & EDA Group)</i>	Sep. 2025 – Jun. 2027 (Exp.) <i>Hsinchu, Taiwan</i>
National Tsing Hua University <i>B.S. in Electrical Engineering GPA: 4.1/4.3 Distinction Graduation</i>	Sep. 2021 – Jun. 2024 <i>Hsinchu, Taiwan</i>
National Tsing Hua University <i>B.S. in Physics Transferred to EE (Top 1 of 65; Elite Student Award)</i>	Sep. 2020 – Jun. 2021 <i>Hsinchu, Taiwan</i>
Coursework: IC Design Lab (A+), VLSI Testing, VLSI Design, Computer Architecture, Deep Learning	

WORK EXPERIENCE

Digital IC Design Intern <i>Andes Technology Corporation Acceleration R&D Division</i>	Nov. 2024 – Aug. 2025 <i>Hsinchu, Taiwan</i>
Affiliate Trainee (Remote) <i>A3D3 Institute University of Washington</i>	Nov. 2024 – Present <i>Washington, U.S.</i>
Graduate Research Assistant <i>National Yang Ming Chiao Tung University Parallel Computing System Laboratory</i>	Sep. 2025 – Jun. 2027 (Exp.) <i>Hsinchu, Taiwan</i>

AWARDS & CERTIFICATES

Excellent Poster Award <i>Taiwan and Japan Conference on Circuits and Systems (TJCAS)</i>	Aug. 2025 <i>Kaohsiung, Taiwan</i>
Cell-Based Digital Chip Design and Implementation (ADFP - TSMC 16nm) <i>Taiwan Semiconductor Research Institute (TSRI)</i>	Sep. 2024 <i>Hsinchu, Taiwan</i>
Distinction Graduation (Top 5% of 116 in Professional Elective GPA) <i>National Tsing Hua University Electrical Engineering</i>	Jun. 2024 <i>Hsinchu, Taiwan</i>
College of Science Elite Student Award (Top 1 of 65) <i>National Tsing Hua University College of Science</i>	Apr. 2021 <i>Hsinchu, Taiwan</i>

PUBLICATIONS

Real-Time GPU Kalman-Filter Tracking via Kernel Refactoring and INT8 Surrogates <i>Fast Machine Learning for Science Conference 2025, CERN First Author</i>	
An Integrated FPGA Implementation of Complete GNN-Based Trajectory Reconstruction <i>Taiwan and Japan Conference on Circuits and Systems (TJCAS) 2025 Second Author</i>	
A High-Performance Implementation of GNN-Based Trajectory Reconstruction on FPGA <i>VLSI Design/CAD Symposium 2025 Second Author</i>	
Fine-Grained Image Recognition from Scratch with Teacher-Guided Data Augmentation <i>arXiv Fifth Author</i>	

PROJECTS

Regfile Automatic Code Generation <i>Andes Technology Corporation</i>	Nov. 2024 – Aug. 2025 <i>Hsinchu, Taiwan</i>
CUDA Pipeline Optimization for Particle Tracking at HL-LHC <i>A3D3 Institute University of Washington</i>	Nov. 2024 – Present <i>Washington, U.S.</i>
UltraLightweight HDC-CNN for NeurIPS 2025 Weak Lensing Challenge <i>NeurIPS FAIR Universe Challenge</i>	Oct. 2025 – Nov. 2025 <i>Top-20 Ranking</i>
NVIDIA NSYS/NCU Profile and Analysis of Token Reduction for ViT <i>National Yang Ming Chiao Tung University Parallel Computing System Laboratory</i>	Oct. 2025 – Nov. 2025 <i>Hsinchu, Taiwan</i>

SKILLS

Programming Languages: Python, C/C++, Verilog/SystemVerilog, HLS, CUDA, Perl, Shell
Domains: Efficient Machine Learning, Computer Architecture, Digital IC Design, RTL/C++ Codegen