

# Hao-Chun Liang

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## EDUCATION

<b>National Yang Ming Chiao Tung University</b> <i>M.Eng. in Institute of Pioneer Semiconductor Innovation (ICS &amp; EDA Group)</i>	Sep. 2025 – Jun. 2027 (Exp.) <i>Hsinchu, Taiwan</i>
<b>National Tsing Hua University</b> <i>B.S. in Electrical Engineering   GPA: 4.1/4.3   Distinction Graduation</i> <ul style="list-style-type: none"><li>Transferred from Dept. of Physics (Top 1 of 65; College of Science Elite Student Award).</li></ul>	Sep. 2020 – Jun. 2024 <i>Hsinchu, Taiwan</i>

**Coursework:** IC Design Lab (A+), VLSI Testing, VLSI Design, Computer Architecture, Deep Learning

## WORK EXPERIENCE

<b>Digital IC Design Intern</b> <i>Andes Technology Corporation   Acceleration R&amp;D Division</i>	Nov. 2024 – Aug. 2025 <i>Hsinchu, Taiwan</i>
<b>Affiliate Trainee (Remote)</b> <i>A3D3 Institute   University of Washington</i>	Nov. 2024 – Present <i>Washington, U.S.</i>
<b>Graduate Research Assistant</b> <i>National Yang Ming Chiao Tung University   Parallel Computing System Laboratory</i>	Sep. 2025 – Jun. 2027 (Exp.) <i>Hsinchu, Taiwan</i>

## AWARDS & CERTIFICATES

<b>Elite New Graduate Scholarship</b> <i>Industry Academia Innovation School, NYCU</i>	Dec. 2025 <i>Hsinchu, Taiwan</i>
<b>Excellent Poster Award</b> <i>Taiwan and Japan Conference on Circuits and Systems (TJCAS)</i>	Aug. 2025 <i>Kaohsiung, Taiwan</i>
<b>Cell-Based Digital Chip Design and Implementation (ADFP - TSMC 16nm)</b> <i>Taiwan Semiconductor Research Institute (TSRI)</i>	Sep. 2024 <i>Hsinchu, Taiwan</i>
<b>Distinction Graduation (Top 5% of 116 in Professional Elective GPA)</b> <i>National Tsing Hua University   Electrical Engineering</i>	Jun. 2024 <i>Hsinchu, Taiwan</i>
<b>College of Science Elite Student Award (Top 1 of 65)</b> <i>National Tsing Hua University   College of Science</i>	Apr. 2021 <i>Hsinchu, Taiwan</i>
<b>Presidential Award (Received 3 times)</b> <i>National Tsing Hua University</i>	Sep. 2020 – Jun. 2024 <i>Hsinchu, Taiwan</i>

## PUBLICATIONS

<b>Real-Time GPU Kalman-Filter Tracking via Kernel Refactoring and INT8 Surrogates</b> <i>Fast Machine Learning for Science Conference 2025, CERN   First Author</i>
<b>An Integrated FPGA Implementation of Complete GNN-Based Trajectory Reconstruction</b> <i>Taiwan and Japan Conference on Circuits and Systems (TJCAS) 2025   Second Author</i>
<b>A High-Performance Implementation of GNN-Based Trajectory Reconstruction on FPGA</b> <i>VLSI Design/CAD Symposium 2025   Second Author</i>
<b>Fine-Grained Image Recognition from Scratch with Teacher-Guided Data Augmentation</b> <i>arXiv   Fifth Author</i>

## PROJECTS

<b>Regfile Automatic Code Generation</b> <i>Andes Technology Corporation</i>	Nov. 2024 – Aug. 2025 <i>Hsinchu, Taiwan</i>
<b>CUDA Pipeline Optimization for Particle Tracking at HL-LHC</b> <i>A3D3 Institute   University of Washington</i>	Nov. 2024 – Present <i>Washington, U.S.</i>
<b>UltraLightweight HDC-CNN for NeurIPS 2025 Weak Lensing Challenge</b> <i>NeurIPS FAIR Universe Challenge</i>	Oct. 2025 – Nov. 2025 <i>Top-20 Ranking</i>
<b>NVIDIA NSYS/NCU Profile and Analysis of Token Reduction for ViT</b> <i>National Yang Ming Chiao Tung University   Parallel Computing System Laboratory</i>	Oct. 2025 – Nov. 2025 <i>Hsinchu, Taiwan</i>
<b>RISC-V 5-Stage Pipelined CPU Core</b> <i>National Tsing Hua University</i>	Dec. 2023 – Jan. 2024 <i>Hsinchu, Taiwan</i>

## SKILLS

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**Programming Languages:** Python, C/C++, Verilog/SystemVerilog, HLS, CUDA, Perl, Shell

**Domains:** Efficient Machine Learning, Computer Architecture, Digital IC Design, RTL/C++ Codegen