1. Consider a simple single cycle implementation of MIPS ISA. The operation times for the major functional components for this machine are as follows:

Component	Latency
ALU	10 ns
Adder	8 ns
ALU Control Unit	2 ns
Shifter	3 ns
Control Unit/ROM	4 ns
Sign/zero extender	3 ns
2-1 MUX	2 ns
Memory (read/write) (instruction or data)	15 ns
PC Register (read action)	1 ns
PC Register (write action)	1 ns
Register file (read action)	7 ns
Register file (write action)	5 ns
Logic (1 or more levels of gates)	1 ns

(Part A)

In the table below, indicate the components that determine the critical path for the respective instruction, in the order that the critical path occurs. If a component is used, but not part of the critical path of the instruction (ie happens in parallel with another component), it should not be in the table. The register file is used for reading and for writing; it will appear twice for some instructions. All instruction begin by reading the PC register with a latency of 2ns.

Instruction Type	Hardware Elements Used By Instruction											
R-Format												
Load												
Store												

(Part B)

Place the latencies of the components that you have decided for the critical path of each instruction in the table below. Compute the sum of each of the component latencies for each instruction.

Instruction Type	Hardware Latencies For Respective Elements											Total
R-Format	2 ns											
Load	2 ns											
Store	2 ns											

(Part C)

Use the total latency column to derive the following critical path information:

- Given the data path latencies above, which instruction determines the overall machine critical path (latency)?
- What will be the resultant clock cycle time of the machine based on the critical path instruction?
- What frequency will the machine run?