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COE 0147 – Lab 7 Work

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**Part 1 -**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Input |  |  |  | Output |  |
| A | B | C | D | X1 | X2 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X1**  CD  AB | 00 | 01 | 11 | 10 |  | **X0**  CD  AB | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |  | 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |  | 01 | 1 | 0 | 0 | 1 |
| 11 | 1 | 1 | 1 | 1 |  | 11 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 1 | 0 |  | 10 | 1 | 0 | 0 | 1 |

= AB + BD + AD

= A ⊕ (B ⊕ D)

**Part 2 –**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input |  |  |  |  |  | Output |  |  |
| A | B | C | D | T | P | X2 | X1 | X0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 2 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 2 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 2 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 3 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 2 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 2 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 2 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 3 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 3 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 4 | 0 | 1 | 0 | 0 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X2**  CD  AB | 00 | 01 | 11 | 10 |  | **X1**  CD  AB | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |  | 00 | 0 | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | 0 |  | 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | 1 | 1 | 1 |  | 11 | 1 | 0 | 0 | 0 |
| 10 | 0 | 0 | 1 | 0 |  | 10 | 1 | 1 | 0 | 1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **X0**  CD  AB | 00 | 01 | 11 | 10 |  |
| 00 | 0 | 0 | 0 | 0 |  |
| 01 | 0 | 0 | 0 | 0 |  |
| 11 | 0 | 0 | 0 | 0 |  |
| 10 | 0 | 0 | 0 | 0 |  |

= 0

**Practice Problems –**



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction Type | Hardware Elements Used By Instruction | | | | | | |
| R-Format | PC read | Instruction memory | Read register | MUX | ALU | MUX | Write register |
| Load | PC read | Instruction memory | Read register | ALU | Memory read | MUX | Write register |
| Store | PC read | Instruction memory | Read register | ALU | Memory write |  |  |

For all three, it was determined that the “control unit/ALU control” would be updated in parallel with the “read register” hardware elements. Since the controllers only take a cumulative 12 ns and the read register takes 15 ns, it was determined that the read register step was the critical path step. The same goes for the adder and sign extenders. The paths listed above are the longest steps associated with each instruction type.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction Type | Hardware Elements Used By Instruction | | | | | | | Total |
| R-Format | 2 | 15 | 7 | 2 | 10 | 2 | 5 | 43 ns |
| Load | 2 | 15 | 7 | 10 | 15 | 2 | 5 | 56 ns |
| Store | 2 | 15 | 7 | 10 | 15 |  |  | 49 ns |

* 1. The **load** instruction determines the overall machine critical path because it takes the longest.  
     The resultant clock cycle time will be **56 ns**.  
     The resultant frequency will be 1/56ns or **17.86 MHz**.