MT793X IoT SDK for Audio User Guide

Version: 1.2

Release date: 2021-11-18

Use of this document and any information contained therein is subject to the terms and conditions set forth in Exhibit 1. This document is subject to change without notice.

Version History

Version	Date	Author	Description
0.1	2021-04-29	Xuan xu	Initial draft
1.0	2021-04-29	Xuan xu	First official release
1.1	2021-07-30	Xuan xu	Add audio interface info
1.2	2021-11-18	Jason Chang	Add quick start

Table of Contents

List of Figures

1 Quick Start

1.1 Voice Assistant test

In this chapter, we provide a simple way to test the voice assistant and assume the project demo image has been burned to the device. For more details, please refer to MT793X IoT SDK for Hands on Training document.

User can get audio response from MT7933 by saying trigger word and command word, the procedure will be introduced in next section.

1.2 Set up the reference board

1. Change jumper **J24** and **J6** to switch speaker mode
2. Connect Audio cable
3. Plug in Micro USB CON8 for supplying 5V power and FTDI debug board for CM33 UART communication
4. After finishing step 3, the reference board will be power on and LED will light up

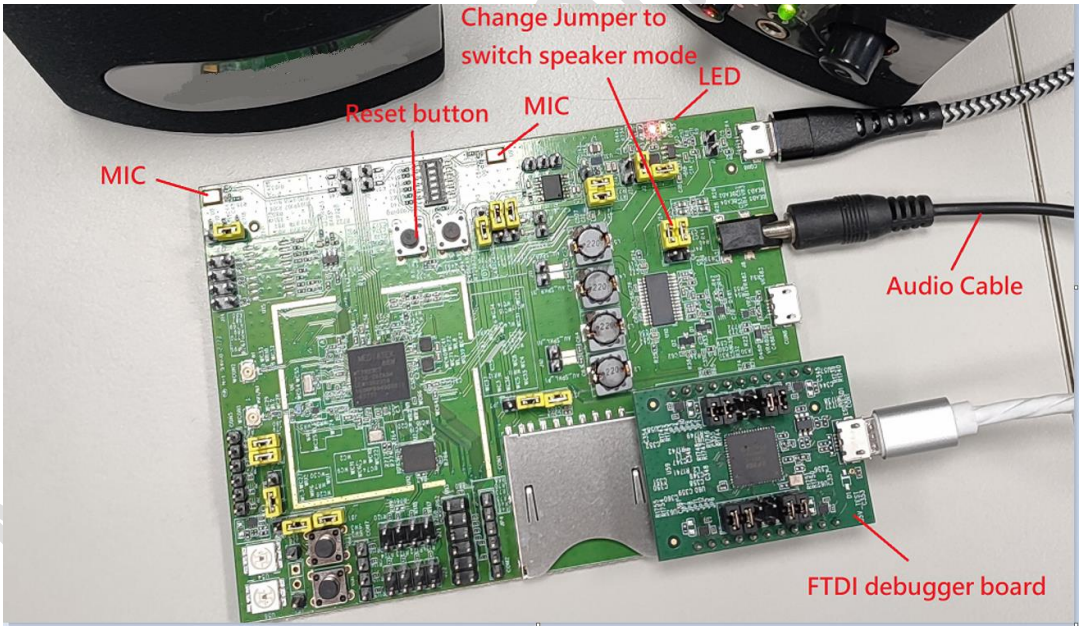

Figure 1-1. Jumpers and connectors on the MT7933 HDK

1.3 Test voice assistant

1. Open terminal and set 921600 baud, select last Comport and press reset button
2. Check terminal shows log and can type command
3. ADSP enable
   - **aud_dbg cset ADSP_Enable 1 1**
4. Start VA program
   - **aud_dbg va -v 1**
5. Say "**Hey siri**" and hear response
6. Say example command words
7. Repeat Step 5.

Trigger word："Hey Siri"

Command word："Open Camera", "Take a picture", "Play music", "Stop music", "Previous Song", "Next Song", "Volume Louder", "Volume Down"

```
$ aud_dbg cset ADSP_Enable 1 1
[amixer_cset_cmd]:2479: msg: value[1] = 0
[amixer_cset_cmd]:2481: msg: param_num = 1
[adsp_enable_put]:755: msg: set_adsp_enable
```

Figure 1-2. ADSP Enable

```
$ aud_dbg va -v 1
[add_new_dpcm]:70: msg: ADSP_HOSTLESS_VA<-->ADSP_UL9_IN BE:1
[add_new_dpcm]:70: msg: ADSP_VA_FE<-->ADSP_UL9_IN BE:1
[add_new_dpcm]:70: msg: ADSP_UL9_IN BE<-->INTADC in:1
[add_new_dpcm]:70: msg: ADSP_UL9_IN BE<-->GASRC0_C:1
[add_new_dpcm]:70: msg: GASRC0_C<-->dummy_end_c:1
[dpcm_be_dai_startup]:61: msg: dummy_end_c endpointer
[mt7933_afe_gasrc_startup]:3650: msg: [0] capture
[dpcm_be_dai_startup]:61: msg: INTADC in endpointer
[mt7933_adsp_be_startup]:1147: msg: mt7933_adsp_be_startup
```

Figure 1-3. Start VA program

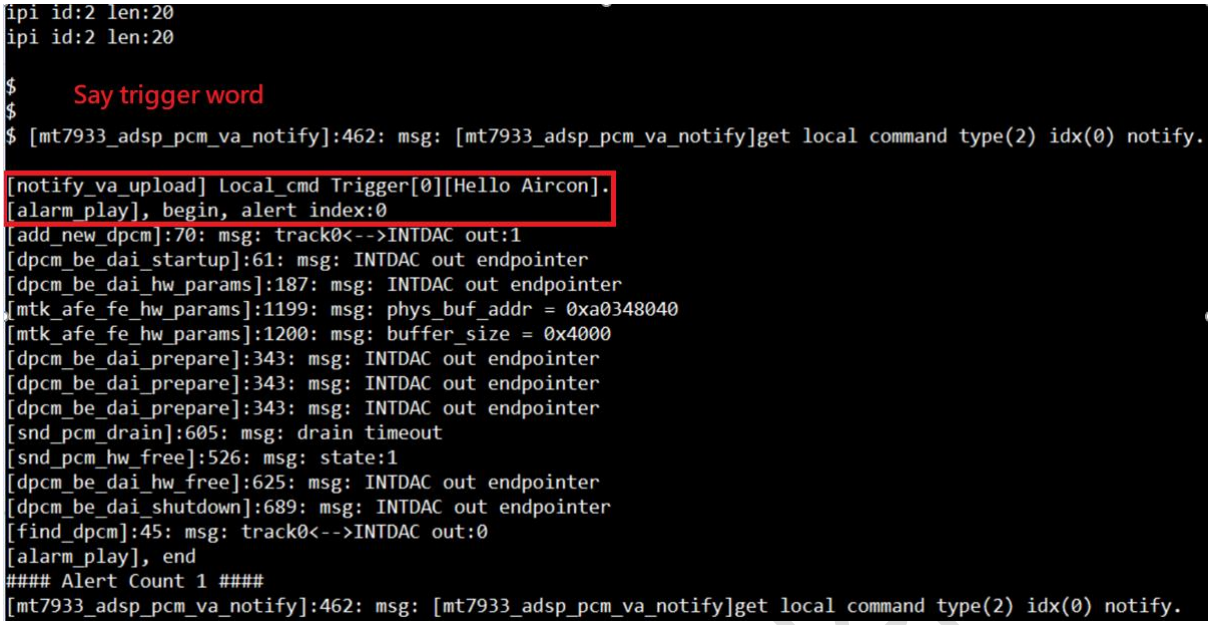

Figure 1-4. Say trigger word

2 Compilation

2.1 Project Compile

2.1.1 Makefile

./project/mt7933_hdk/apps/bga_sdk_demo/GCC/Makefile

```
# AUDIO driver files
ifeq ($(MTK_MT7933_AUDIO_DRIVER_ENABLE),y)
include $(SOURCE_DIR)/middleware/MTK/audio_services/driver/mt7933/module.mk
CFLAGS += -DMTK_MT7933_AUDIO_DRIVER_ENABLE
endif
```

Figure 2-1. Makefile

2.1.2 Feature.mk

./project/mt7933_hdk/apps/bga_sdk_demo/GCC/feature.mk

```
#Audio driver
MTK_MT7933_AUDIO_DRIVER_ENABLE = y
MTK_MT7933_AUDIO_CODEC_ENABLE = y
```

Figure 2-2. Audio enable

```
#HIFIXDSP
MTK_HIFI4DSP_ENABLE = y
```

Figure 2-3. ADSP enable

2.2 Audio Compile

2.2.1 Makefile

./middleware/MTK/audio_services/driver/mt7933/module.mk

Note: Do not change the configuration unless necessary

2.2.2 Feature.mk

./middleware/MTK/audio_services/driver/mt7933/feature.mk

Note: Do not change the configuration unless necessary

3 FreeRTOS Startup

3.1 Main Function

The main function is the entrance to the FreeRTOS system.

./project/mt7933_hdk/apps/bga_sdk_demo/src/main.c

3.2 Activated Modules

- system
- gpio
- low power
- cli
- wdt
- usb
- gcpu
- **audio**
- …….

```
#ifdef MTK_MT7933_AUDIO_DRIVER_ENABLE
    printf("AUDIO DRIVER INIT\n");
    extern void audio_init(void);
    audio_init();
#endif
```

Figure 3-1. audio init

audio_init is mainly used for the setting of audio driver, including power/CG/register.

4 Audio Interfaces

Audio Interface	Feature
DMIC	Supports 4-channel DMIC (in one wire mode); 8, 16, 32, 48 kHz; 24 bits
I2S Out (2st)	2 channels, 192 kHz, 32 bits (M)
I2S In (2nd)	2 channels, 192 kHz, 32 bits (M/S)
TDM In (1st)	8 channels, 48 kHz, 32 bits (M)
Internal Audio Codec	2-channel DAC. Support up to 48 kHz 3-channel ADC. Support up to 48 kHz

5 CLI Instruction

5.1 CLI Register

./project/mt7933_hdk/apps/bga_sdk_demo/src/cli_cmds.c

```
static cmd_t   _cmds_normal[] = {
    { "mem",    "show memory type of <addr>",    _cmd_mem_type,      NULL },
    { "s",      "search <addr> <len> <pat>",     _cmd_find_mem,      NULL },
    { "d",      "dump memory <addr> <len>",      _cmd_dump_mem,      NULL },
    { "f",      "fill memory",                   _cmd_fill_mem,      NULL },
    { "rr",     "read reg",                      _cmd_read_reg,      NULL },
    { "wr",     "write reg",                     _cmd_write_reg,     NULL },
    PSRAM_CMDS
#ifdef BRINGUP_WIFI_ENABLE
    { "wifi",   "wifi commands", NULL, wifi_init_cli },
    { "iwpriv", "WiFi iw command", iwpriv_cli, NULL },
#ifdef MTK_IPERF_ENABLE
    IPERF_CLI_ENTRY
#endif
#endif
#ifdef BRINGUP_BT_ENABLE
    { "bt",   "BT commands",                   NULL,       &_cmds_bt[0] },
#endif
#ifdef BRINGUP_DSP_ENABLE
    ADSP_CLI_ENTRY
#endif
    GOTO_TEST_MODE_CLI_ENTRY
    MINICLI_NORMAL_MODE_CLI_CMDS
    OS_CLI_ENTRY
#ifdef MTK_UT_ENABLE
    UT_CLI_ENTRY
#endif
#ifdef MTK_MT7933_AUDIO_DRIVER_ENABLE
    { "aud_dbg", "audio driver debug common", NULL, &audio_drv_debug_cmds[0]},
#endif
```

Figure 4-1. cli cmds

./middleware/MTK/audio_services/driver/mt7933/test/audio_test.c

```
cmd_t audio_drv_debug_cmds[] = {
    { "loglevel", "set log level", set_loglevel_cmd, NULL },
    { "play", "play music", audio_play_cmd, NULL },
    { "capture", "capture music", audio_capture_cmd, NULL },
    { "loopback", "play the recorded data directly", audio_loopback_cmd, NULL },
    { "cget",    "amixer cget", amixer_cget_cmd, NULL },
    { "cset",    "amixer cset", amixer_cset_cmd, NULL },
    { "dsp_r",    "dsp read", dsp_read_cmd, NULL },
    { "dsp_rw",    "dsp read and write", dsp_read_write_cmd, NULL },
    { "reg_read",    "read register", audio_register_read_cmd, NULL },
    { "reg_write",    "write register", audio_register_write_cmd, NULL },
#ifdef VA_TEST_SUPPORT
    { "va",    "va", va_main_cmd, NULL },
    { "va_stop",    "va_stop", va_stop_cmd, NULL },
    { "va_dump",    "va_dump", va_dump_cmd, NULL },
#endif
#ifdef FILE_SYS_SUPPORT
    { "play_file", "play pcm file", audio_play_file_cmd, NULL },
    { "capture_file", "capture pcm file", audio_capture_file_cmd, NULL },
    { "ff", "ff file", audio_ff_cmd, NULL },
#endif
    { NULL, NULL, NULL, NULL } // end of table
};
```

Figure 4-2. audio cli

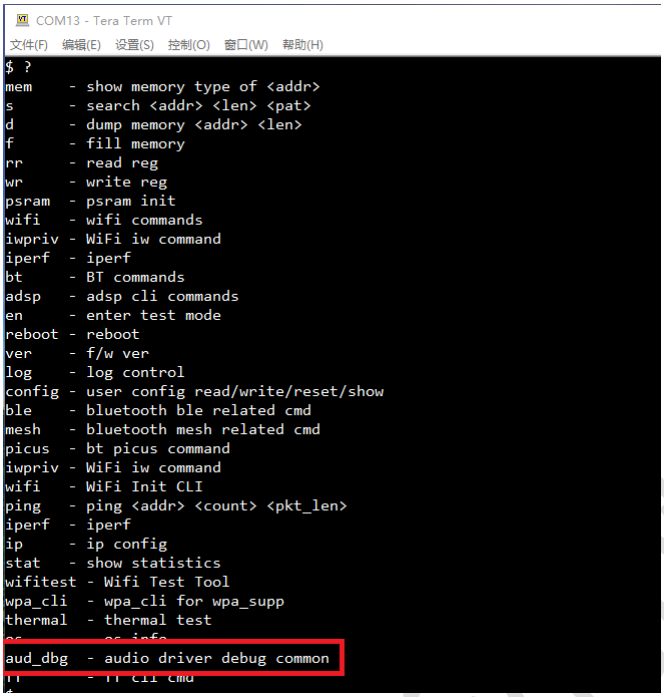

Figure 4-3. cli

5.2 CLI -- loglevel

aud_dbg loglevel [val]

```
enum AUD_LOG_LEVEL {
    AUD_LOG_ERR = 1,
    AUD_LOG_WARN,
    AUD_LOG_MSG,
    AUD_LOG_DBG,
    AUD_LOG_DEV,
};
```

Figure 4-4. loglevel

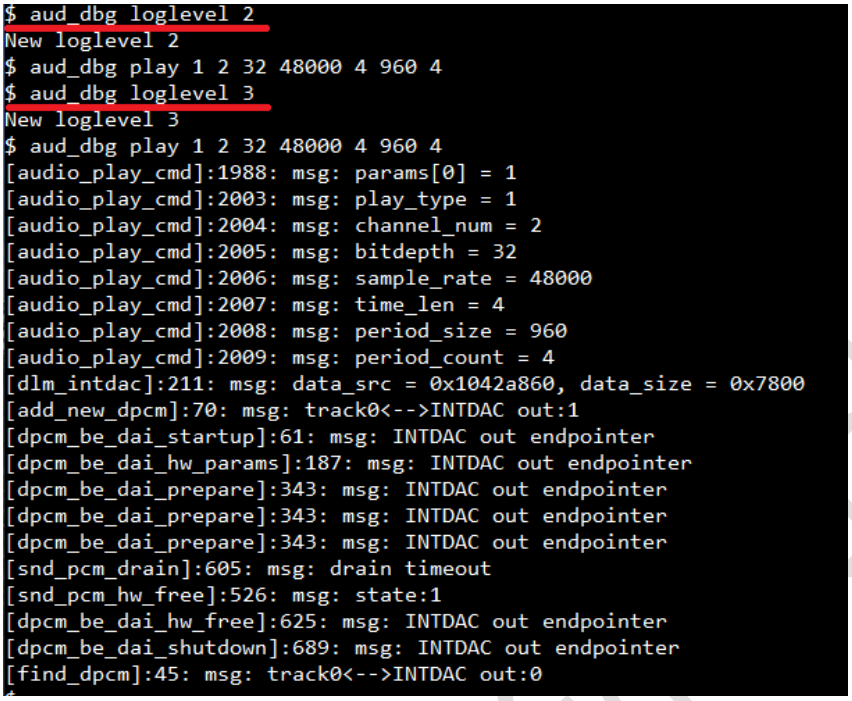

Figure 4-5. loglevel test

5.3 Tinypcm

./middleware/MTK/audio_service/sound/include/tinypcm.h

API:

- snd_pcm_open
- snd_pcm_writei
- snd_pcm_readi
- snd_pcm_hw_params
- snd_pcm_sw_params
- snd_pcm_start
- snd_pcm_prepare
- snd_pcm_hw_free
- snd_pcm_drop
- snd_pcm_drain
- snd_pcm_close
- snd_pcm_avail

5.4 CLI -- Play

aud_dbg play [play_type] [channel] [bitdepth] [rate] [time len] [period size] [period count]

5.4.1 dlm_gsrc_intdac

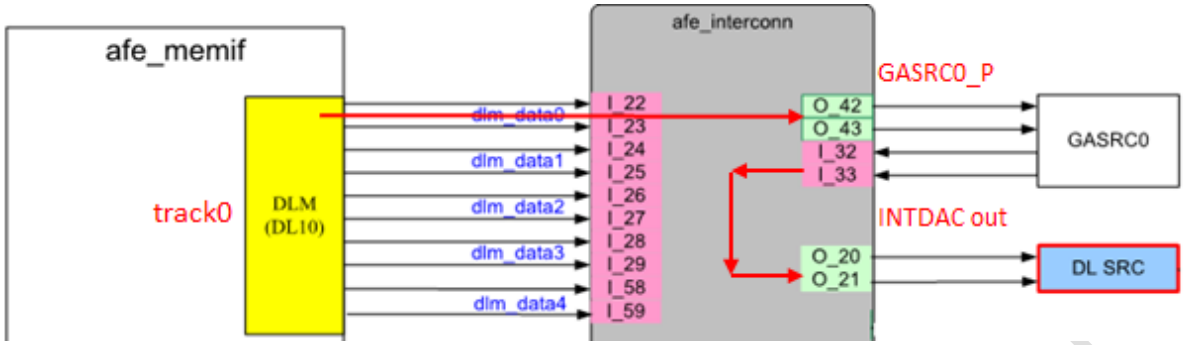

Figure 4-6. dlm_gsrc_intdac path

```
connect_route("track0", "GASRC0_P", 1, CONNECT_FE_BE);
connect_route("GASRC0_P", "INTDAC out", 1, CONNECT_FE_BE);
connect_route("I_22", "O_42", 1, CONNECT_IO_PORT);
connect_route("I_23", "O_43", 1, CONNECT_IO_PORT);
connect_route("I_32", "O_20", 1, CONNECT_IO_PORT);
connect_route("I_33", "O_21", 1, CONNECT_IO_PORT);
```

Figure 4-7. dlm_gsrc_intdac route

./middleware/MTK/audio_services/driver/mt7933/mt7933/mt7933-machine.c

You also need to fix the playback format of DAC.

```
static int mt7933_int_dac_fixup(struct snd_soc_pcm_runtime *rtd, struct msd_hw_params *params)
{
//   params->rate = 48000;
    params->channels = 2;
    return 0;
}
```

Figure 4-8. dlm_gsrc_intdac fixup

5.4.2 dlm_intdac

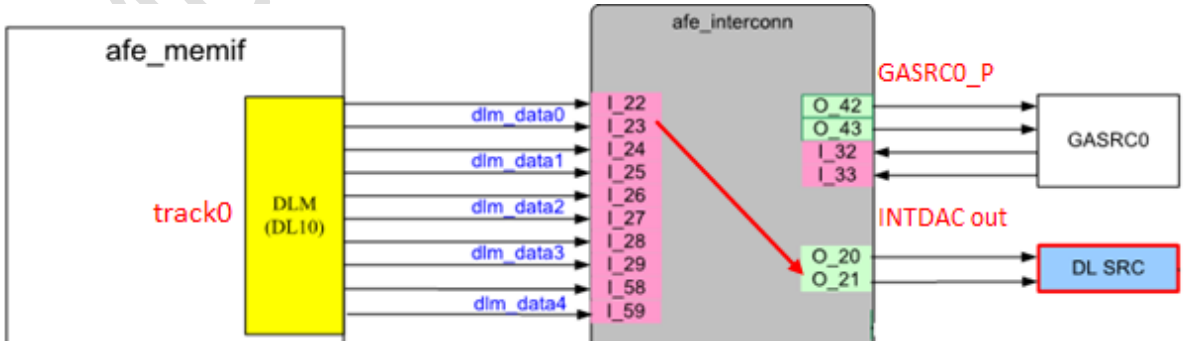

Figure 4-9. dlm_intdac path

```
connect_route("track0", "INTDAC out", 1, CONNECT_FE_BE);
connect_route("I_22", "O_20", 1, CONNECT_IO_PORT);
connect_route("I_23", "O_21", 1, CONNECT_IO_PORT);
```

Figure 4-10. dlm_intdac route

5.4.3 dlm_etdmout2

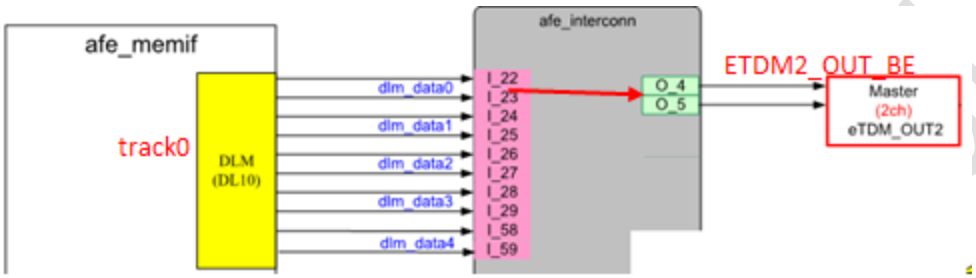

Figure 4-11. dlm_etdmout2 path

```
connect_route("track0", "ETDM2_OUT_BE", 1, CONNECT_FE_BE);
connect_route("I_22", "O_04", 1, CONNECT_IO_PORT);
connect_route("I_23", "O_05", 1, CONNECT_IO_PORT);
```

Figure 4-12. dlm_etdmout2 route

5.5 CLI -- Capture

5.5.1 ul3_intadc

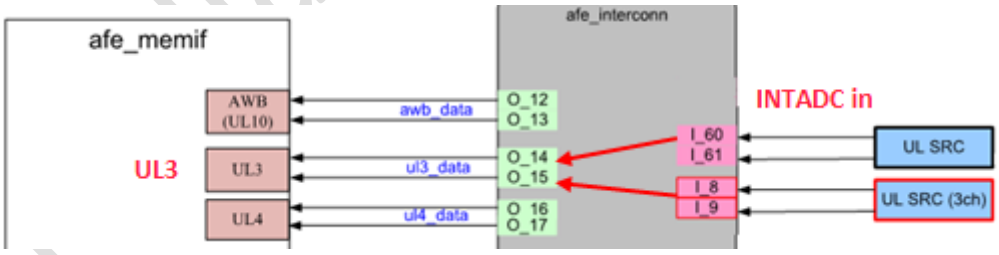

Figure 4-13. ul3_intadc path

```
    connect_route("UL3", "INTADC in", 1, CONNECT_FE_BE);
#ifdef PINMUX_QFN_DEFAULT
    connect_route("I_60", "O_14", 1, CONNECT_IO_PORT);
    connect_route("I_61", "O_15", 1, CONNECT_IO_PORT);
#elif defined PINMUX_BGA_DEFAULT
    connect_route("I_60", "O_14", 1, CONNECT_IO_PORT);
    connect_route("I_08", "O_15", 1, CONNECT_IO_PORT);
#endif
```

Figure 4-14. ul3_intadc route

5.5.2 ul3_dmic

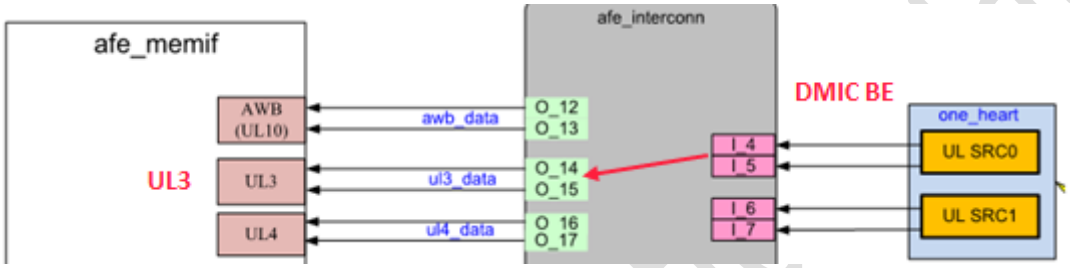

Figure 4-15. ul3_dmic path

```
connect_route("UL3", "DMIC BE", 1, CONNECT_FE_BE);
connect_route("I_04", "O_14", 1, CONNECT_IO_PORT);
connect_route("I_05", "O_15", 1, CONNECT_IO_PORT);
```

Figure 4-16. ul3_dmic route

5.5.3 ul9_intadc

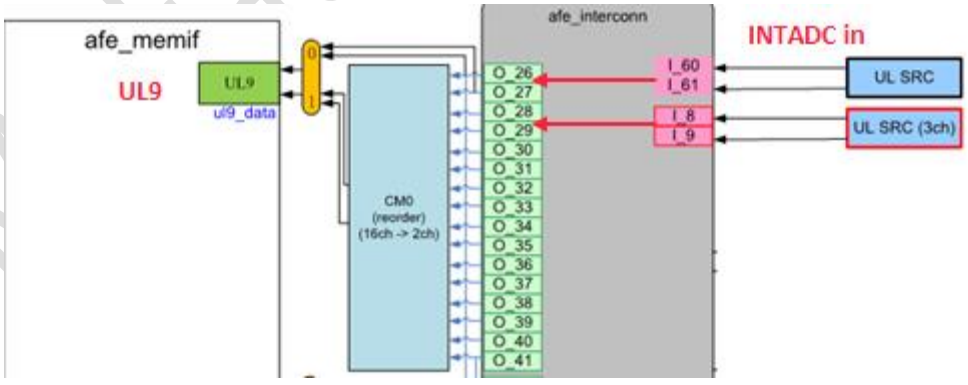

Figure 4-17. ul9_intadc

```
connect_route("UL9", "INTADC in", 1, CONNECT_FE_BE);
connect_route("I_60", "O_26", 1, CONNECT_IO_PORT);
connect_route("I_61", "O_27", 1, CONNECT_IO_PORT);
connect_route("I_08", "O_28", 1, CONNECT_IO_PORT);
connect_route("I_09", "O_29", 1, CONNECT_IO_PORT);
```

Figure 4-18. ul9_intadc route

5.5.4 ul9_etdmin2

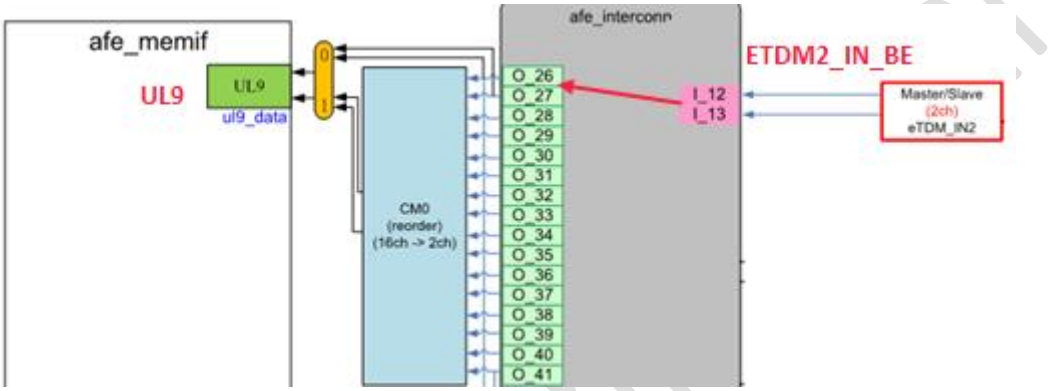

Figure 4-19. ul9_etdmin2 path

```
connect_route("UL9", "ETDM2_IN_BE", 1, CONNECT_FE_BE);
connect_route("I_12", "O_26", 1, CONNECT_IO_PORT);
connect_route("I_13", "O_27", 1, CONNECT_IO_PORT);
```

Figure 4-20. ul9_etdmin2 route

5.5.5 ul9_intadc_and_dlm

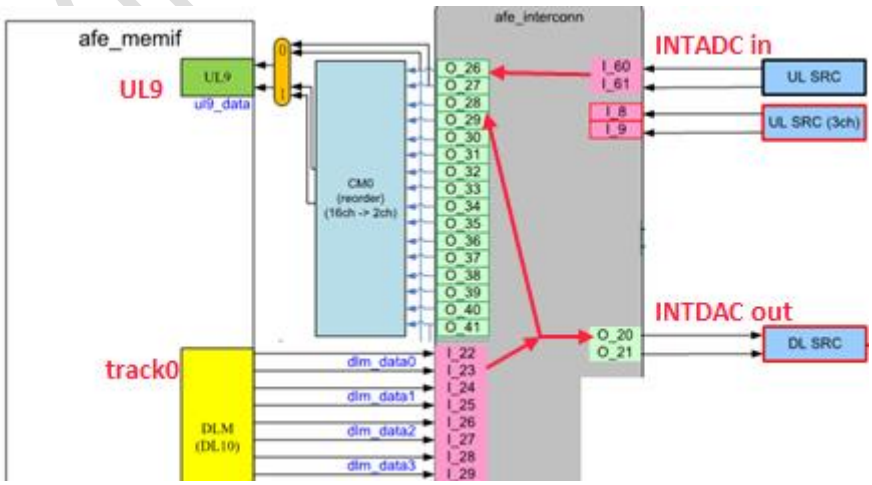

Figure 4-21. ul9_intadc_and_dlm path

```
connect_route("track0", "INTDAC out", 1, CONNECT_FE_BE);
connect_route("I_22", "O_20", 1, CONNECT_IO_PORT);
connect_route("I_23", "O_21", 1, CONNECT_IO_PORT);
connect_route("I_22", "O_28", 1, CONNECT_IO_PORT);
connect_route("I_23", "O_29", 1, CONNECT_IO_PORT);
connect_route("UL9", "INTADC in", 1, CONNECT_FE_BE);
connect_route("I_60", "O_26", 1, CONNECT_IO_PORT);
connect_route("I_61", "O_27", 1, CONNECT_IO_PORT);
```

Figure 4-22. ul9_intadc_and_dlm route

5.6 CLI – Playback and Capture Audio File

5.6.1 Setting

./middleware/MTK/audio_services/driver/mt7933/feature.mk

```
# Audio Feature Option Configuration
########################################
CFG_MTK_AUDIODSP_SUPPORT        = y
CFG_WRAP_CAPTURE_SUPPORT        = n
CFG_FILE_SYS_SUPPORT            = y
CFG_DSP_BOOT_RUN                = n
CFG_VA_TEST_SUPPORT             = y
CFG_VA_TASK_SUPPORT             = y
CFG_RECORD_TASK_SUPPORT         = n
CFG_IPC_SUPPORT                 = y
```

Figure 4-23. File system feature

ff mount SD:/

```
$ ff mount SD:/
Vol(0)FF_MAX_SS: 512
SD init frequency: 13000
PIO mode
[FS]: Mount OK!
$ 00-00 02:56:46.422 100 E -----------------SD init Run -----------

00-00 02:56:46.423 100 I set clk final:390, request: 400, sclk: 50000, MSDC_CFG = 0x02002019 MSDC_PS: 0x010f00
02

00-00 02:56:46.423 100 I init hardware done cfg:0x0200209b

00-00 02:56:46.423 100 I set clk final:390, request: 400, sclk: 50000, MSDC_CFG = 0x0200209b MSDC_PS: 0x010f00
02

00-00 02:56:46.623 100 I set clk final:12500, request: 13000, sclk: 50000, MSDC_CFG = 0x02000119 MSDC_PS: 0x01
0f0002

00-00 02:56:46.623 100 I set clk final:12500, request: 13000, sclk: 50000, MSDC_CFG = 0x02000199 MSDC_PS: 0x01
0f0002
```

Figure 4-24. ff mount

5.6.2 Operation

aud_dbg play_file [play_type] [channel] [bitdepth] [rate] [time len] [period size] [period count] [file_name]

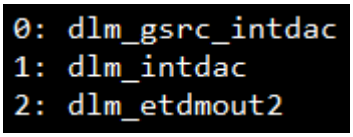

Figure 4-25. play type -- file system

aud_dbg capture_file [capture_type] [channel] [bitdepth] [rate] [time len] [period size] [period count] [file_name]

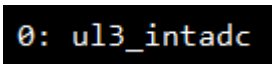

Figure 4-26. capture type -- file system

6 DSP Introduction

6.1 DSP Features

Cadence Tensilica HiFi 4 DSP

- Xtensa DSP architecture
- Single HiFi 4 DSP 300/600MHz in the MT7933
  - Tool Chain: RI-2019.1
  - IDE: Xtensa Xplorer 8.0.10

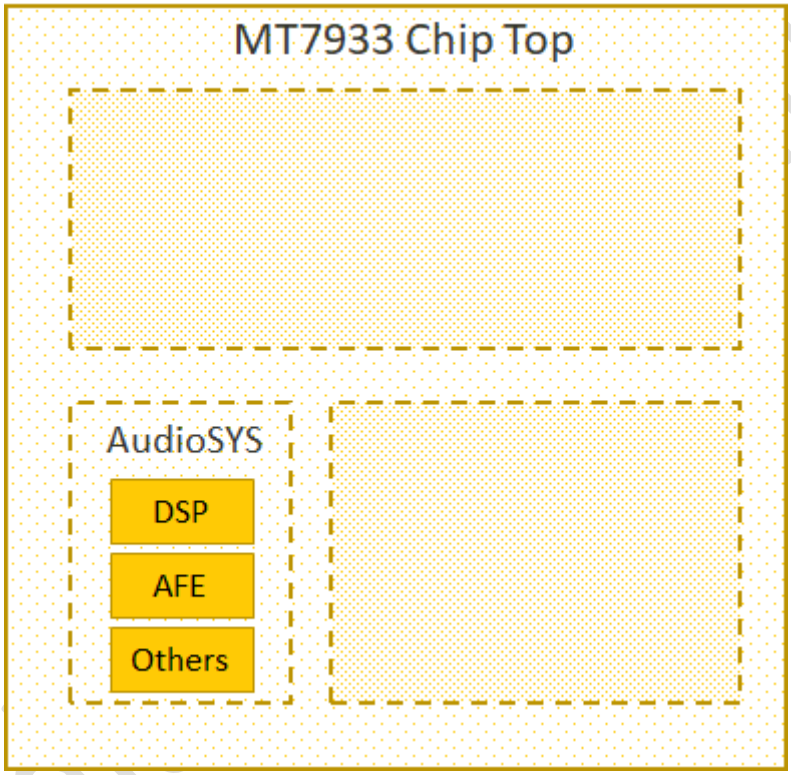

Figure 5-1. MT7933 Chip Top

6.2 Hello, DSP

6.2.1 Auto Boot Up

./middleware/MTK/audio_services/driver/mt7933/feature.mk

```
CFG_MTK_AUDIODSP_SUPPORT        = y
CFG_WRAP_CAPTURE_SUPPORT        = n
CFG_FILE_SYS_SUPPORT            = y
CFG_DSP_BOOT_RUN                = n
CFG_VA_TEST_SUPPORT             = y
CFG_VA_TASK_SUPPORT             = y
CFG_RECORD_TASK_SUPPORT         = n
CFG_IPC_SUPPORT                 = y
CFG_GPIO_SUPPORT                = y
CFG_DRV_MUSIC_DATA_EN           = n
```

Figure 5-2. auto boot up dsp

6.2.2 Cli on CM33 uart

aud_dbg cset ADSP_Enable 1 1

```
(201105_12:12:16.020)[0.000]FreeRTOS V10.2.0 b900ff
(201105_12:12:16.021)[0.003][systimer] ostimer_init_cycle = 0x8A746DC at 13MHz.
(201105_12:12:16.021)[0.008]adsp_info = 0xa003fc00
(201105_12:12:16.021)[0.011]adsp_send_obj = 0xa003fc20
(201105_12:12:16.021)[0.014]adsp_rcv_obj = 0xa003fd40
(201105_12:12:16.021)[0.017]adsp_rcv_obj->share_buf = 0xa003fd50
(201105_12:12:16.021)[0.021]in platform_init
(201105_12:12:16.021)[0.023][D]+audio_init(), Heap free/total = 125844/134144
(201105_12:12:16.021)[0.028][D]+audio_driver_init
(201105_12:12:16.021)[0.031][D]-audio_driver_init
(201105_12:12:16.021)[0.033][D]-audio_init(), Heap free/total = 125752/134144
(201105_12:12:16.021)[0.038]dsp_hw_res_init [time:38670307]
```

Figure 5-3. enable dsp

6.3 Start Voice Detection

Cli on CM33 uart: **aud_dbg va -v 1**

Figure 5-4. Start voice detection

6.4 VA Flow

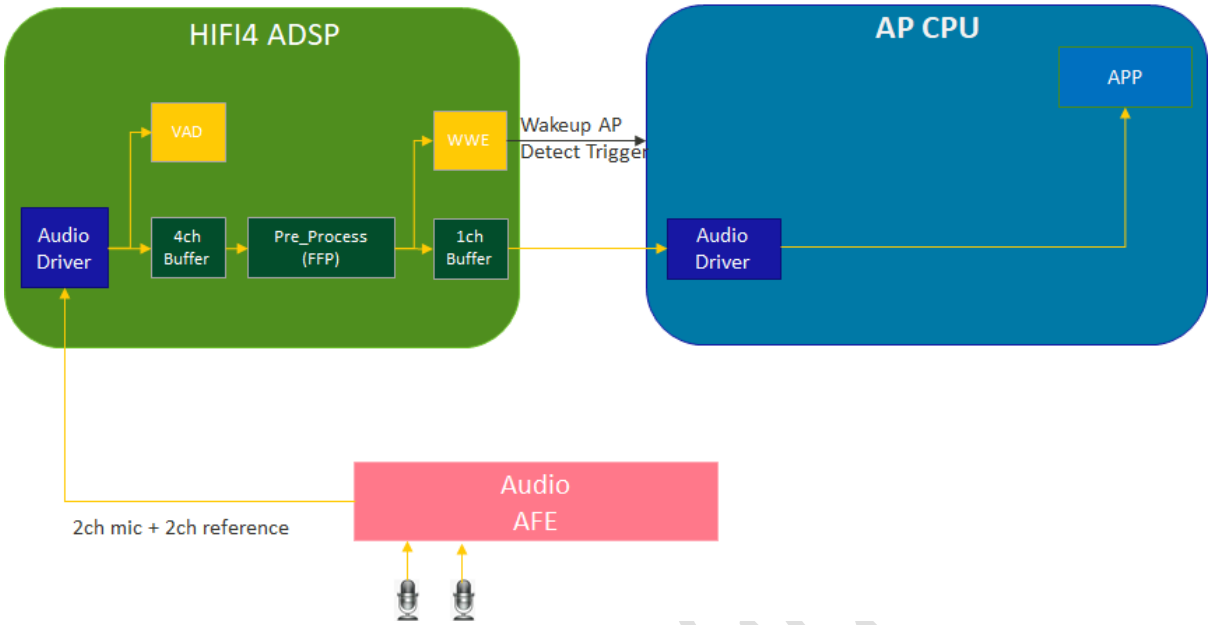

Figure 5-5. VA flow

6.5 Route

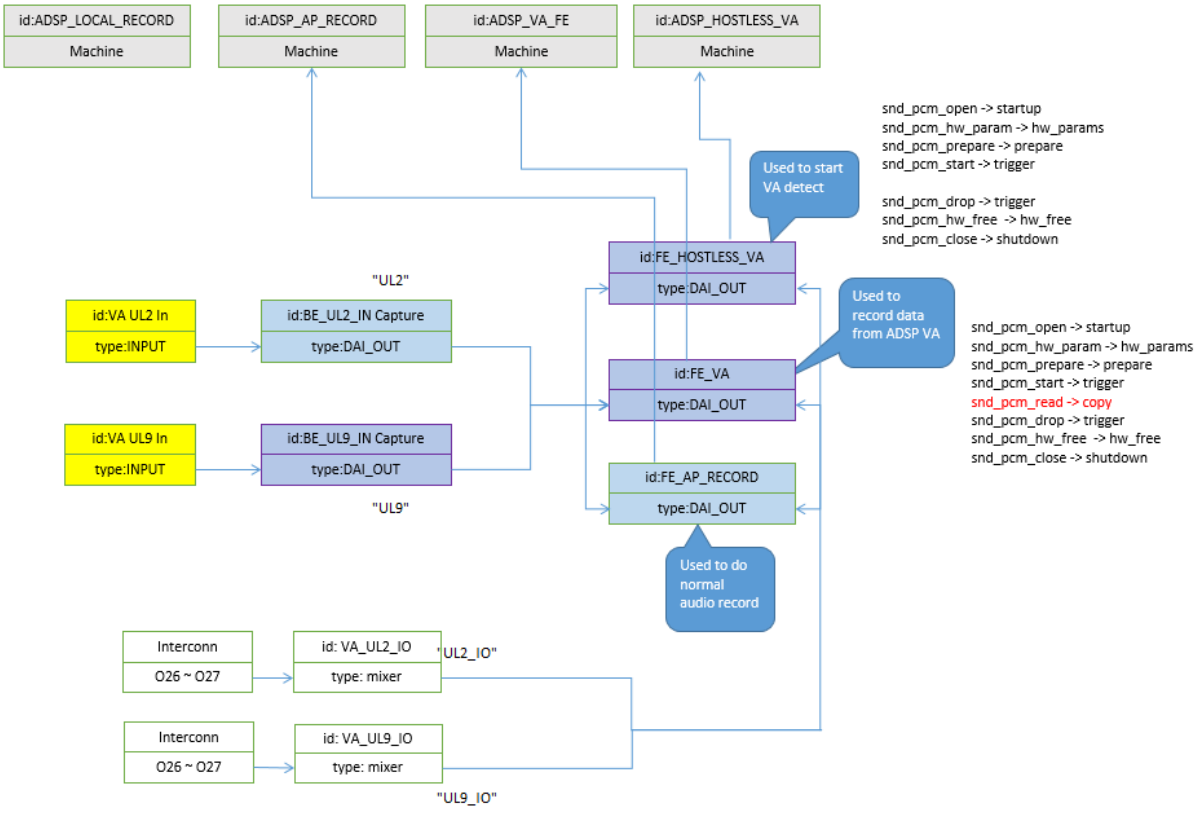

Figure 5-6. VA route

./middleware/MTK/audio_services/driver/mt7933/test/va.c

```
#ifdef VA_TEST_SUPPORT
    { "va",     "va", va_main_cmd, NULL },
    { "va_stop",     "va_stop", va_stop_cmd, NULL },
    { "va_dump",     "va_dump", va_dump_cmd, NULL },
#endif
```

Figure 5-7. VA cli

```
void va_main(int argc, char *argv[])
{
    int ret = 0;
    struct va_task *p_va_task = task_constructor();
    struct msd_hw_params *params = (struct msd_hw_params *)p_va_task->priv;

    ret = va_cmd_parser(argc, argv, params);
    if (ret < 0)
        return;

    connect_route("ADSP_HOSTLESS_VA", "ADSP_UL9_IN BE", 1, CONNECT_FE_BE);
    connect_route("ADSP_VA_FE", "ADSP_UL9_IN BE", 1, CONNECT_FE_BE);
    connect_route("ADSP_UL9_IN BE", "INTADC in", 1, CONNECT_FE_BE);
    connect_route("ADSP_UL9_IN BE", "GASRC0_C", 1, CONNECT_FE_BE);
    connect_route("GASRC0_C", "dummy_end_c", 1, CONNECT_FE_BE);
    connect_route("I_60", "O_26", 1, CONNECT_IO_PORT);
    connect_route("I_08", "O_27", 1, CONNECT_IO_PORT);
    connect_route("I_22", "O_28", 1, CONNECT_IO_PORT);
    connect_route("I_23", "O_29", 1, CONNECT_IO_PORT);

    xTaskCreate(va_capture_loop,
        "ap_aud_t_va",
        p_va_task->thread_stack_dep,
        (void *)p_va_task,
        p_va_task->thread_priority,
        &p_va_task->thread_handler);
```

Figure 5-8. VA route code

6.6 Buffer Flow

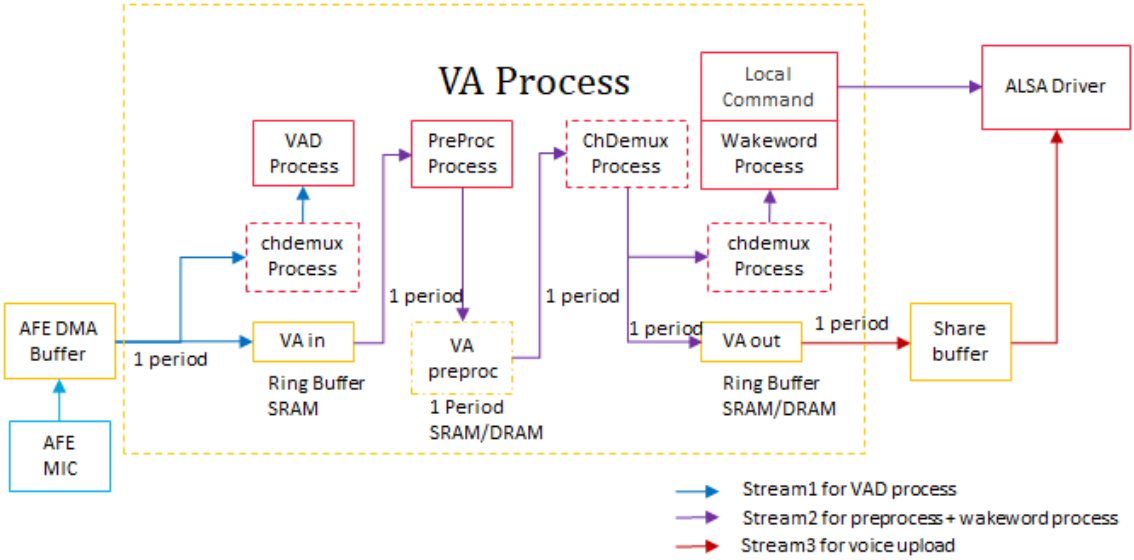

Figure 5-9. VA process buffer flow

Exhibit 1 Terms and Conditions

Your access to and use of this document and the information contained herein (collectively this "Document") is subject to your (including the corporation or other legal entity you represent, collectively "You") acceptance of the terms and conditions set forth below ("T&C"). By using, accessing or downloading this Document, You are accepting the T&C and agree to be bound by the T&C. If You don't agree to the T&C, You may not use this Document and shall immediately destroy any copy thereof.

This Document contains information that is confidential and proprietary to MediaTek Inc. and/or its affiliates (collectively "MediaTek") or its licensors and is provided solely for Your internal use with MediaTek's chipset(s) described in this Document and shall not be used for any other purposes (including but not limited to identifying or providing evidence to support any potential patent infringement claim against MediaTek or any of MediaTek's suppliers and/or direct or indirect customers). Unauthorized use or disclosure of the information contained herein is prohibited. You agree to indemnify MediaTek for any loss or damages suffered by MediaTek for Your unauthorized use or disclosure of this Document, in whole or in part.

MediaTek and its licensors retain titles and all ownership rights in and to this Document and no license (express or implied, by estoppels or otherwise) to any intellectual propriety rights is granted hereunder. This Document is subject to change without further notification. MEDIATEK DOES NOT ASSUME ANY RESPONSIBILITY ARISING OUT OF OR IN CONNECTION WITH ANY USE OF, OR RELIANCE ON, THIS DOCUMENT, AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY, INCLUDING, WITHOUT LIMITATION, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

THIS DOCUMENT AND ANY OTHER MATERIALS OR TECHNICAL SUPPORT PROVIDED BY MEDIATEK IN CONNECTION WITH THIS DOCUMENT, IF ANY, ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE. MEDIATEK SPECIFICALLY DISCLAIMS ALL WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR A PARTICULAR PURPOSE, COMPLETENESS OR ACCURACY AND ALL WARRANTIES ARISING OUT OF TRADE USAGE OR OUT OF A COURSE OF DEALING OR COURSE OF PERFORMANCE. MEDIATEK SHALL NOT BE RESPONSIBLE FOR ANY MEDIATEK DELIVERABLES MADE TO MEET YOUR SPECIFICATIONS OR TO CONFORM TO A PARTICULAR STANDARD OR OPEN FORUM.

Without limiting the generality of the foregoing, MEDIATEK MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR DOES MEDIATEK ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT, CIRCUIT OR SOFTWARE. You agree that You are solely responsible for the designing, validating and testing Your product incorporating MediaTek's product and ensure such product meets applicable standards and any safety, security or other requirements.

The above T&C and all acts in connection with the T&C or this Document shall be governed, construed and interpreted in accordance with the laws of Taiwan, without giving effect to the principles of conflicts of law.