MT7931 RFB User Guide

Version: **1.2**
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Version History

Version	Date	Description
1.0	2020-12-01	Initial release
1.1	2021-10-01	Modify latest design file and description
1.2	2021-10-27	Update GPIO table and PCB photo

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1 Introduction

1.1 General Description

MediaTek LinkIt™ for real-time operating system (RTOS) is a low-cost and easy-to-use Internet of Things (IoT) development platform to design, prototype, evaluate and implement IoT projects. The platform supports MT7931 hardware development kit (HDK). This user manual provides required knowledge on features of the HDK, including the pins, communication interfaces, core microcontroller unit (MCU) description, the networking capabilities and how to use them through the host driver.

MediaTek's MT7931 is a highly integrated single chip that features an Arm® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. The MT7931 is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

The MT7931 is based on Arm Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The chip also supports rich peripheral interfaces, including UART, SDIO, I2C, SPI, I2S, and auxiliary ADC.

These features are used to download and debug a project on MT7931 HDK.

Figure 1 shows the front view of the HDK including a main board and an FTDI debug board.

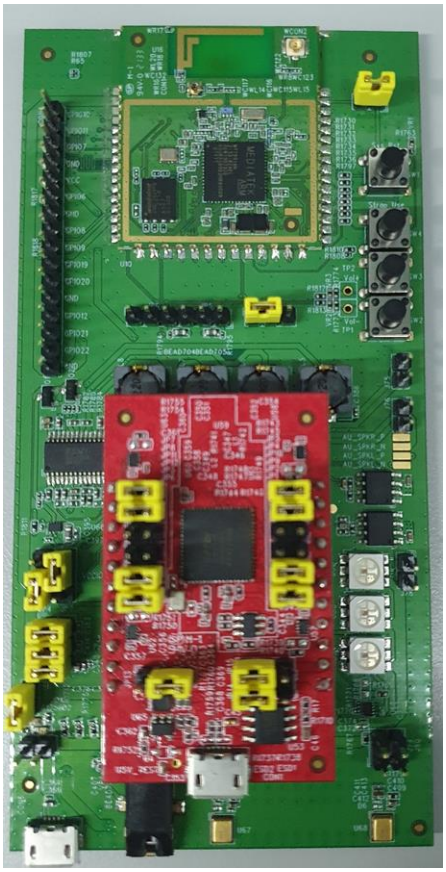

Figure 1. Front view of MT7931 HDK and FTDI debug board

2 Get Started with the HDK

Before commencing the application development, you need to configure the development platform.

2.1 Configuring the MT7931 HDK

MT7931 DRQFN RFB HDK includes a Base Board (MT7933_DRQFN_RFB_BASE), an MT7931 stamp module (MT7933_DRQFN_RFB_BASE) and an FTDI Debug board (MT7933_FTDI_debug board_V10). Figure 2 shows the top view of the MT7931 DRQFN RFB.

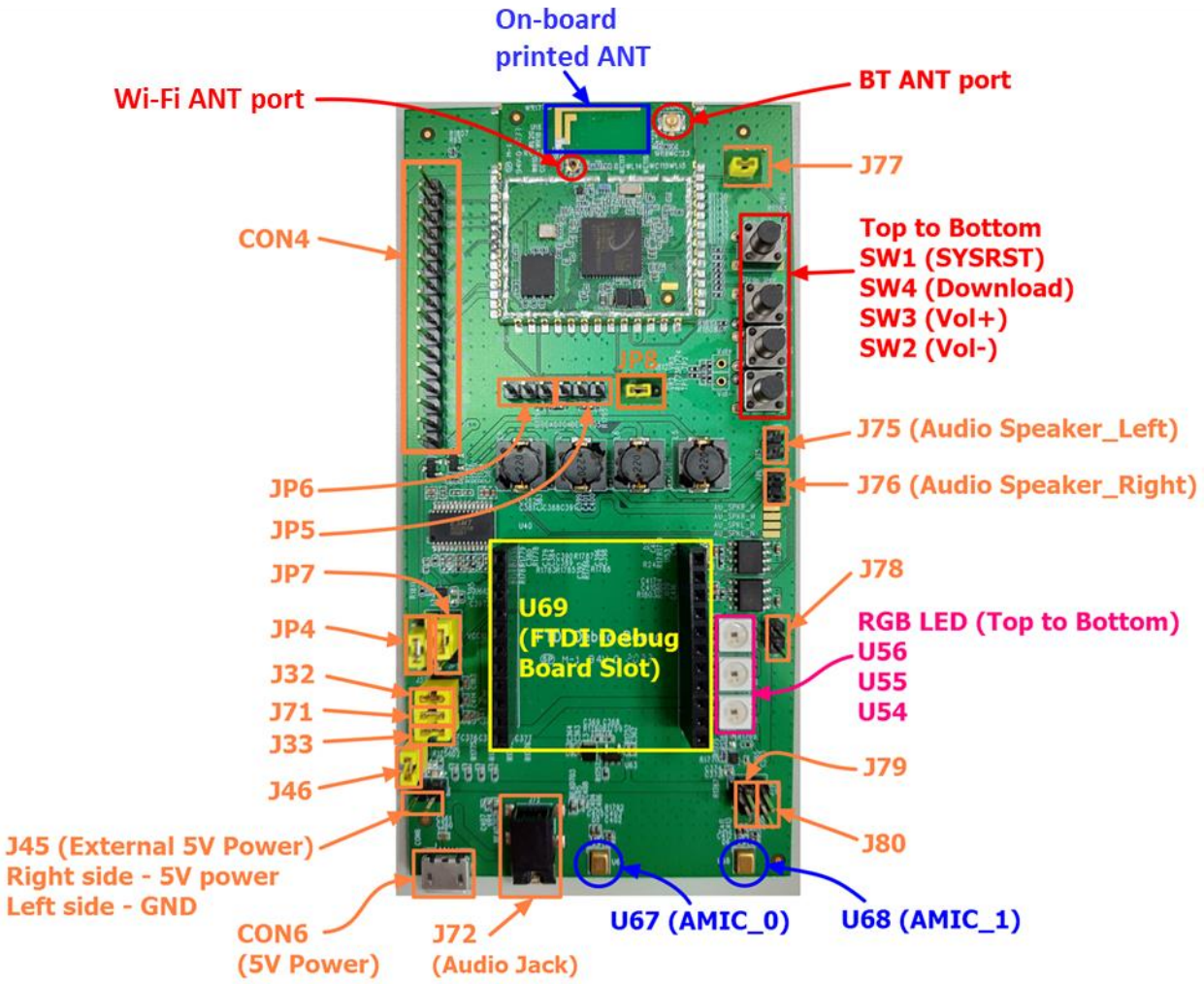

Figure 2. Jumpers and connectors on the MT7931 HDK

The description of pins (Figure 2) and their functionality are provided below.

1. **CON6** is a USB 5V power for MT7931 main board, or you can use external 5V power at **J45.**
2. Press **SW1** to reset the system. For information about **SW2** to **SW4**, see Section 0.
3. For Wi-Fi and BT function, MT7931 main board reserves a **Wi-Fi SMA connector** and a **BT SMA connector**. You can also use the **on-board printed antenna** to **transmit and receive** RF signal.

4. The **FTDI debug board** can transfer USB interface to UART interface. Using this debug board can debug through UART, transmit and receive a signal form PC.
5. **U67** and **U68** are on-board AMICs which can catch voice command.
6. **J75** and **J76** are audio speaker connectors which can connect 8-ohm/2W speaker to achieve voice assistant function.
7. **U54, U55** and **U56** are RGB LEDs controlled by SPIM interface.
8. **CON4** supports multifunction GPIO interface. For more detail, refer to Section 4.7.

2.2 Installing the FTDI Debug Board Drivers on Microsoft Windows

To configure the MT7931 HDK:

1. Ensure the FTDI debug board connects to MT7931 main board at **U69**.
2. Connect the FTDI debug board to the computer using a Micro-USB cable.
3. Connect a 5V power at MT7931_DRQFN_RFB **CON6** with a Micro-USB cable.
4. Check whether your PC is running on a X86 or X64 system. Download and install FTDI Windows serial port driver from Here. (The red block in the following figure shows the file to download)

Currently Supported D2XX Drivers:

		Processor Architecture					
Operating System	Release Date	x86 (32-bit)	x64 (64-bit)	ARM	MIPS	SH4	Comments
Windows*	2017-08-30	2.12.28	2.12.28	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides.
Windows RT	2014-07-04	1.0.2	-	1.0.2	-	-	A guide to support the driver (AN_271) is available here
Linux	2018-06-22	1.4.8	1.4.8	1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard-float *** 1.4.8 ARMv7 hard-float *** 1.4.8 ARMv8 hard-float ***	1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt-uclibc		If unsure which ARM version to use, compare the output of `readelf` and `file` commands on a system binary with the content of release/build/libftd2xx.txt in each package. ReadMe NEW! Video Install Guide

5. If your OS is Windows7 or 10, please open Windows **Control Panel** then click **System** and enter **Device Manager**.
6. In **Device Manager**, navigate to **Ports** (**COM & LPT**) (see Figure 3).
7. A new **COM** device should appear under Ports (**COM & LPT**) in **Device Manager**, as shown in Figure 3. Note the **COMx** port number of the serial communication port. This information is needed to send command and receive logs from the **COM** port.

   The com port numbers (**COMx**) are different at different PC. In order to check the function of each com port, you can recognize the order of these com ports. As Figure 3 shows, the first com port (#1) means “DSP UART”, the second com port (#2) means “UART0”, the third com port (#3) means “UART1”, and the fourth com port (#4) means “CM33 UART”.

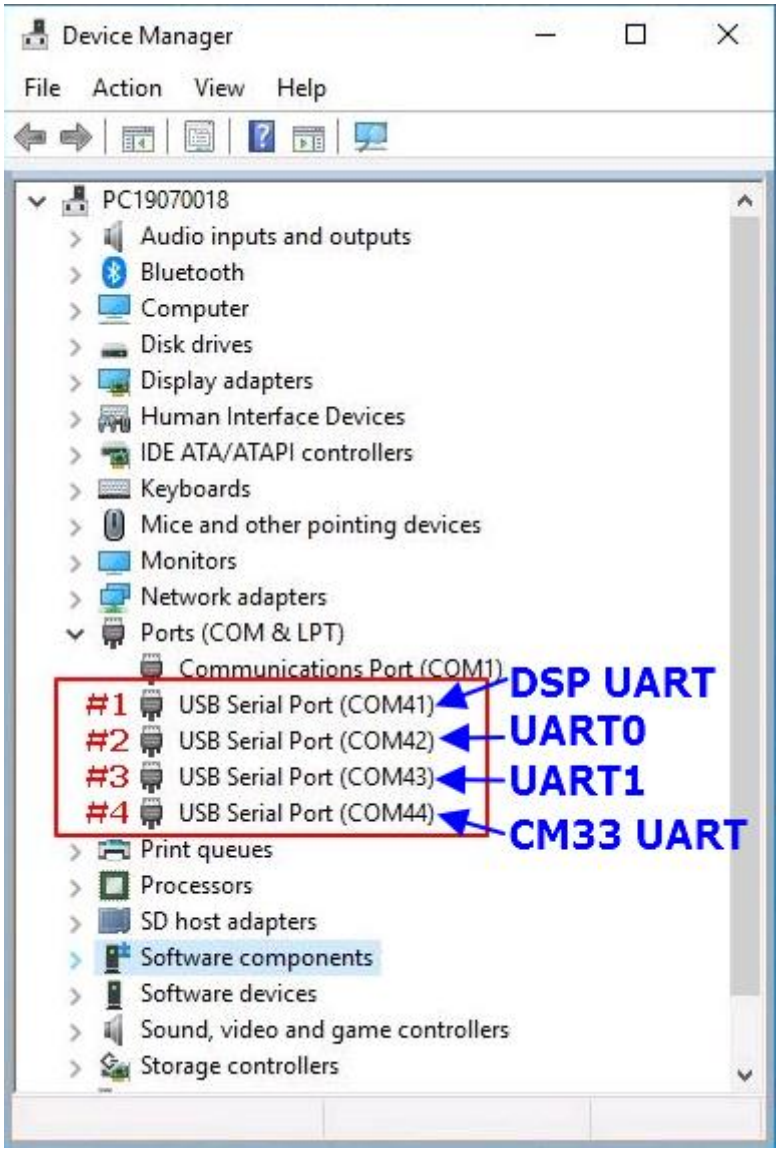

Figure 3. COM port associated with the MT7931 HDK

2.3 Downloading the Image Using the MT7931 HDK

The MT7931 HDK is embedded with 8MB flash memory. The boot options are either from the flash memory or from the UART port.

To update the image on the MT7931 HDK:

1. Download the latest Image.
2. Ensure **U69** connects to an **FTDI debug board**.
3. Ensure **CON6** connects to 5V power with Micro-USB cable and **FTDI debug board** connects to PC with Micro-USB cable.
4. Check the **Device Manager** at PC. There are 4 USB serial ports as Figure 3 shows.
5. Decompress the image file and open the “FBTool_gui” tool. See the red box in Figure 4.

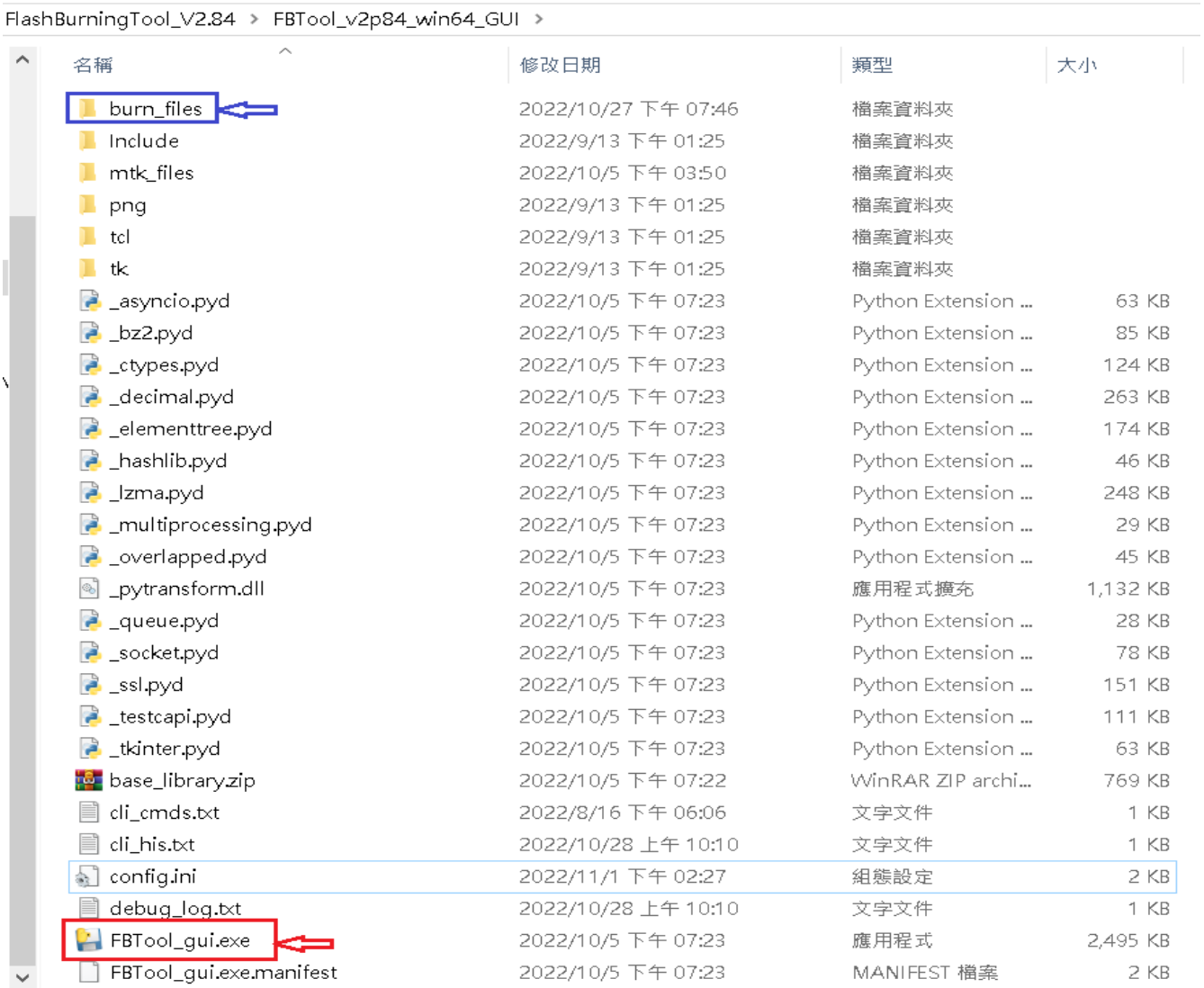

Figure 4. FlashBurningTool:FBTool_gui.exe

6. Refer to Figure 5. Click “Open” button to navigate the folder of your scatter files (See the blue arrow in Figure 5). And press “Refresh” button.
7. Refer to Figure 5. Go to red box 1 and choose the file you want to burn into flash.
8. Refer to Figure 5. Go to red box 2 and choose the “CM33 UART” port of your PC. (Refer to Step 7 in Section 2.2 to check which USB serial port is CM33 UART port at your PC).
9. Keep “**SW1**” and “**SW4**” pressed and refer to Figure 5. Click “Download” (See red box 3 in Figure 5) and wait for FlashBurningTool feedback.
10. After clicking “Download” button and release “**SW1**” and “**SW4**” , you see the progress bar as Figure 6 and Figure 7 show.
11. Check FlashBurningTool to see the progress bar of burning image.(See red box 4 in Figure 5 and wait to 100%)

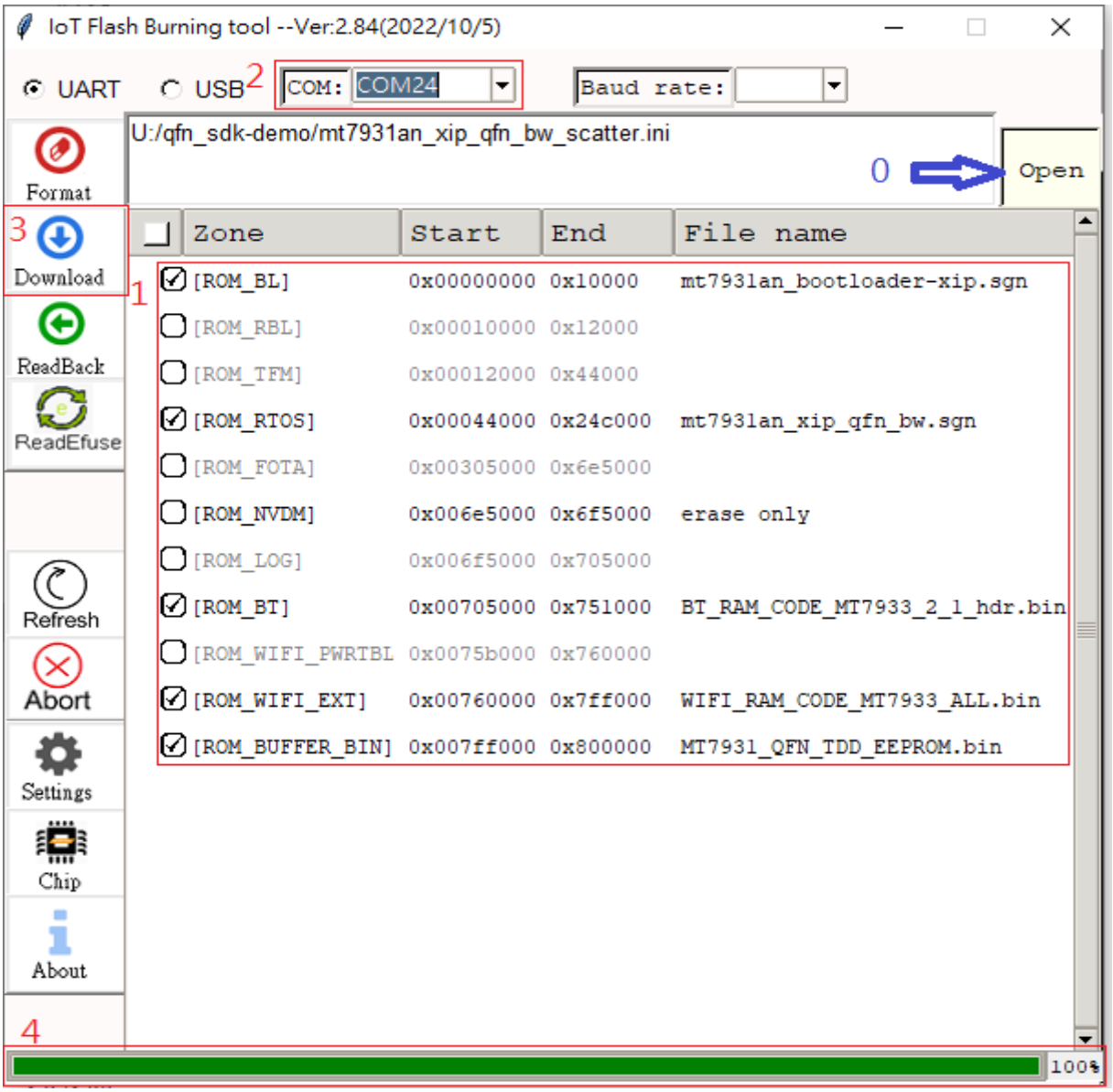

Figure 5. FlashBurningTool_User intrerface

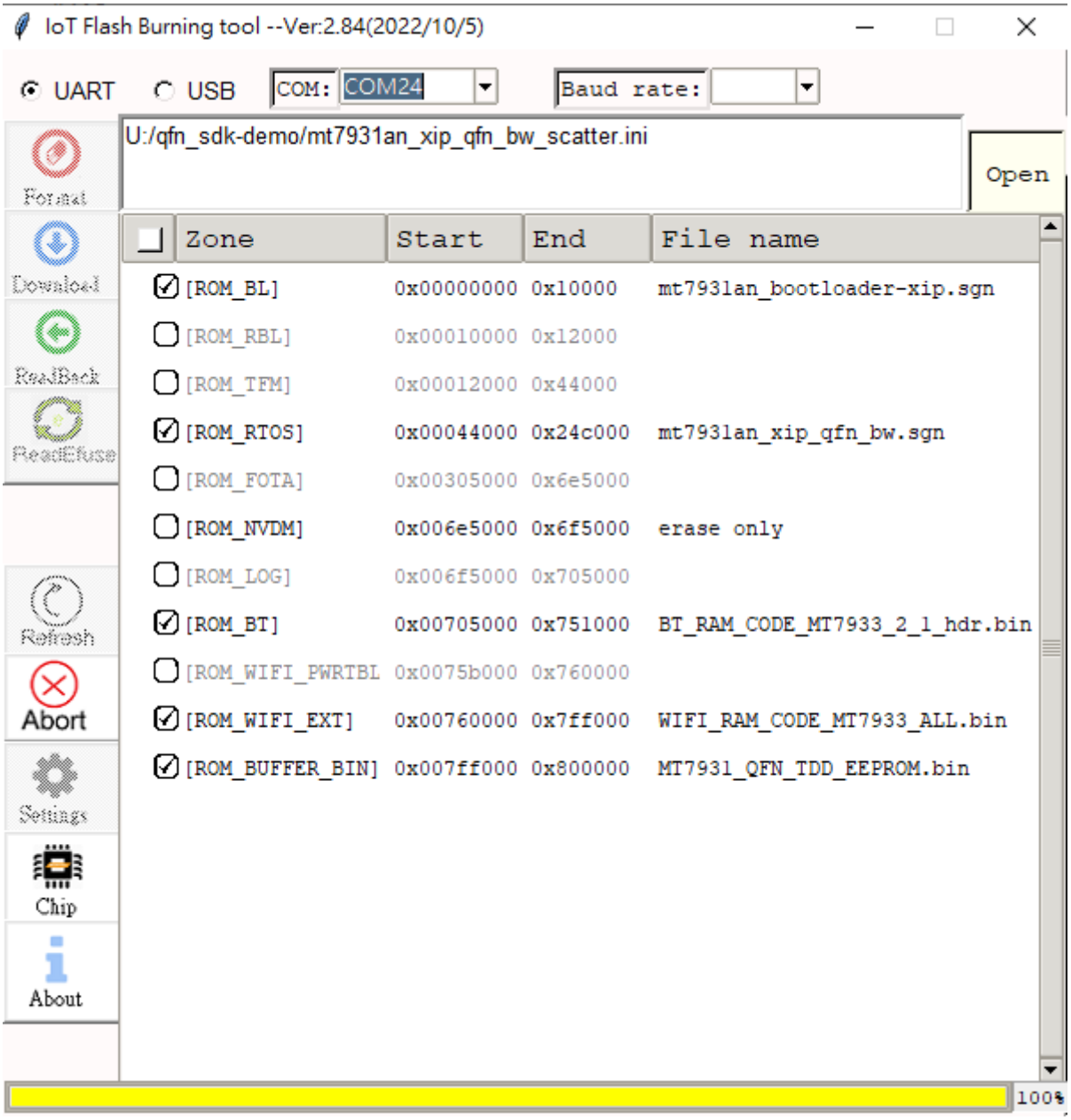

Figure 6. FlashBurningTool_operation step 1

Figure 7. FlashBurningTool_operation step 2

3 Hardware Features

This chapter provides the main supported features of the MT7931 HDK. The detailed description of the features is provided in the upcoming sections.

3.1 Features Description

3.1.1 Technology and Package

- 9 mm x 8.7 mm DRQFN package

3.1.2 Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input
- Supports 26-MHz crystal clock with low power operation in idle mode
- Supports 32-kHz crystal oscillator or internal 32-kHz for low power sleep mode

3.1.3 Platform

- Arm Cortex-M33 MCU with FPU with up to 300-MHz clock speed
- Embedded 1MB SRAM
- Supports external serial flash up to 16MB with eXecute In Place (XIP) and on-the-fly AES
- Supports hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security
- Supports up to 27 General-Purpose IOs, which are multiplexed with SPI, I2C, Aux ADC, UART, and GPIO interfaces
- Supports 12 DMA channels

3.1.4 Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ax 5GHz and 2.4GHz
- Supports 20 MHz, bandwidth in 2.4G/5GHz band, and MCS0 to MCS8
- Supports MU-MIMO RX
- Supports uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Supports STBC RX, LDPC TX, and RX Beamforming
- Wi-Fi security WFA WPA/WPA2/WPA3 personal
- Supports 11ax TWT low power
- Integrated balun, PA, LNA, and T/R switch
- Supports antenna diversity

3.1.5 Bluetooth

- Bluetooth v5.0 with 2-Mbps PHY rate, Long-range and LE Advertising Extensions
- Integrated balun and PA
- Supports Wi-Fi/Bluetooth coexistence

3.1.6 Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme

4 Hardware Feature Configuration

4.1 Microcontroller

The MCU subsystem consists of a 32-bit MCU, the AHB/APB bus matrix, internal RAM/ROM with ROM patch function, the flash controller and the system peripherals including Direct Memory Access (DMA) engine and the General-Purpose Timer (GPT). The MT7931 features an Arm Cortex-M33 processor, which is the most energy efficient Arm processor currently available. It supports clock rates up to 200 MHz when core power is 0.7V and 300 MHz when core power is 0.8V.

The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The MT7931 includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provides other memory protection features. The MT7931 also includes FPU in Cortex-M33 MCU.

4.2 Power Supply

Power up with a Micro-USB connector. An on-board switching regulator provides voltage of 3.3V for the MT7931 HDK based on the MT7931, if the power is supplied from an on-board Micro-USB connector **CON6** (Figure 2). Note that the jumpers **J46**, **J33**, **J32, JP4** pin2 and pin3 and **JP7** pin2 and pin3 are required to be set on. More details on the jumpers can be found in Table 1.

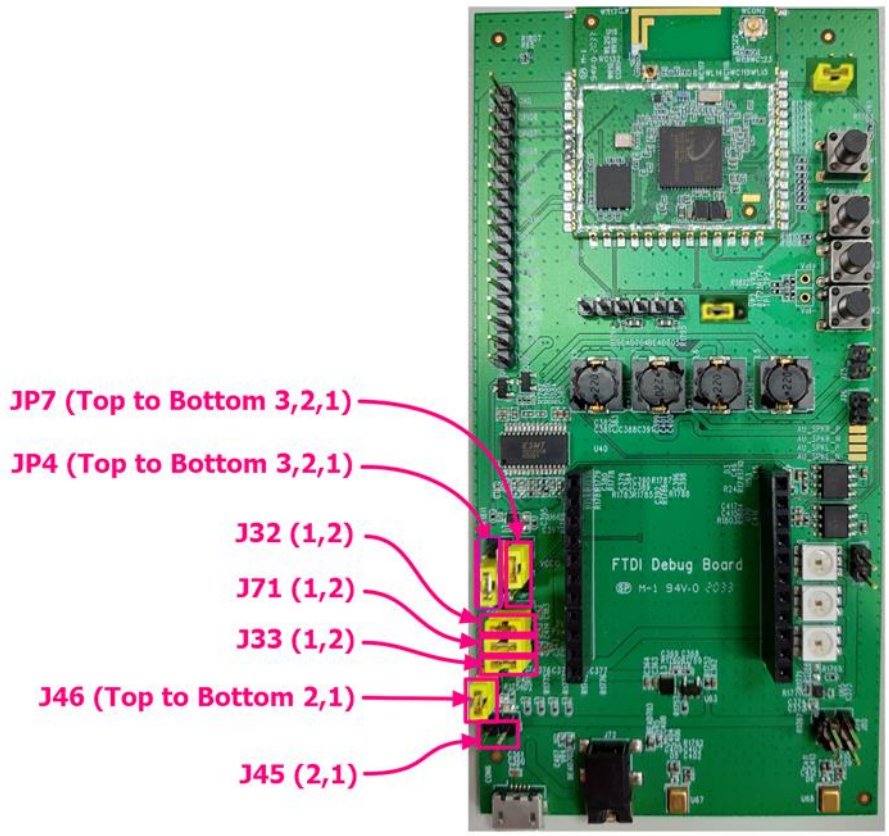

Figure 8. Default power jumper plot

Table 1. Jumper settings for system power input through USB connection

Jumper	Usage	Comments
J45	External 5V power supply	Use external power source to supply 5V voltage to MT7931 DRQFN RFB. Pin1 is 5V source. Pin2 is GND.
J46	Current measurement (3V3)	Measure the current flow in the MT7931 DRQFN RFB.
J33	3V3 for external components	Measure the current flow in the MT7931.
J71	Reserved for extra 3V3 request for other components	
JP8	Flash IO power (3V3 or 1V8)	Default RFB flash is 3V3 IO
J32	3V3 for external LDO (1.8V and 0.8V)	
JP4	Switch VCCIO to 3V3 power domain or 1V8 power domain	Selecting pins 1 and 2 means VCCIO uses 3V3 power domain Selecting pins 2 and 3 means VCCIO uses 1V8 power domain **Caution: The flash of MT7931_DRQFN_RFB by default uses 1V8 power domain. If you want to change VCCIO to 3V3 power domain, please rework flash to 3V3 power domain flash, for example W25Q128JVPIQ.**
JP7	Switch 1V8 VCCIO from internal PHYLDO or external LDO	Selecting pins 1 and 2 means 1V8 VCCIO from external buck component. Selecting pins 2 and 3 means 1V8 VCCIO from internal PHYLDO.

4.3 Audio

The MT7931 HDK has on-board audio connector associated with different functionalities of the board (**錯誤! 找不到參照來源。**9). For detail of audio related function, refer to Table 2.

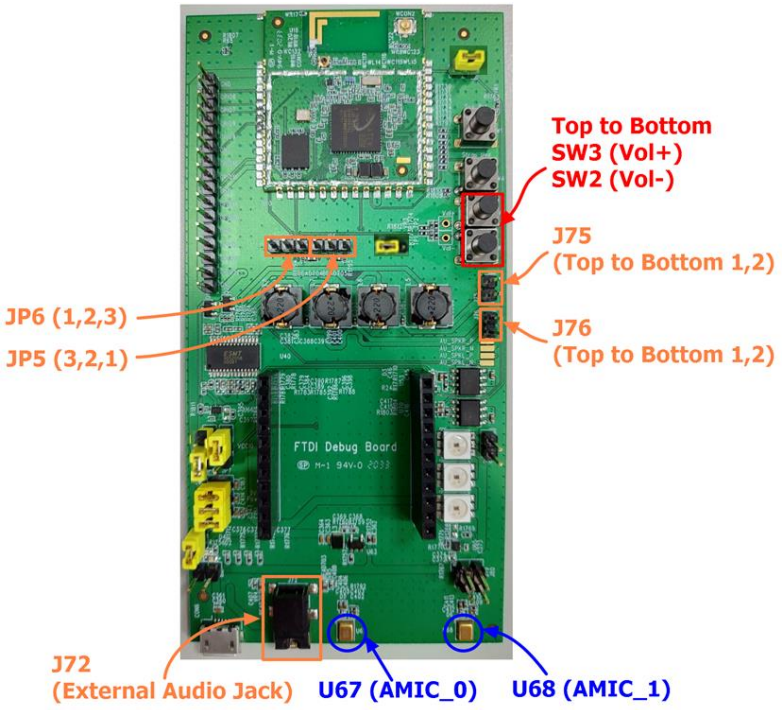

Figure 9. Audio related function

Table 2. Audio related function

Item	Detail
J72	3.5-mm audio jack for external active speaker.
J75	Audio header for left speaker
J76	Audio header for right speaker
U67	AMIC for left channel (the microphone hole is set at back side of MT7931 DRQFN RFB)
U68	AMIC for right channel (the microphone hole is set at back side of MT7931 DRQFN RFB)
SW3	Audio volume up button
SW2	Audio volume down button
JP5	This jumper switches the audio output trace: Selecting pin1 and pin2 means audio is output to audio jack. Selecting pin2 and pin3 means audio is output to J75.
JP6	This jumper switches the audio output trace: Selecting pin1 and pin2 means audio is output to J76. Selecting pin2 and pin3 means audio is output to audio jack.

4.4 Buttons

The MT7931 HDK is equipped with buttons with the following functionality.
Figure 2 shows the push buttons. Table 3 lists the function of the buttons.

Table 3. Buttons

Button	Name	Detail
SW1	SYSRST	Press SW1 to restart the MT7931 DRQFN RFB
SW2	Vol-	Audio volume down button
SW3	Vol+	Audio volume up button
SW4	Download key	Press SW4 to make MT7931 DRQFN RFB strap into download mode

4.5 Antenna

By default, the board ships with RF signals routed to the on-board printed antenna. And MT7931 DRQFN RFB reserves a conductive test component, I-PEX and mini-IPEX connector, which allows you to test the signals using a compatible cable. Refer to Figure 10 to see more detail.

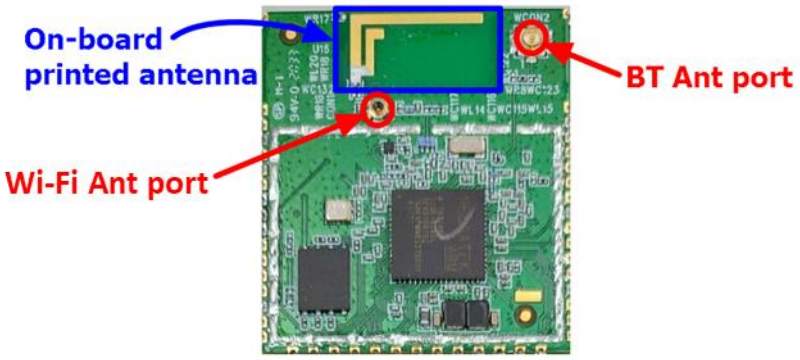

Figure 10. On-board printed antenna

4.6 RGB LED

As Figure 2 shows, the MT7931 HDK has on-board RGB LEDs **(U54, U55** and **U56)** controlled by SPIM interface. Ensure that jumpers **J79** and **J80** are connected before using RGB LED function. If you want to cascade more RGB LED, you can connect to **J78.**

4.7 Extension Connectors

The MT7931 HDK provides similar pin-out extension connectors for various sensor and device connectivity, as shown in Figure 11 and described in Table 5.

The board has 29 GPIOs multiplexed with other interfaces. Depending on the use case, you can configure each I/O functionality.

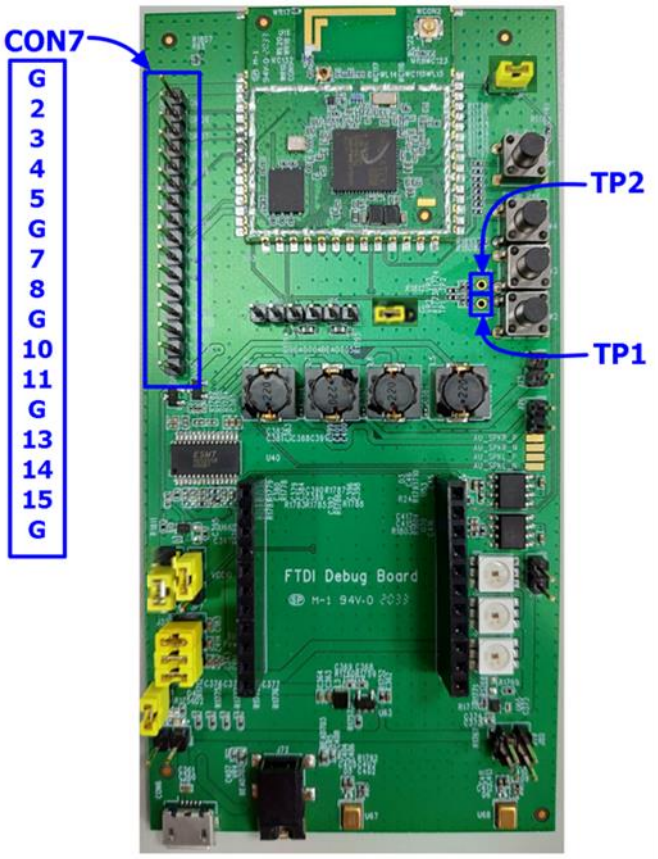

Figure 11. GPIO pin-out extension connectors

Table 4. GPIO pin-out extension connectors

Signal Name	Connector Pin Number	Signal Name	Connector Pin Number
GPIO_0	Reserved for flash	**GPIO_15**	TP2
GPIO_1	Reserved for flash	**GPIO_16**	TP1
GPIO_2	Reserved for flash	**GPIO_17**	Reserved for UART0
GPIO_3	Reserved for flash	**GPIO_18**	Reserved for UART0
GPIO_4	Reserved for flash	**GPIO_19**	CON7 – 10
GPIO_5	Reserved for flash	**GPIO_20**	CON7 – 11
GPIO_6	CON7 – 2	**GPIO_21**	CON7 – 14
GPIO_7	CON7 – 3	**GPIO_22**	CON7 – 15
GPIO_8	CON7 – 4	**GPIO_23**	Reserved for DSP UART
GPIO_9	CON7 – 5	**GPIO_24**	Reserved for DSP UART
GPIO_10	CON7 – 7	**GPIO_42**	Reserved for UART1
GPIO_11	CON7 – 8	**GPIO_44**	Reserved for UART1
GPIO_12	CON7 – 13	**GPIO_48**	Reserved for CM33 UART
GPIO_13	Reserved for ANT switch	**GPIO_50**	Reserved for CM33 UART
GPIO_14	Reserved for audio mute		

Table 5. GPIO pin multi-function definition

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CA33 EINT0
	0101	DEBUG_0	O			Debug signal
	0110	ANT_SEL0	O			Antenna Select 0
	0111	BGF_EINT_10_B	I			
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO Command
	0010	MSDC0_CMD	I/O			
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CA33 EINT1
	0101	DEBUG_1	O			Debug signal
	0110	ANT_SEL1	O			Antenna Select 1
	0111	PINMUX_EXT_INT_N_IN	I			
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 data0
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			
	0101	DEBUG_2	O			Debug signal
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CA33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 data1
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 Control
	0101	DEBUG_3	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 data2
	0011	I2SIN_DAT0	I			
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug signal
	0110	I2C0_SCL	I/O			
	0111	CM33_GPIO_EINT2	I			CA33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0010	MSDC0_DAT3	I/O			
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug signal
	0110	I2C0_SDA	I			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CA33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_TXD	O			
	0010	MSDC0_RST	O			MSDC0 reset
	0011	CONN_BT_TXD	O			
	0100	WIFI_TXD	O			
	0101	DEBUG_6	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CA33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	USB_IDDIG	I			USB OTG ID pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CA33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	USB_DRV_VBUS	O			USB OTG host mode driving enable output.
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100					
	0101	DEBUG_8	O			Debug signal
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CA33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	USB_OC	I			USB Host mode over-current input notify
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug signal
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CA33 EINT7
GPIO_B_4	0000	GPIO[16]	I/O	I	PD	GPIO 16
	0001 *	USB_VBUS_VALID	I			USB device mode VBUS detect
	0010	SPIM1_CS_N	O			SPI1 (Master) Chip Select
	0011	IR_IN	I			
	0100	I2SIN_MCK	O			I2SRX MCLK

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0101	DEBUG_10	O			Debug signal
	0110	ANT_SEL7	O			Antenna Select 7
	0111	CM33_GPIO_EINT8	I			CA33 EINT8
GPIO_B_5	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug signal
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CA33 EINT9
GPIO_B_6	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 Control
	0110	IR_IN	I			
	0111	CM33_GPIO_EINT10	I			CA33 EINT10
GPIO_B_7	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			
	0010	UART0_RTS	O			UART0 Control
	0011	I2C1_SDA	I			I2C1 Data
	0100	I2SIN_LRCK	O			I2SRX LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			
	0111	CM33_GPIO_EINT11	I			CA33 EINT11
GPIO_B_8	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCKC	I			
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	I			I2C1 clock
	0100	I2SIN_BCK	O			I2SRX BCK
	0101	DEBUG_12	O			Debug signal
	0110	PTA_EXT_IF_FACT	I			
	0111	CM33_GPIO_EINT12	I			CA33 EINT12
GPIO_B_9	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMSC	I/O			
	0010	PTA_EXT_IF_PRI	I/O			
	0011	TDMIN_LRCK	I/O			
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug signal
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CA33 EINT13
GPIO_B_10	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCKC	I			

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0010	PTA_EXT_IF_WLAN_ACT	O			
	0011	TDMIN_DI	I			
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug signal
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CA33 EINT14
GPIO_B_11	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TMSC	I/O			
	0010	DSP_URXD0	I			
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug signal
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15				CA33 EINT15
GPIO_B_12	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			
	0011	I2C0_SCL	I/O			I2C0 clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	CM33_UART_TX	O			CM33 UART TX
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CA33 EINT16
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	CM33_RSVD1	I			
	0010 *	DBSYS_SWCLK_TCLK	I			CM33 JTAG, CM33_SWD
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	CM33_RSDV3	I/O			
	0010 *	DBSYS_SWDIO_TMS	I			CM33 JTAG, CM33_SWD
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CA33 EINT18
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			
	0010	CM33_TRACE_D2	O			
	0011	KEYPAD_KPROW_1	I/O			
	0100	DSP_URXD0	I			
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0111	AUDIO_DEBUG_IN_0	I			
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			
	0010	CM33_TRACE_D0	O			
	0011	KEYPAD_KPCOL_0	I			
	0100	DSP_UTXD0	O			
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			

4.8 RTC

The MT7931 HDK features an RTC module. The clock source operates at 32.768-kHz crystal oscillator or an external clock source. The RTC has built-in accurate timer to wake up the system when the user-defined timer expires. The RTC uses a different power source from the Power Management Unit (PMU). In retention mode, the PMU is turned off while the RTC module remains powered on. The RTC module only consumes 3µA in retention mode. The RTC has a dedicated PMU control pin, RTC_PMU_EN (pin F12), which is used to turn the power on when the RTC timer expires and turn the power off to enter the hibernate mode.

4.9 FTDI Debug Board

By default, MT7931 DRQFN RFB should connect to an FTDI debug board at U69 (Figure 12). The FTDI debug board (Figure 12) allows UART signal being converted to USB signal. This debug board also provides a Micro-USB connector to connect with your PC with USB cable.

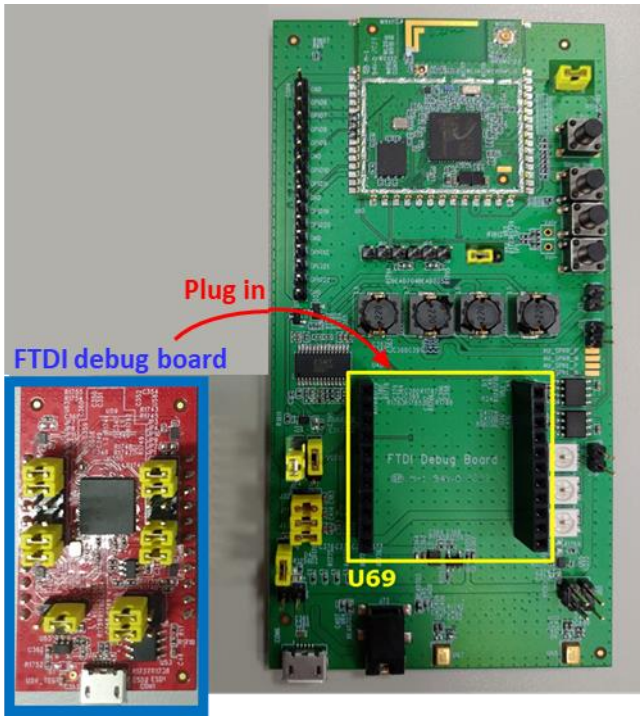

Figure 12. FTDI debug board

5 Appendix

Board name	Schematic
MT7931_DRQFN_RFB_Dougher Board	 IOT_MT7931_DR QFN_RFB_DB_4L_V
MT7931_DRQFN_RFB_Base Board	 IOT_MT7931_DR QFN_RFB_BASE_4L
MT7931_FTDI_Debug Board_V10	 IOT_MT7933_FTDI _debug_board_4L

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