MT793X IoT SDK for GDMA User Guide

Version: 1.0
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Version History

Version	Date	Description
0.1	2021-01-04	Initial draft

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1 Overview

This document introduces the hardware and software features of of GDMA, and provides a GDMA programming guide.

2 Instruction

2.1 DMA Concept

Direct Memory Access (DMA) is the operation in which data is directly copied (transported) from one resource to another resource, for example DRAM, in a computer system without the involvement of the CPU.

2.2 DMA Efficiency

DMA requires internal buffer to make data transfer smoothly.
The minimum size of transfer data is 1 byte.

2.3 Architecture Diagram

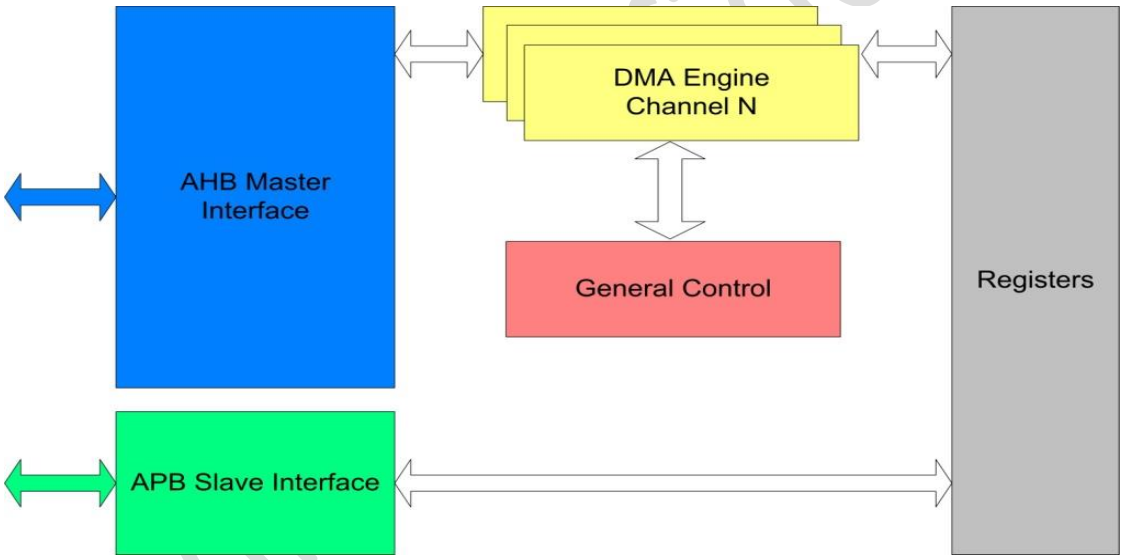

Figure 1. GDMA Architecture Diagram

3 Feature

3.1 Block Diagram

Slave X and Slave Y may be DRAM or SRAM.
GDMA can work in polling mode or interrupt mode.
Data is transferred in AXI bus.

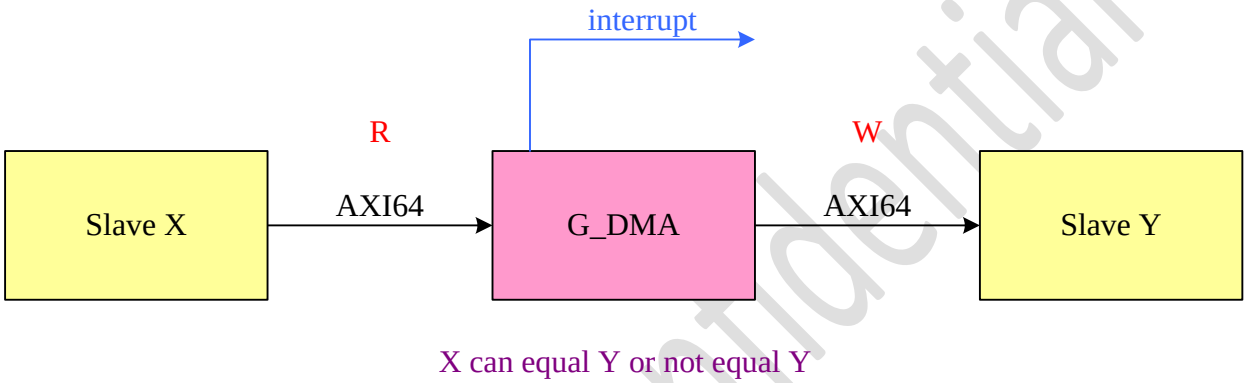

Figure 2. GDMA Block Diagram

3.2 Ring Buffer and Double Buffer

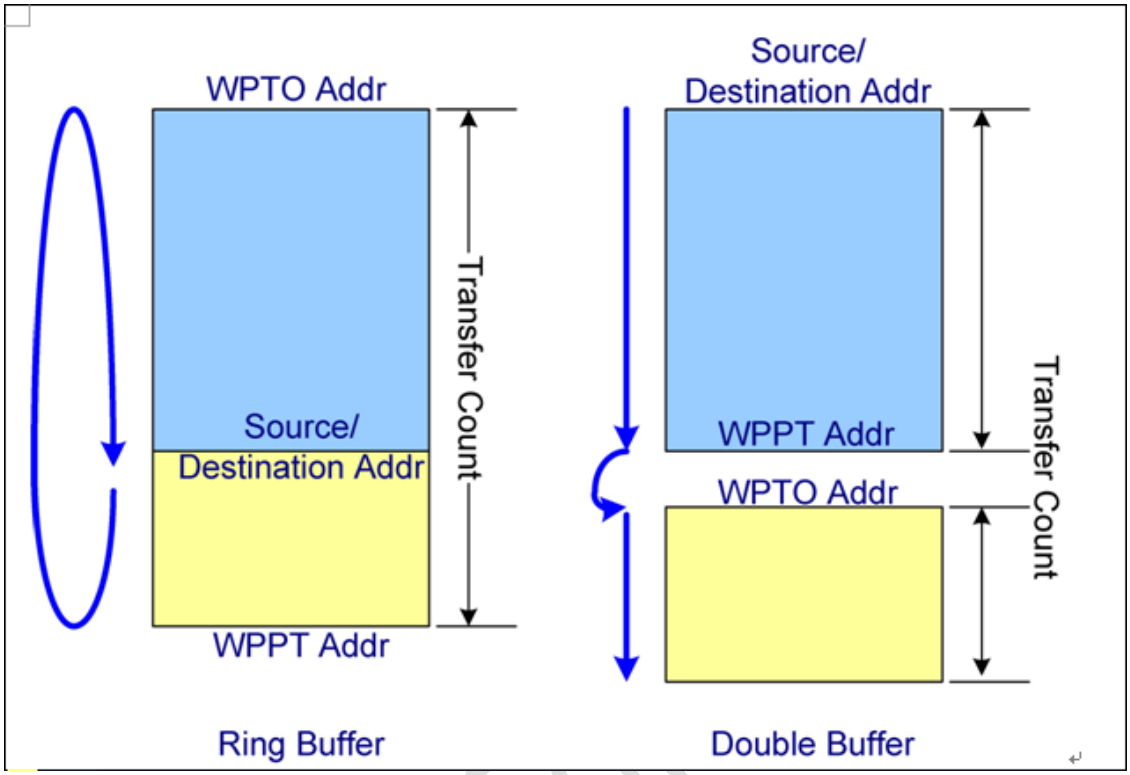

Figure 3. Ring Buffer/Double Buffer

There is only one interrupt signal sent out when all data tranfers are done in the ring buffer and double buffer mode.

3.3 Limiter

The limiter improves bus usage and ensures not too many bus resources are occupied by DMA to avoid damaging the performance of other tasks, especially real-time tasks.

The transaction is issued with delay for a pre-configured cycle period. This does not affect the clock frequency of GDMA.

The period is from 0 to 1023 clock cycles. The slow-down counter only slows down the read transaction, and does not affect the write transaction. This way, the overall throughput is reduced.

SLOW_EN (CQ_DMA+0x0018)[2] is the enable bit of bandwidth limiter function and SLOW_CNT (CQ_DMA+0x0018)[14:5] is the delay cycle period.

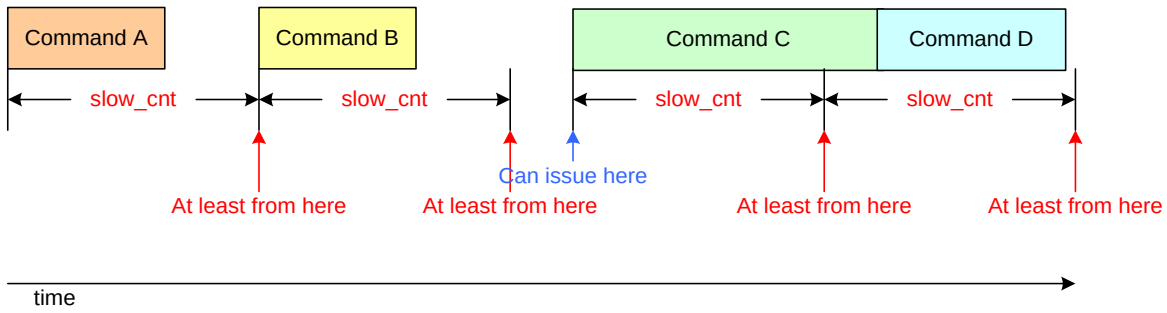

Figure 4. Limiter

3.4 Fixed Address

Both the source address and destination address support the fixed mode.

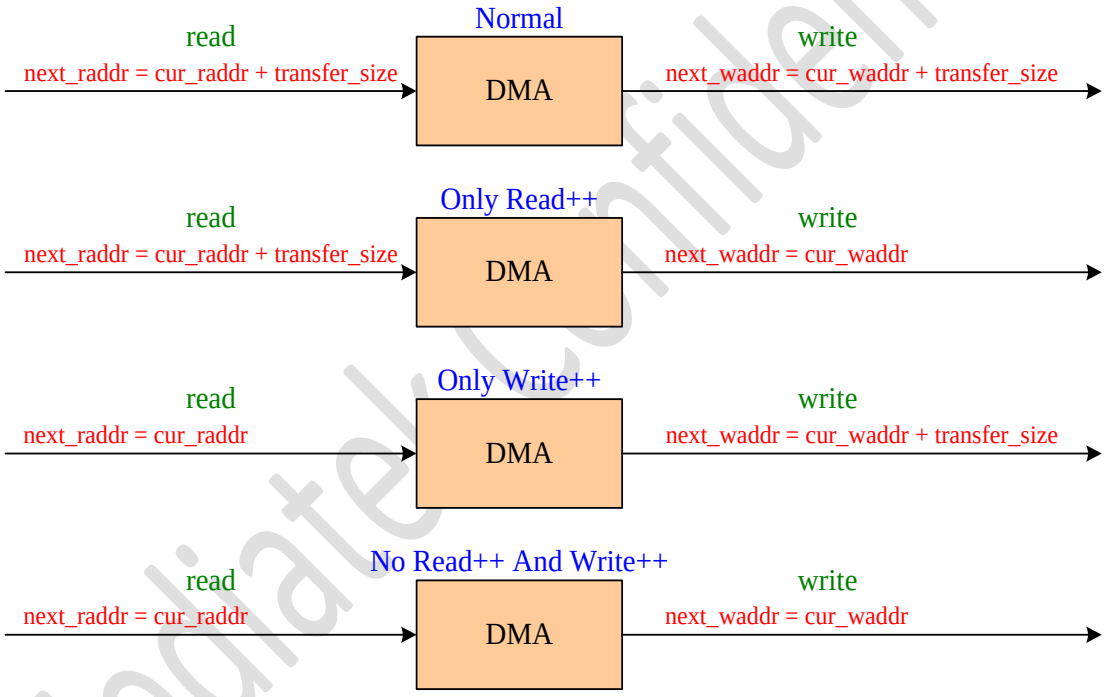

Figure 5. Fixed Address

3.5 Address Alignment

The source and destination addresses can be any byte alignment. This address is changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR is treated as FIX_PATTERN.

4 Programming Guide

4.1 Polling Mode

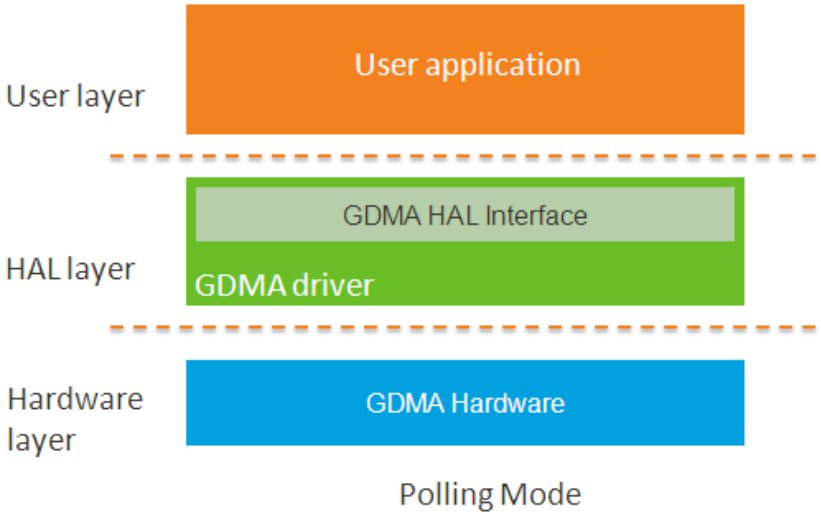

Figure 6. Polling Mode

4.2 Interrupt Mode

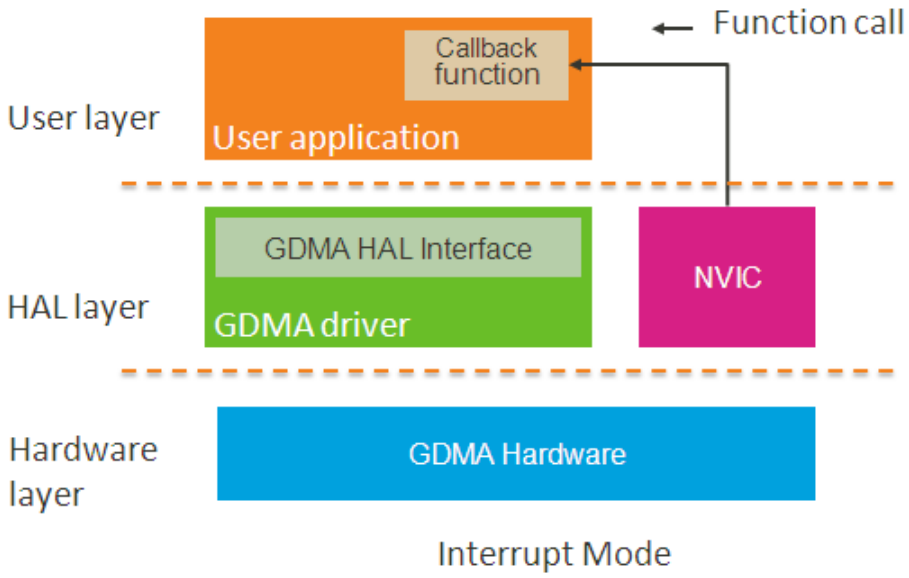

Figure 7. Interrupt Mode

4.3 GDMA APIs List

Table 1. API List

NUM	APIs list
1	hal_gdma_status_t hal_gdma_init(hal_gdma_channel_t channel)
2	hal_gdma_status_t hal_gdma_deinit(hal_gdma_channel_t channel)
3	hal_gdma_status_t hal_gdma_start_polling(hal_gdma_channel_t channel,uint32_t destination_address, uint32_t source_address, uint32_t data_length)
4	hal_gdma_status_t hal_gdma_start_interrupt(hal_gdma_channel_t channel, uint32_t destination_address,uint32_t source_address, uint32_t data_length)
5	hal_gdma_status_t hal_gdma_stop(hal_gdma_channel_t channel)
6	hal_gdma_status_t hal_gdma_register_callback(hal_gdma_channel_t channel, hal_gdma_callback_t callback, void *user_data)
7	hal_gdma_status_t hal_gdma_get_running_status(hal_gdma_channel_t channel, hal_gdma_running_status_t *running_status)

4.4 Programming Sequence

- Set source and destination addresses in GDMA_SRC and GDMA_DES.
- Select the burst, bus size or interrupt option in GDMA_CON.
- Set transfer times in GDMA_COUNT.
- Set GDMA_START to 1 to start this channel. Set GDMA_START to 0 to stop the DMA action.
- Note: The configurations in the above 4 steps are logged into DMA state machine ONLY when GDMA_START is set from 0 to 1.
- When transaction is over, the processor should receive an interrupt. If the interrupt is not enabled, the processor can poll status in global status. For more details, GDMA_RLCT shows how many transfers are left.

4.5 Configuration

Path:

project\<borad>\apps\<application>\inc\ hal_feature_config.h

```
/*****************************************************************************
* module ON or OFF feature option,only option in this temple
*****************************************************************************/

//#define HAL_ACCDET_MODULE_ENABLED
#define HAL_ADC_MODULE_ENABLED
#define HAL_AES_MODULE_ENABLED
//#define HAL_AUDIO_MODULE_ENABLED
#define HAL_CACHE_MODULE_ENABLED
#define HAL_DES_MODULE_ENABLED
#define HAL_EINT_MODULE_ENABLED
#define HAL_FLASH_MODULE_ENABLED
#define HAL_GDMA_MODULE_ENABLED
#define HAL_GPC_MODULE_ENABLED
#define HAL_GPIO_MODULE_ENABLED
#define HAL_GPT_MODULE_ENABLED
#define HAL_I2C_MASTER_MODULE_ENABLED
#define HAL_I2S_MODULE_ENABLED
#define HAL_IRRX_MODULE_ENABLED
#define HAL_IRTX_MODULE_ENABLED
//#define HAL_ISINK_MODULE_ENABLED
//#define HAL_KEYPAD_MODULE_ENABLED
```

Figure 8.Configuration

5 Register Map

Module name: CQ_DMA Base address: (+0x34408000)

Address	Name	Width	Register Function
34408000	CQ_DMA_G_DMA_0_INT_FLAG	32	General DMA Interrupt Flag Register
34408004	CQ_DMA_G_DMA_0_INT_EN	32	General DMA Interrupt Enable Register
34408008	CQ_DMA_G_DMA_0_EN	32	General DMA Enable Register
3440800C	CQ_DMA_G_DMA_0_RST	32	General DMA Reset Register
34408010	CQ_DMA_G_DMA_0_STOP	32	General DMA Stop Register
34408014	CQ_DMA_G_DMA_0_FLUSH	32	General DMA Flush Register
34408018	CQ_DMA_G_DMA_0_CON	32	General DMA Control Register
3440801C	CQ_DMA_G_DMA_0_SRC_ADDR	32	General DMA Source Address Register
34408020	CQ_DMA_G_DMA_0_DST_ADDR	32	General DMA Destination Address Register
34408024	CQ_DMA_G_DMA_0_LEN1	32	General DMA Transfer Length 1 Register
34408028	CQ_DMA_G_DMA_0_LEN2	32	General DMA Transfer Length 2 Register
3440802C	CQ_DMA_G_DMA_0_JUMP_ADDR	32	General DMA Jump Address Register
34408030	CQ_DMA_G_DMA_0_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
34408034	CQ_DMA_G_DMA_0_CONNECT	32	General DMA Connect Register
34408038	CQ_DMA_G_DMA_0_AXIATTR	32	General DMA AXI Attribute Register
3440803C	CQ_DMA_G_DMA_0_SEC_EN	32	General DMA Security Enable Register
34408040	CQ_DMA_G_DMA_0_APB_LATADDR	32	General DMA Security Latch Address Register
34408044	CQ_DMA_G_DMA_0_ABORT	32	General DMA Security Abort Register
34408048	CQ_DMA_G_DMA_0_DCM_EN	32	General DMA HW DCM Enable
34408050	CQ_DMA_G_DMA_0_DEBUG	32	General DMA Debug
34408060	CQ_DMA_G_DMA_0_SRC_ADDR2	32	General DMA Source Address Register
34408064	CQ_DMA_G_DMA_0_DST_ADDR2	32	General DMA Destination Address Register
34408068	CQ_DMA_G_DMA_0_JUMP_ADDR2	32	General DMA Jump Address Register

34408080	CQ_DMA_G_DMA_1_INT_FLAG	32	General DMA Interrupt Flag Register
34408084	CQ_DMA_G_DMA_1_INT_EN	32	General DMA Interrupt Enable Register
34408088	CQ_DMA_G_DMA_1_EN	32	General DMA Enable Register
3440808C	CQ_DMA_G_DMA_1_RST	32	General DMA Reset Register
34408090	CQ_DMA_G_DMA_1_STOP	32	General DMA Stop Register
34408094	CQ_DMA_G_DMA_1_FLUSH	32	General DMA Flush Register
34408098	CQ_DMA_G_DMA_1_CON	32	General DMA Control Register
3440809C	CQ_DMA_G_DMA_1_SRC_ADDR	32	General DMA Source Address Register
344080A0	CQ_DMA_G_DMA_1_DST_ADDR	32	General DMA Destination Address Register
344080A4	CQ_DMA_G_DMA_1_LEN1	32	General DMA Transfer Length 1 Register
344080A8	CQ_DMA_G_DMA_1_LEN2	32	General DMA Transfer Length 2 Register
344080AC	CQ_DMA_G_DMA_1_JUMP_ADDR	32	General DMA Jump Address Register
344080B0	CQ_DMA_G_DMA_1_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
344080B4	CQ_DMA_G_DMA_1_CONNECT	32	General DMA Connect Register
344080B8	CQ_DMA_G_DMA_1_AXIATTR	32	General DMA AXI Attribute Register
344080BC	CQ_DMA_G_DMA_1_SEC_EN	32	General DMA Security Enable Register
344080C0	CQ_DMA_G_DMA_1_APB_LATADDR	32	General DMA Security Latch Address Register
344080C4	CQ_DMA_G_DMA_1_ABORT	32	General DMA Security Abort Register
344080C8	CQ_DMA_G_DMA_1_DCM_EN	32	General DMA HW DCM Enable
344080D0	CQ_DMA_G_DMA_1_DEBUG	32	General DMA Debug
344080E0	CQ_DMA_G_DMA_1_SRC_ADDR2	32	General DMA Source Address Register
344080E4	CQ_DMA_G_DMA_1_DST_ADDR2	32	General DMA Destination Address Register
344080E8	CQ_DMA_G_DMA_1_JUMP_ADDR2	32	General DMA Jump Address Register
34408100	CQ_DMA_G_DMA_2_INT_FLAG	32	General DMA Interrupt Flag Register
34408104	CQ_DMA_G_DMA_2_INT_EN	32	General DMA Interrupt Enable Register
34408108	CQ_DMA_G_DMA_2_EN	32	General DMA Enable Register
3440810C	CQ_DMA_G_DMA_2_RST	32	General DMA Reset Register

34408110	CQ_DMA_G_DMA_2_STOP	32	General DMA Stop Register
34408114	CQ_DMA_G_DMA_2_FLUSH	32	General DMA Flush Register
34408118	CQ_DMA_G_DMA_2_CON	32	General DMA Control Register
3440811C	CQ_DMA_G_DMA_2_SRC_ADDR	32	General DMA Source Address Register
34408120	CQ_DMA_G_DMA_2_DST_ADDR	32	General DMA Destination Address Register
34408124	CQ_DMA_G_DMA_2_LEN1	32	General DMA Transfer Length 1 Register
34408128	CQ_DMA_G_DMA_2_LEN2	32	General DMA Transfer Length 2 Register
3440812C	CQ_DMA_G_DMA_2_JUMP_ADDR	32	General DMA Jump Address Register
34408130	CQ_DMA_G_DMA_2_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
34408134	CQ_DMA_G_DMA_2_CONNECT	32	General DMA Connect Register
34408138	CQ_DMA_G_DMA_2_AXIATTR	32	General DMA AXI Attribute Register
3440813C	CQ_DMA_G_DMA_2_SEC_EN	32	General DMA Security Enable Register
34408140	CQ_DMA_G_DMA_2_APB_LATADDR	32	General DMA Security Latch Address Register
34408144	CQ_DMA_G_DMA_2_ABORT	32	General DMA Security Abort Register
34408148	CQ_DMA_G_DMA_2_DCM_EN	32	General DMA HW DCM Enable
34408150	CQ_DMA_G_DMA_2_DEBUG	32	General DMA Debug
34408160	CQ_DMA_G_DMA_2_SRC_ADDR2	32	General DMA Source Address Register
34408164	CQ_DMA_G_DMA_2_DST_ADDR2	32	General DMA Destination Address Register
34408168	CQ_DMA_G_DMA_2_JUMP_ADDR2	32	General DMA Jump Address Register

34408000 CQ_DMA_G_DMA_0_INT_FLAG General DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLAG**

Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG	**This flag will be raised when DMA is finished.** Write 0 to clear it. 1. When normal operation is done, EN will be set from 1 to 0, and the interrupt flag will be set to 1. 2. Set STOP=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 3. Set FLUSH=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 4. Set WARM_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1. 5. Set HARD_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1.

34408004 CQ_DMA_G_DMA_0_INT_EN General DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** Only when this bit is set to 1 will the interrupt be sent to CPU to receive this interrupt. However, even without this bit set to 1, the flag can still be set to 1 when DMA is finished. 0: Disable 1: Enable

Bit(s)	Name	Description

34408008 CQ_DMA_G_DMA_0_EN General DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables general DMA** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

3440800C CQ_DMA_G_DMA_0_RST General DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW

Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to be 0, and HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

34408010 CQ_DMA_G_DMA_0_STOP General DMA Stop Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**STOP**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses general DMA** Set PAUSE to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops general DMA** Set STOP to 1 to stop DMA and wait for EN to become 0 then set STOP back to 0 to finish the stop mechanism.

Bit(s)	Name	Description
		When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

34408014 CQ_DMA_G_DMA_0_FLUSH General DMA Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes general DMA** Set FLUSH to 1 to stop DMA and allow DMA to flush its internal buffer residual data to the outer memory. After flush is finished, DMA will set EN to 0 to stop DMA. There may still be data not transferred (len may not be 0 after EN = 0). SW sets FLUSH to 1 and waits for EN to become 0 then set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

34408018 CQ_DMA_G_DMA_0_CON General DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**RSIZE**				**WSIZE**					**WRAP_SEL**		**BURST_LEN**		

Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_EN	SLOW_CNT										RADDR_FIX_EN	WADDR_FIX_EN	SLOW_EN	FIX_EN	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only valid when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only valid when WADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source) 1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid value: 0~7. The best case is to set it to 3 (4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8

Bit(s)	Name	Description
		6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN=1 and WRAP_SEL=1, WADDR_FIX_EN will have no function. Likewise, if WRAP_EN=1 and WRAP_SEL=0, RADDR_FIX_EN will have no function. When FIX_EN=1 and WRAP_EN=1, WRAP_SEL can only be set to 1. The read side cannot be set to wrap. 0: Disable 1: Enable
14:5	SLOW_CNT	**General DMA slow-down counter** Only slows down the read side; the overall throughput will also be reduced. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN=1 or "WRAP_EN=1 and WRAP_SEL=0", this bit will not function. When this function is enabled, note the following limits on DMA: 1. src_addr must be 8-byte aligned. 2. The read transaction size depends on RSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed 1: Fixed
3	WADDR_FIX_EN	**General DMA fixed write address** When "WRAP_EN=1 and WRAP_SEL=1", this bit will not function. When this function is enabled, note the following limits on DMA: 1. dst_addr must be 8-byte aligned. 2. The write transaction size depends on WSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed 1: Fixed
2	SLOW_EN	**Enables general DMA slow-down**

Bit(s)	Name	Description
		0: Disable 1: Enable
1	FIX_EN	**General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, i.e. when FIX_EN=1, RADDR_FIX_EN will be ignored. 0: Not use fixed pattern 1: Use fixed pattern

3440801C **CQ_DMA_G_DMA_0_SRC_ADDR** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** Can be any byte alignment. This address will be changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN.

34408020 **CQ_DMA_G_DMA_0_DST_ADDR** **General DMA Destination Address Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**General DMA destination address** Can be any byte alignment. This address will be changed after each bus transaction. However, when WADDR_FIX_EN = 1, dst_addr must be 8-byte aligned.

34408024 CQ_DMA_G_DMA_0_LEN1 General DMA Transfer Length 1 Register 0FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN1											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:0	LEN1	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. When read fix and write wrap is set, LEN1 must be a multiple number of the byte number indicated by RSIZE. 0: 0 byte transfer 1: 1 byte transfer

34408028 CQ_DMA_G_DMA_0_LEN2 General DMA Transfer Length 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	LEN2	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

3440802C **CQ_DMA_G_DMA_0_JUMP_ADDR** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JUMP_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JUMP_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** Can be any byte alignment. Only valid when wrap_en = 1.

34408030 CQ_DMA_G_DMA_0_INT_BUF_SIZE General DMA Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	**General DMA size of data in internal buffer**

34408034 CQ_DMA_G_DMA_0_CONNECT General DMA Connect Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	RATIO	**General DMA request/ack connection ratio** 0: 1/2 1: 1/1
2	DIR	**General DMA request/ack connection direction**

Bit(s)	Name	Description
		0: req/ack connected to write side
		1: req/ack connected to read side
1:0	CONNECT	**General DMA request/ack connection**
		1, 2 and 3 are only valid when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1.
		0: No connection
		1: Connect set1 (req/ack)
		2: Connect set2 (req/ack)
		3: Connect set3 (req/ack)

34408038 **CQ_DMA_G_DMA_0_AXIATTR** **General DMA AXI Attribute Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	**General DMA AXI AWUSER signal**
		0: Go through non-coherent bus
		1: Go through coherent bus. Set up this bit when the destination is SYSRAM.
19:16	WCACHE	**General DMA AXI AWCACHE signal**
4	RUSER	**General DMA AXI ARUSER signal**
		0: Go through non-coherent bus
		1: Go through coherent bus. Set up this bit when the source is SYSRAM.
3:0	RCACHE	**General DMA AXI ARCACHE signal**

Bit(s)	Name	Description

3440803C CQ_DMA_G_DMA_0_SEC_EN General DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DOMAIN_EN		PDOMAIN_CFG			DOMAIN_CFG				SEC_EN
Type							RW		RW			RW				RW
Reset							0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	DOMAIN_EN	**Sets up apb domain value check enable**
7:5	PDOMAIN_CFG	**Sets up apb domain value**
4:1	DOMAIN_CFG	**Sets up axi domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

34408040 CQ_DMA_G_DMA_0_APB_LATADDR General DMA Security Latch Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	**When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.**

34408044 CQ_DMA_G_DMA_0_ABORT General DMA Security Abort Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VID	W_VID				APB_ABORT								
Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID, and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	**Indicate that APB Read violation happens**
28	W_VID	**Indicate that APB Write violation happens**
24	APB_ABORT	**When APB read/write violation happens, this bit will be 1'b1**

34408048 CQ_DMA_G_DMA_0_DCM_EN General DMA HW DCM Enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	DCM_EN	**Sets up GDMA HW DCM enable** If dcm_en = 0, DMA will not auto gate the clock when DMA is idle.

34408050 CQ_DMA_G_DMA_0_DEBUG General DMA Debug 00000013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				1	0	0	1	1

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

Bit(s)	Name	Description

34408060 **CQ_DMA_G_DMA_0_SRC_ADDR2** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SRC_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SRC_ADDR2	**General DMA source address bit[32]**

34408064 **CQ_DMA_G_DMA_0_DST_ADDR2** **General DMA Destination Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DST_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DST_ADDR2	**General DMA destination address [32]**

34408068 **CQ_DMA_G_DMA_0_JUMP_ADDR2** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**JUMP_ADDR2**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	JUMP_ADDR2	**General DMA jump address [32]**

34408080 **CQ_DMA_G_DMA_1_INT_FLAG** **General DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLAG**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG	**This flag will be raised when DMA is finished.** Write 0 to clear it. 1. When normal operation is done, EN will be set from 1 to 0, and the interrupt flag will be set to 1.

Bit(s)	Name	Description
		2. Set STOP=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 3. Set FLUSH=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 4. Set WARM_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1. 5. Set HARD_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1.

34408084 CQ_DMA_G_DMA_1_INT_EN General DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** Only when this bit is set to 1 will the interrupt be sent to CPU to receive this interrupt. However, even without this bit set to 1, the flag can still be set to 1 when DMA is finished. 0: Disable 1: Enable

34408088 CQ_DMA_G_DMA_1_EN General DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables general DMA** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

3440808C CQ_DMA_G_DMA_1_RST General DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)**

Bit(s)	Name	Description
		SW sets WARM_RST to 1 and waits for EN to be 0, and HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

34408090 CQ_DMA_G_DMA_1_STOP General DMA Stop Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**STOP**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses general DMA** Set PAUSE to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops general DMA** Set STOP to 1 to stop DMA and wait for EN to become 0 then set STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

34408094 CQ_DMA_G_DMA_1_FLUSH General DMA Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes general DMA** Set FLUSH to 1 to stop DMA and allow DMA to flush its internal buffer residual data to the outer memory. After flush is finished, DMA will set EN to 0 to stop DMA. There may still be data not transferred (len may not be 0 after EN = 0). SW sets FLUSH to 1 and waits for EN to become 0 then set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

34408098 CQ_DMA_G_DMA_1_CON General DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RSIZE				WSIZE					WRAP_SEL		BURST_LEN		
Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_EN	SLOW_CNT										RADDR_FIX_EN	WADDR_FIX_EN	SLOW_EN	FIX_EN	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only valid when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only valid when WADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source) 1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid value: 0~7. The best case is to set it to 3 (4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8 6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN=1 and WRAP_SEL=1, WADDR_FIX_EN will have no function. Likewise, if WRAP_EN=1 and WRAP_SEL=0, RADDR_FIX_EN will have no function. When FIX_EN=1 and WRAP_EN=1, WRAP_SEL can only be set to 1. The read side cannot be set to wrap. 0: Disable 1: Enable

Bit(s)	Name	Description
14:5	SLOW_CNT	**General DMA slow-down counter** Only slows down the read side; the overall throughput will also be reduced. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN=1 or "WRAP_EN=1 and WRAP_SEL=0", this bit will not function. When this function is enabled, note the following limits on DMA: 1. src_addr must be 8-byte aligned. 2. The read transaction size depends on RSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed 1: Fixed
3	WADDR_FIX_EN	**General DMA fixed write address** When "WRAP_EN=1 and WRAP_SEL=1", this bit will not function. When this function is enabled, note the following limits on DMA: 1. dst_addr must be 8-byte aligned. 2. The write transaction size depends on WSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed 1: Fixed
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, i.e. when FIX_EN=1, RADDR_FIX_EN will be ignored. 0: Not use fixed pattern 1: Use fixed pattern

3440809C **CQ_DMA_G_DMA_1_SRC_ADDR** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** Can be any byte alignment. This address will be changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN.

344080A0 **CQ_DMA_G_DMA_1_DST_ADDR** **General DMA Destination Address Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**General DMA destination address** Can be any byte alignment. This address will be changed after each bus transaction. However, when WADDR_FIX_EN = 1, dst_addr must be 8-byte aligned.

Bit(s)	Name	Description

344080A4 CQ_DMA_G_DMA_1_LEN1 General DMA Transfer Length 1 Register 0FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN1											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:0	LEN1	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. When read fix and write wrap is set, LEN1 must be a multiple number of the byte number indicated by RSIZE. 0: 0 byte transfer 1: 1 byte transfer

344080A8 CQ_DMA_G_DMA_1_LEN2 General DMA Transfer Length 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	LEN2	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

344080AC **CQ_DMA_G_DMA_1_JUMP_ADDR** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JUMP_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JUMP_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** Can be any byte alignment. Only valid when wrap_en = 1.

344080B0 **CQ_DMA_G_DMA_1_INT_BUF_SIZE** **General DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							

Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	**General DMA size of data in internal buffer**

344080B4 **CQ_DMA_G_DMA_1_CONNECT** **General DMA Connect Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	RATIO	**General DMA request/ack connection ratio** 0: 1/2 1: 1/1
2	DIR	**General DMA request/ack connection direction** 0: req/ack connected to write side 1: req/ack connected to read side
1:0	CONNECT	**General DMA request/ack connection** 1, 2 and 3 are only valid when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1. 0: No connection 1: Connect set1 (req/ack) 2: Connect set2 (req/ack) 3: Connect set3 (req/ack)

344080B8 CQ_DMA_G_DMA_1_AXIATTR General DMA AXI Attribute Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	**General DMA AXI AWUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set up this bit when the destination is SYSRAM.
19:16	WCACHE	**General DMA AXI AWCACHE signal**
4	RUSER	**General DMA AXI ARUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set up this bit when the source is SYSRAM.
3:0	RCACHE	**General DMA AXI ARCACHE signal**

344080BC CQ_DMA_G_DMA_1_SEC_EN General DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DOMAIN_EN		PDOMAIN_CFG			DOMAIN_CFG				SEC_EN
Type							RW		RW			RW				RW

Reset							0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	DOMAIN_EN	**Sets up apb domain value check enable**
7:5	PDOMAIN_CFG	**Sets up apb domain value**
4:1	DOMAIN_CFG	**Sets up axi domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

344080C0 CQ_DMA_G_DMA_1_APB_LATADDR General DMA Security Latch Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	**When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.**

344080C4 CQ_DMA_G_DMA_1_ABORT General DMA Security Abort Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VID	W_VID				APB_ABORT								

Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID, and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	**Indicate that APB Read violation happens**
28	W_VID	**Indicate that APB Write violation happens**
24	APB_ABORT	**When APB read/write violation happens, this bit will be 1'b1**

344080C8 **CQ_DMA_G_DMA_1_DCM_EN** **General DMA HW DCM Enable** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	DCM_EN	**Sets up GDMA HW DCM enable** If dcm_en = 0, DMA will not auto gate the clock when DMA is idle.

344080D0 CQ_DMA_G_DMA_1_DEBUG General DMA Debug 00000013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				1	0	0	1	1

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

344080E0 CQ_DMA_G_DMA_1_SRC_ADDR2 General DMA Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SRC_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SRC_ADDR2	**General DMA source address bit[32]**

344080E4 **CQ_DMA_G_DMA_1_DST_ADDR2** **General DMA Destination Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**DST_ADDR2**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DST_ADDR2	**General DMA destination address [32]**

344080E8 **CQ_DMA_G_DMA_1_JUMP_ADDR2** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**JUMP_ADDR2**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	JUMP_ADDR2	**General DMA jump address [32]**

34408100 CQ_DMA_G_DMA_2_INT_FLAG General DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG	**This flag will be raised when DMA is finished.** Write 0 to clear it. 1. When normal operation is done, EN will be set from 1 to 0, and the interrupt flag will be set to 1. 2. Set STOP=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 3. Set FLUSH=1 and operation will be done, then EN will be set from 1 to 0, and the interrupt flag will be set to 1. 4. Set WARM_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1. 5. Set HARD_RST=1 and operation will be done, then EN will be set from 1 to 0, but the interrupt flag will not be set to 1.

34408104 CQ_DMA_G_DMA_2_INT_EN General DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** Only when this bit is set to 1 will the interrupt be sent to CPU to receive this interrupt. However, even without this bit set to 1, the flag can still be set to 1 when DMA is finished. 0: Disable 1: Enable

34408108 CQ_DMA_G_DMA_2_EN General DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables general DMA** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

Bit(s)	Name	Description

3440810C CQ_DMA_G_DMA_2_RST General DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HARD_RST**	**WARM_RST**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to be 0, and HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

34408110 CQ_DMA_G_DMA_2_STOP General DMA Stop Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses general DMA** Set PAUSE to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops general DMA** Set STOP to 1 to stop DMA and wait for EN to become 0 then set STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

34408114 CQ_DMA_G_DMA_2_FLUSH General DMA Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes general DMA** Set FLUSH to 1 to stop DMA and allow DMA to flush its internal buffer residual data to the outer memory. After flush is finished, DMA will set EN to 0 to stop DMA. There may still be data not transferred (len may not be 0 after EN = 0).

Bit(s)	Name	Description
		SW sets FLUSH to 1 and waits for EN to become 0 then set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

34408118 CQ_DMA_G_DMA_2_CON General DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RSIZE				WSIZE					WRAP_SEL		BURST_LEN		
Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_EN	SLOW_CNT										RADDR_FIX_EN	WADDR_FIX_EN	SLOW_EN	FIX_EN	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only valid when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only valid when WADDR_FIX_EN = 1. 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 bytes. 3: Transaction size is 1 byte.

Bit(s)	Name	Description
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source) 1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid value: 0~7. The best case is to set it to 3 (4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8 6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN=1 and WRAP_SEL=1, WADDR_FIX_EN will have no function. Likewise, if WRAP_EN=1 and WRAP_SEL=0, RADDR_FIX_EN will have no function. When FIX_EN=1 and WRAP_EN=1, WRAP_SEL can only be set to 1. The read side cannot be set to wrap. 0: Disable 1: Enable
14:5	SLOW_CNT	**General DMA slow-down counter** Only slows down the read side; the overall throughput will also be reduced. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN=1 or "WRAP_EN=1 and WRAP_SEL=0", this bit will not function. When this function is enabled, note the following limits on DMA: 1. src_addr must be 8-byte aligned. 2. The read transaction size depends on RSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed

Bit(s)	Name	Description
		1: Fixed
3	WADDR_FIX_EN	**General DMA fixed write address** When "WRAP_EN=1 and WRAP_SEL=1", this bit will not function. When this function is enabled, note the following limits on DMA: 1. dst_addr must be 8-byte aligned. 2. The write transaction size depends on WSIZE. 3. The burst length is always single. 4. dst_addr must not be at EMI. 0: Not fixed 1: Fixed
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, i.e. when FIX_EN=1, RADDR_FIX_EN will be ignored. 0: Not use fixed pattern 1: Use fixed pattern

3440811C **CQ_DMA_G_DMA_2_SRC_ADDR** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address**

Bit(s)	Name	Description
		Can be any byte alignment. This address will be changed after each bus transaction. However, when RADDR_FIX_EN = 1, src_addr must be 8-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN.

34408120 CQ_DMA_G_DMA_2_DST_ADDR General DMA Destination Address Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**General DMA destination address** Can be any byte alignment. This address will be changed after each bus transaction. However, when WADDR_FIX_EN = 1, dst_addr must be 8-byte aligned.

34408124 CQ_DMA_G_DMA_2_LEN1 General DMA Transfer Length 1 Register 0FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN1											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:0	LEN1	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. When read fix and write wrap is set, LEN1 must be a multiple number of the byte number indicated by RSIZE. 0: 0 byte transfer 1: 1 byte transfer

34408128 CQ_DMA_G_DMA_2_LEN2 General DMA Transfer Length 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	LEN2	**General DMA transfer length** Can be any byte alignment. This number will decrease when data are fetched from the source side. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

3440812C CQ_DMA_G_DMA_2_JUMP_ADDR General DMA Jump Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JUMP_ADDR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JUMP_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** Can be any byte alignment. Only valid when wrap_en = 1.

34408130 **CQ_DMA_G_DMA_2_INT_BUF_SIZE** **General DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	**General DMA size of data in internal buffer**

34408134 **CQ_DMA_G_DMA_2_CONNECT** **General DMA Connect Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	RATIO	**General DMA request/ack connection ratio** 0: 1/2 1: 1/1
2	DIR	**General DMA request/ack connection direction** 0: req/ack connected to write side 1: req/ack connected to read side
1:0	CONNECT	**General DMA request/ack connection** 1, 2 and 3 are only valid when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1. 0: No connection 1: Connect set1 (req/ack) 2: Connect set2 (req/ack) 3: Connect set3 (req/ack)

34408138 CQ_DMA_G_DMA_2_AXIATTR General DMA AXI Attribute Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	**General DMA AXI AWUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set up this bit when the destination is SYSRAM.
19:16	WCACHE	**General DMA AXI AWCACHE signal**
4	RUSER	**General DMA AXI ARUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set up this bit when the source is SYSRAM.
3:0	RCACHE	**General DMA AXI ARCACHE signal**

3440813C CQ_DMA_G_DMA_2_SEC_EN General DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DOMAIN_EN		PDOMAIN_CFG			DOMAIN_CFG				SEC_EN
Type							RW		RW			RW				RW
Reset							0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	DOMAIN_EN	**Sets up apb domain value check enable**
7:5	PDOMAIN_CFG	**Sets up apb domain value**
4:1	DOMAIN_CFG	**Sets up axi domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

34408140 CQ_DMA_G_DMA_2_APB_LATADDR General DMA Security Latch Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	**When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.**

34408144 CQ_DMA_G_DMA_2_ABORT General DMA Security Abort Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VID	W_VID				APB_ABORT								
Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID, and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	**Indicate that APB Read violation happens**
28	W_VID	**Indicate that APB Write violation happens**

Bit(s)	Name	Description
24	APB_ABORT	**When APB read/write violation happens, this bit will be 1'b1**

34408148 CQ_DMA_G_DMA_2_DCM_EN General DMA HW DCM Enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	DCM_EN	**Sets up GDMA HW DCM enable** If dcm_en = 0, DMA will not auto gate the clock when DMA is idle.

34408150 CQ_DMA_G_DMA_2_DEBUG General DMA Debug 00000013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				1	0	0	1	1

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

34408160 **CQ_DMA_G_DMA_2_SRC_ADDR2** **General DMA Source Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SRC_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SRC_ADDR2	**General DMA source address bit[32]**

34408164 **CQ_DMA_G_DMA_2_DST_ADDR2** **General DMA Destination Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DST_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DST_ADDR2	**General DMA destination address [32]**

34408168 **CQ_DMA_G_DMA_2_JUMP_ADDR2** **General DMA Jump Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													JUMP_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	JUMP_ADDR2	**General DMA jump address [32]**

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