MT793X IoT SDK for AUXADC User Guide

Version: 0.1

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Version History

Version	Date	Description
0.1	2021-07-29	Initial draft
0.2	2022-08-08	Add auxadc api

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1 Overview

1.1 Hardware Features

- Input channel number: 12 channels
- Sampling and output data rate: 2MS/s
- Input signal range: 0V-VREF18 voltage level
- SNR ≥ 60dB @ full input swing
- Latency time: 2 clocks

The IOs of auxiliary ADC (Analog-to-Digital Converter) can be set as either analog IO for ADC function or digital IO for GPIO function:

- Analog MODE: Used for ADC application; input voltage range is 0V~VREF18.
- Digital MODE: Used for GPIO application; input voltage is 3.3V.

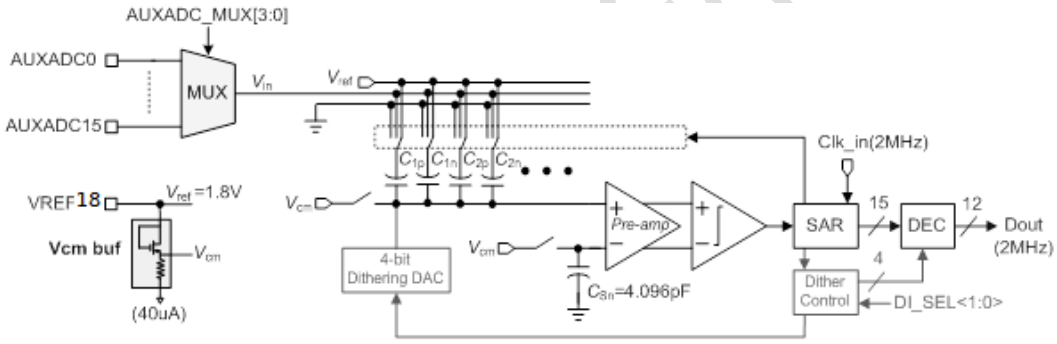

Figure 1-1. Auxiliary ADC Analog IP Block Diagram

Keywords of the figure: AUXADC_MUX, AUXADC0, Dithering DAC, Dither Control, DI_DEL, SAR, DEC, Dout

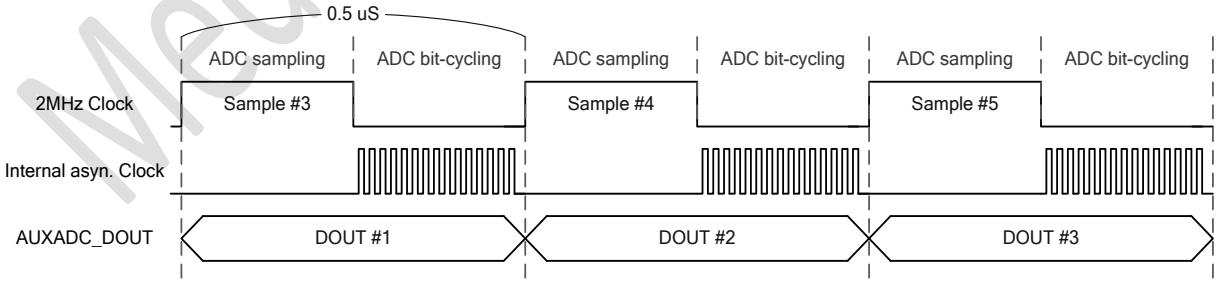

Figure 1-2. Auxiliary ADC Clock Timing Diagram

Keywords of the figure: ADC sampling, ADC bit-cycling, DOUT

Table 1-1. Auxiliary ADC Specification

Symbol	Parameter	Min	Typical	Max	Unit	Comment

N	Resolution		12		Bit	
CH	Channel Number		16		Channel	
FC	Clock Rate		2		MHz	
FS	Sampling Rate @ N-Bit(1)		2		MSPS	FS=2MHz
TS	Sample period		0.5		µS	=1/FS
VPP	Input Swing			VREF18	V	Dithering ON: Max=0.98*VREF18
VIN	Input voltage	0		VREF18	V	Dithering ON: Max=0.98*VREF18
SC	Sampling capacitance		4		pF	
RIN	Series Input Impedance: Unselected channel Selected channel	400M	10K		Ohm	
	Dither waveform type		Sawtooth			
	RMS noise added at input(2)	0.2	0.3	0.4	LSB	
	Dither step size (programmable)	0	4	4	LSB	Programmable (0,4)
N_{avg}	Number of samples averaged in hardware (programmable)	1	32	64		Programmable (1,2,4, 8,16, 32,64)
T_{dither}	Dither period	1	16	16	TS	Programmable(1,2,4,8,16)
	Dither Magnitude	0	64	64	LSB	=DITHERSTEP*T_{dither}
DNL	Differential Nonlinearity without dithering and averaging		± 1	± 2	LSB	No dithering and no averaging
INL	Integral Nonlinearity without dithering and averaging		± 2	± 4	LSB	
$DNL_{dither+average}$	Differential Nonlinearity with dithering and averaging		± 0.5	± 1	LSB	With dithering and averaging
$INL_{dither+average}$	Integral Nonlinearity with dithering and averaging			± 2	LSB	
OE	Offset Error			± 10	mV	
FSE	Full Swing Error			± 50	mV	
SNR	Signal to Noise Ratio(3)	60	63	66	dB	
DVDD	Digital Power Supply	1.0	1.1	1.2	V	
VREF18	Reference voltage=1.8V	1.6	1.8	AVDD	V	For VREF18 < 2.15V, RG_AUXADC[31]=1 (default) For VREF18 > 2.15V, RG_AUXADC[31] =0
AVDD	Analog Power Supply	2.25	2.5	2.75	V	
IOVDD	IO Power Supply	2.25	2.5	2.75	V	
T	Operating Temperature	0		60	℃	
Slide 13	Current Consumption			400	µA	
	Power-Down Current			1	µA	

Note 1: Given that FS=2MHz Note 2: Programmable by changing comparator tail current Note 3: At 1 kHz Input Frequency

1.2 Register Definition

- GPIO mode control register.
- GPIO direction control register.
- GPIO pull-up/pull-down control register.
- GPIO data output register.
- GPIO data input register.
- GPIO IES Control register.
- GPIO DRV Control register.

2 Driver Introduction

2.1 Driver Architecture

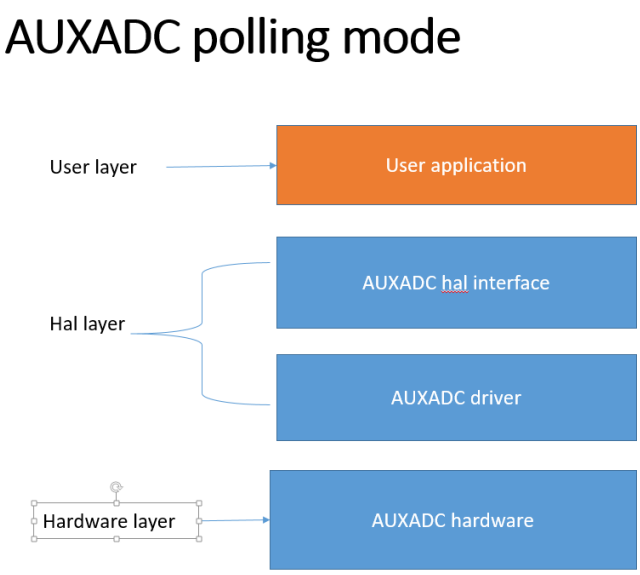

Figure 2-1. AUXADC Polling Mode

2.2 Driver API Reference

API	Introduction
hal_adc_get_data_polling()	AUXADC receives sample data for a channel.
Hal_adc_init()	Change axuadc pin from digital mode to auxadc analog mode and enable auxadc clk
Hal_adc_deinit()	Disable auxadc clk and change axuadc pin from analog mode to auxadc digital mode

2.3 Sample Code

```
    for (channel = 0; channel < HAL_ADC_CHANNEL_MAX; channel++) {
        ret = hal_adc_get_data_polling(channel, &val);
        if (ret < 0)
            printf("hal_adc_get_data_polling fail.\r\n");
        voltage = val * 1800 / 4096;
        printf("hal_adc_get_data_polling pass. channel(%d), val(0x%lx),
voltage(%ld mv)\r\n", channel, val, voltage);
    }
```

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