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Lab 5

ENGN 1640
April 2, 2019

Contents

1 Part 1

Include the assembly and machine code of the factorial program and your program of choice in the documentation.

Note: This code is located in instruction_mem.v and all commented out except the factorial program.

1.1 Program 1:

```
addi x1, x0, 0
addi x2, x0, 16
addi x3, x0, 100
addi x4, x0, 8
add x5, x1, x2
add x6, x3, x4
sw x5, 0(x1)
sw x6, 4(x2)
```

```
rom_fact[0] = 32'b00000000000000000000000010010011; //8'h00000093;      //addi x1 x0 0
rom_fact[1] = 32'b00000001000000000000000100010011; //8'h01000113;      //addi x2 x0 16
rom_fact[2] = 32'b00000110010000000000000110010011; //8'h06400193;      //addi x3 x0 100
rom_fact[3] = 32'b00000000100000000000001000010011; //8'h00800213;      //addi x4 x0 8
rom_fact[4] = 32'b00000000001000001000001010110011; //8'h002082b3;      //add x5 x1 x2
rom_fact[5] = 32'b00000000010000011000001100110011; //8'h00418333;      //add x6 x3 x4
rom_fact[6] = 32'b00000000010100001010000000100011; //8'h0050a023;      //sw x5 0(x1)
rom_fact[7] = 32'b00000000011000010010001000100011; //8'h00612223;  //sw x6 4(x2)
rom_fact[8] = 32'b00000000000000000000000001111111; //8'b11111111;  //halt
```

1.2 Program 2:

```
addi t0, x0, 8
addi t1, x0, 15
sw t1, 0(t0)
add t2, t1, t0
sub t3, t1, t0
mul s1, t2, t3
addi t0, t0, 4
lw s2, -4(t0)
sub s2, s1, s2
slli s2, s2, 2
sw s2, 0(t0)
```

```
rom_fact[0] = 32'b00000000100000000000001010010011; //0x00800293       addi x5 x0 8
rom_fact[1] = 32'b00000000111100000000001100010011; //0x00f00313       addi x6 x0 15
rom_fact[2] = 32'b00000000011000101010000000100011; //0x0062a023       sw x6 0(x5)
rom_fact[3] = 32'b00000000010100110000001110110011; //0x005303b3       add x7 x6 x5
rom_fact[4] = 32'b01000000010100110000111000110011; //0x40530e33       sub x28 x6 x5
rom_fact[5] = 32'b00000011110000111000010010110011; //0x03c384b3       mul x9 x7 x28
rom_fact[6] = 32'b00000000010000101000001010010011; //0x00428293       addi x5 x5 4
rom_fact[7] = 32'b11111111110000101010100100000011; //0xffc2a903       lw x18 -4(x5)
rom_fact[8] = 32'b01000001001001001000100100110011; //0x41248933       sub x18 x9 x18
rom_fact[9]= 32'b00000000001010010001100100010011; //0x00291913 slli x18 x18 2
rom_fact[10]= 32'b00000001001000101010000000100011; //0x0122a023       sw x18 0(x5)
rom_fact[11]= 32'b00000000000000000000000001111111; //8'b11111111;  //halt
```

1.3 factorial:

```
addi a0, x0, 6
jal ra, fact
sw a0, 0(x0)
done

fact:
addi sp, sp, -8
sw  ra, 4(sp)
sw  a0, 0(sp)
addi a0, a0, -1
bne a0, x0, else
addi a0, x0, 1
addi sp, sp, 8
```

```
jalr x0, 0(ra)
else:
jal ra, fact
addi t0, a0,0
lw  a0, 0(sp)
lw  ra, 4(sp)
addi sp, sp, 8
mul a0, a0, t0
jalr x0, 0(ra)
```

Verilog Code for Fact:

```
rom_fact[0] = 32'b00000000011000000000010100010011; //0x00600513         addi x10 x0 6    addi a0, x0, 6

//rom_fact[0] = 32'b00000000001100000000010100010011; //0x00300513       addi x10 x0 3    addi a0, x0, 3

rom_fact[1] = 32'b00000000110000000000000011101111; //0x008000ef         jal x1 12        jal ra, fact

rom_fact[2] = 32'b00000000101000000010000000100011; //0x00a02023         sw x10 0(x0)     sw a0, 0(x0)

rom_fact[3] = 32'b00000000000000000000000011111111; //8'b11111111;   //halt

rom_fact[4] = 32'b11111111100000010000000100010011; //0xff810113         addi x2 x2 -8    addi sp, sp, -8

rom_fact[5] = 32'b00000000000100010010001000100011; //0x00112223         sw x1 4(x2)      sw ra, 4(sp)

rom_fact[6] = 32'b00000000101000010010000000100011; //0x00a12023         sw x10 0(x2)     sw a0, 0(sp)

rom_fact[7] = 32'b11111111111101010000010100010011; //0xfff50513         addi x10 x10 -1  addi a0, a0, -1

rom_fact[8] = 32'b00000000000001010001100001100011; //0x00051863         bne x10 x0 16    bne a0, x0, else

rom_fact[9] = 32'b00000000000100000000010100010011; //0x00100513         addi x10 x0 1    addi a0, x0, 1

rom_fact[10]= 32'b00000000100000010000000100010011; //0x00810113         addi x2 x2 8     addi sp, sp, 8

rom_fact[11] = 32'b00000000000000001000000001100111; //0x00008067        jalr x0 x1 0     jalr x0, 0(ra)

rom_fact[12] = 32'b11111110000111111111000011101111; //0xfe1ff0ef        jal x1 -32       jal ra, fact

rom_fact[13] = 32'b00000000000001010000001010010011; //0x00050293        addi x5 x10 0    addi t0, a0,0

rom_fact[14] = 32'b00000000000000010010010100000011; //0x00012503        lw x10 0(x2)     lw a0, 0(sp)

rom_fact[15] = 32'b00000000010000010010000010000011; //0x00412083        lw x1 4(x2)      lw ra, 4(sp)

rom_fact[16] = 32'b00000000100000010000000100010011; //0x00810113        addi x2 x2 8     addi sp, sp, 8

rom_fact[17] = 32'b00000010010101010000010100110011; //0x02550533        mul x10 x10 x5   mul a0, a0, t0

rom_fact[18] = 32'b00000000000000001000000001100111; //0x00008067        jalr x0 x1 0     jalr x0, 0(ra)
```

1.4 Fib

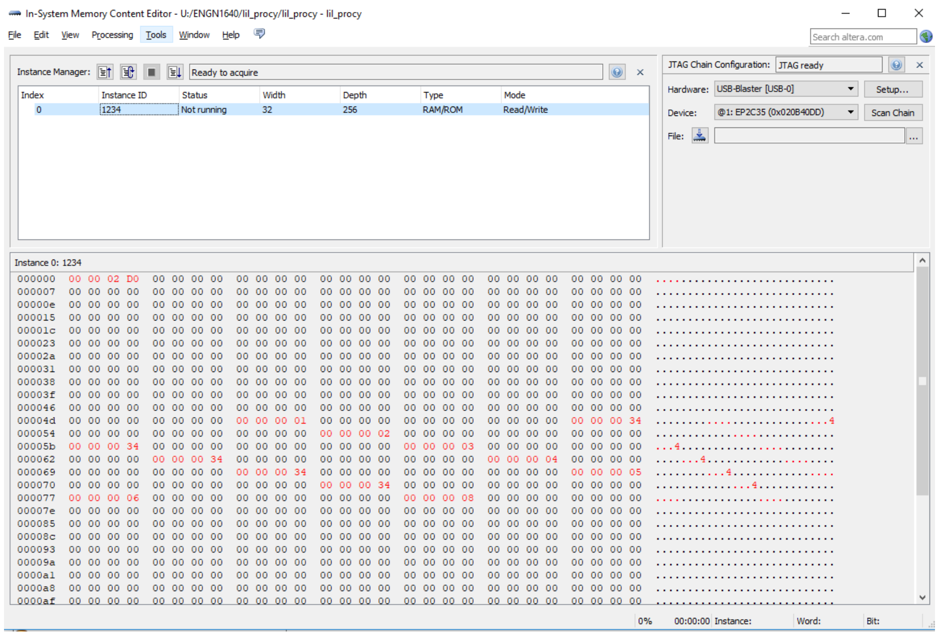
```
addi t2 t2 3 # comparison
addi a0, x0, 6 # load value
jal ra, fib
halt

fib:
addi sp, sp, -8
sw ra, 4(sp)
sw a0, 0(sp)
bge a0 t2 else
addi a1, x0, 1 # if n <= 2
addi sp, sp, 8
jalr x0, 0(ra)
else: # if n >= 2
addi a0 a0 -1 # calc n - 1
jal ra, fib # loose ra with call
addi sp, sp, -4 # save f(n-1) on stack
sw a1, 0(sp)
addi a0 a0 -1 # calc n - 2
jal ra, fib # loose ra with call
addi t1, a1,0 # save f(n - 2)
lw t0, 0(sp) # pop f(n-1)
addi sp, sp, 4
lw a0, 0(sp) # restore n
lw ra, 4(sp)
addi sp, sp, 8
add a1, t1, t0 #f(n-2) + f(n-1)
```

```
jalr x0, 0(ra)

rom_fact[0] = 32'b00000000001100111000001110010011; //0x00338393         addi t2 t2 3 # comparison

rom_fact[1] = 32'b00000000011000000000010100010011; //0x00600513addi a0, x0, 6 # load value


rom_fact[2] = 32'b00000000110000000000000011101111; //0x00c000ef         jal ra, fib

rom_fact[3] = 32'b00000000101100000010000000100011; //0x00b02023         sw a1 0(x0)

rom_fact[4] = 32'b00000000000000000000000011111111; //8'b11111111;  //halt

rom_fact[5] = 32'b11111111100000010000000100010011; //0xff810113         addi sp, sp, -8

rom_fact[6] = 32'b00000000000100010010001000100011; //0x00112223 sw ra, 4(sp)

rom_fact[7] = 32'b00000000101000010010000000100011; //0x00a12023         sw a0, 0(sp)

rom_fact[8] = 32'b00000000011101010101100001100011; //0x00755863         bge a0 t2 else

rom_fact[9] = 32'b00000000000100000000010110010011; //0x00100593         addi a1, x0, 1
# if n <= 2

rom_fact[10] = 32'b00000000100000010000000100010011; //0x00810113        addi sp, sp, 8

rom_fact[11]= 32'b00000000000000001000000001100111; //0x00008067         jalr x0, 0(ra)

rom_fact[12] = 32'b11111111111101010000010100010011; //0xfff50513        addi a0 a0 -1
# calc n - 1

rom_fact[13] = 32'b11111110000111111111000011101111; //0xfe1ff0ef        jal ra, fib
# loose ra with call

rom_fact[14] = 32'b11111111110000010000000100010011; //0xffc10113        addi sp, sp, -4
# save f(n-1) on stack

rom_fact[15] = 32'b00000000101100010010000000100011; //0x00b12023        sw a1, 0(sp)

rom_fact[16] = 32'b11111111111101010000010100010011; //0xfff50513        addi a0 a0 -1
# calc n - 2

rom_fact[17] = 32'b11111101000111111111000011101111; //0xfd1ff0ef        jal ra, fib
# loose ra with call

rom_fact[18] = 32'b00000000000001011000001100010011; //0x00058313        addi t1, a1,0
# save f(n - 2)

rom_fact[19] = 32'b00000000000000010010001010000011; //0x00012283        lw t0, 0(sp)
# pop f(n-1)

rom_fact[20] = 32'b00000000010000010000000100010011; //0x00410113        addi sp, sp, 4

rom_fact[21] = 32'b00000000000000010010010100000011; //0x00012503        lw a0, 0(sp)
# restore n

rom_fact[22] = 32'b00000000010000010010000010000011; //0x00412083        lw ra, 4(sp)

rom_fact[23] = 32'b00000000100000010000000100010011; //0x00810113        addi sp, sp, 8

rom_fact[24] = 32'b00000000010100110000010110110011; //0x005305b3        add a1, t1, t0
#f(n-2) + f(n-1)

rom_fact[25] = 32'b00000000000000001000000001100111; //0x00008067        jalr x0, 0(ra)
```

2 Part 2

Print screenshots that shows the memory contents after executing the factorial program and your program of choice.

Factorial Program:


In-System Memory Content Editor - U:/ENGN1640/lil_procy/lil_procy - lil_procy
File Edit View Processing Tools Window Help
Search altera.com
Setup...
Scan Chain

Instance Manager: Ready to acquire

Index	Instance ID	Status	Width	Depth	Type	Mode
0	1234	Not running	32	256	RAM/ROM	Read/Write

JTAG Chain Configuration: JTAG ready
Hardware: USB-Blaster [USB-0]
Device: @1: EP2C35 (0x020B40DD)
File:

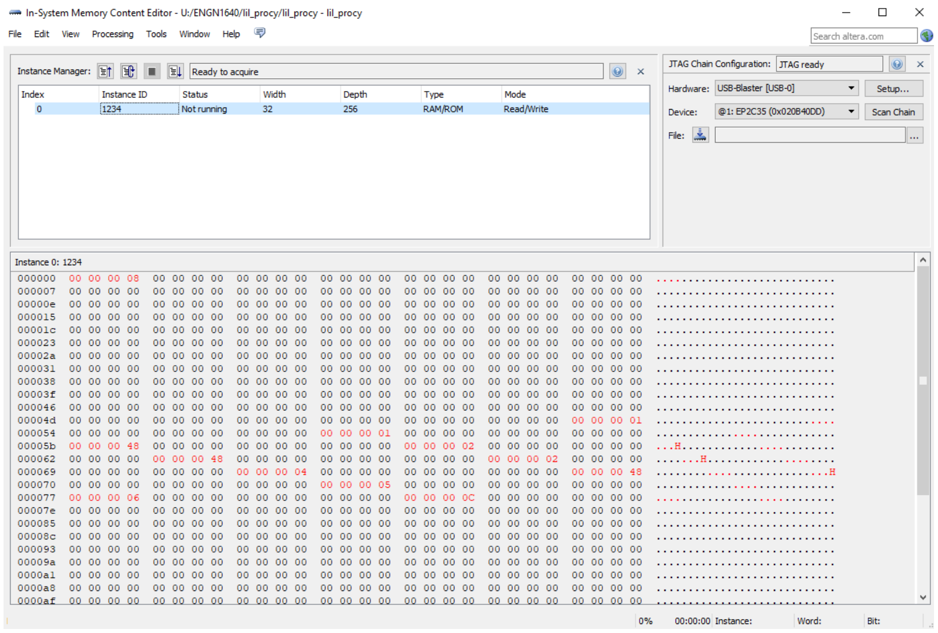
Instance 0: 1234

```
000000  00 00 02 D0  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000007  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00000e  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000015  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00001c  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000023  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00002a  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000031  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000038  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00003f  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000046  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00004d  00 00 00 00  00 00 00 00  00 00 00 01  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 34  ...........................4
000054  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 02  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00005b  00 00 00 34  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 03  00 00 00 00  00 00 00 00  ...4........................
000062  00 00 00 00  00 00 00 34  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 04  00 00 00 00  .......4....................
000069  00 00 00 00  00 00 00 00  00 00 00 34  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 05  ...........4................
000070  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 34  00 00 00 00  00 00 00 00  00 00 00 00  ...............4............
000077  00 00 00 06  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 08  00 00 00 00  00 00 00 00  ............................
00007e  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000085  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00008c  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000093  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00009a  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000a1  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000a8  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000af  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
```

0% 00:00:00 Instance: Word: Bit:

The result is stored in x0 and evaluated to 02 D0. The bottom of the memory content is stuff written to the stack during execution.

Fib Program:


In-System Memory Content Editor - U:/ENGN1640/lil_procy/lil_procy - lil_procy
File Edit View Processing Tools Window Help
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Scan Chain

Instance Manager: Ready to acquire

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JTAG Chain Configuration: JTAG ready
Hardware: USB-Blaster [USB-0]
Device: @1: EP2C35 (0x020B40DD)
File:

Instance 0: 1234

```
000000  00 00 00 08  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000007  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00000e  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000015  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00001c  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000023  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00002a  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000031  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000038  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00003f  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000046  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00004d  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 01  ............................
000054  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 01  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00005b  00 00 00 48  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 02  00 00 00 00  00 00 00 00  ...H........................
000062  00 00 00 00  00 00 00 48  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 02  00 00 00 00  .......H....................
000069  00 00 00 00  00 00 00 00  00 00 00 04  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 48  ...........................H
000070  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 05  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000077  00 00 00 06  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 0C  00 00 00 00  00 00 00 00  ............................
00007e  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000085  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00008c  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
000093  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
00009a  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000a1  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000a8  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
0000af  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ............................
```

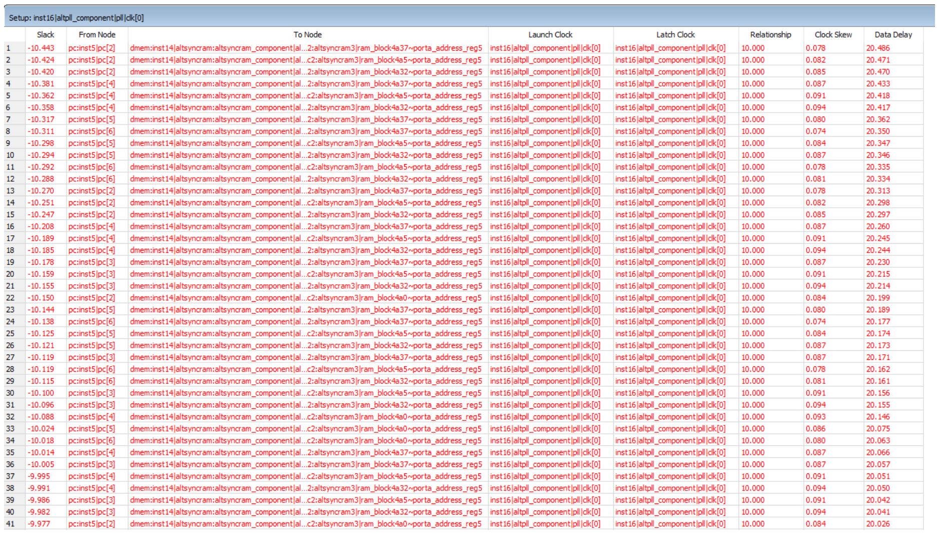
0% 00:00:00 Instance: Word: Bit:

The result is stored in x0 and evaluated to 8. The bottom of the memory content is stuff written to the stack during execution.

3 Part 3

Use the TimingQuest tool to analyze the timing in your design. Report the critical path delay in your design and predicted Fmax. Use the tool to (1) locate the critical path in your floorplan and print the annotated critical in the floorplan view, and (2) estimate the delay breakdown among the different stages of execution (e.g., fetch, decode, execution, memory and write back). Please read the tutorial on TimingQuest analysis tool to understand the operation of this tool. A tutorial is distributed in class and also available on the class web page.

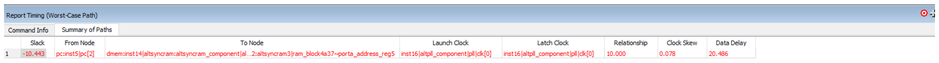
Overview of Critical path:



Setup: inst16\|altpll_component\|pll\|clk[0]

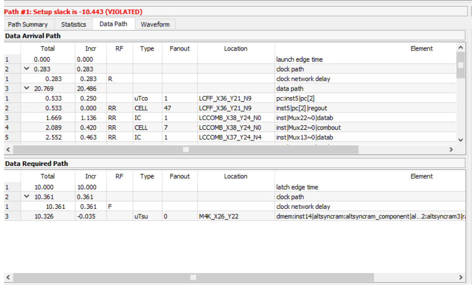
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-10.443	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.078	20.486
2	-10.424	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.082	20.471
3	-10.420	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.085	20.470
4	-10.381	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.433
5	-10.362	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.418
6	-10.358	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.417
7	-10.317	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.080	20.362
8	-10.311	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.074	20.350
9	-10.298	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.084	20.347
10	-10.294	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.346
11	-10.292	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.078	20.335
12	-10.288	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.081	20.334
13	-10.270	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.078	20.313
14	-10.251	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.082	20.298
15	-10.247	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.085	20.297
16	-10.208	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.260
17	-10.189	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.245
18	-10.185	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.244
19	-10.178	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.230
20	-10.159	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.215
21	-10.155	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.214
22	-10.150	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a0~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.084	20.199
23	-10.144	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.080	20.189
24	-10.138	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.074	20.177
25	-10.125	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.084	20.174
26	-10.121	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.173
27	-10.119	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.171
28	-10.119	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.078	20.162
29	-10.115	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.081	20.161
30	-10.100	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.156
31	-10.096	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.155
32	-10.088	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a0~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.093	20.146
33	-10.024	pc:inst5|pc[5]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a0~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.086	20.075
34	-10.018	pc:inst5|pc[6]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a0~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.080	20.063
35	-10.014	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.066
36	-10.005	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.087	20.057
37	-9.995	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.051
38	-9.991	pc:inst5|pc[4]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.050
39	-9.986	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a5~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.091	20.042
40	-9.982	pc:inst5|pc[3]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a32~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.094	20.041
41	-9.977	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...c2:altsyncram3|ram_block4a0~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.084	20.026

Here are a list of worst paths.



Report Timing (Worst-Case Path)

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-10.443	pc:inst5|pc[2]	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|ram_block4a37~porta_address_reg5	inst16|altpll_component|pll|clk[0]	inst16|altpll_component|pll|clk[0]	10.000	0.078	20.486



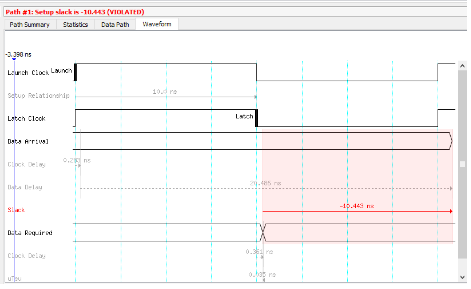
Path #1: Setup slack is -10.443 (VIOLATED)

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.283	0.283					clock path
1	0.283	0.283	R				clock network delay
3	20.769	20.486					data path
1	0.533	0.250		uTco	1	LCFF_X36_Y21_N9	pc:inst5|pc[2]
2	0.533	0.000	RR	CELL	47	LCFF_X36_Y21_N9	inst5|pc[2]|regout
3	1.669	1.136	RR	IC	1	LCCOMB_X38_Y24_N0	inst|Mux22~0|datab
4	2.089	0.420	RR	CELL	7	LCCOMB_X38_Y24_N0	inst|Mux22~0|combout
5	2.552	0.463	RR	IC	1	LCCOMB_X37_Y24_N4	inst|Mux13~0|datab

Data Required Path

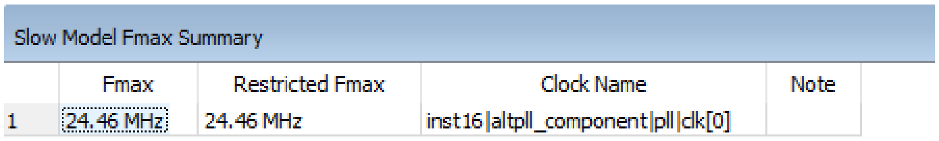
	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	10.361	0.361					clock path
1	10.361	0.361	F				clock network delay
3	10.326	-0.035		uTsu	0	M4K_X26_Y22	dmem:inst14|altsyncram:altsyncram_component|al...2:altsyncram3|r



Path #1: Setup slack is -10.443 (VIOLATED)

The worst path was from the pc counter to the ram (see floor plan below). This path had an arrival time of 21.338ns and a required time of 10.330ns. The slack was -11.008ns.

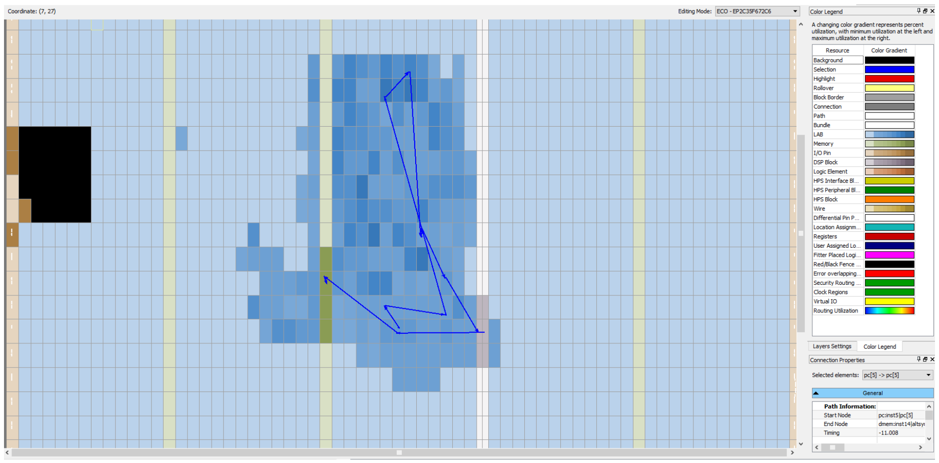
3.1 Delay:



Slow Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	24.46 MHz	24.46 MHz	inst16|altpll_component|pll|clk[0]	

The reported Fmax value is 24.46MHz.



A changing color gradient represents percent utilization, with minimum utilization at the left and maximum utilization at the right.

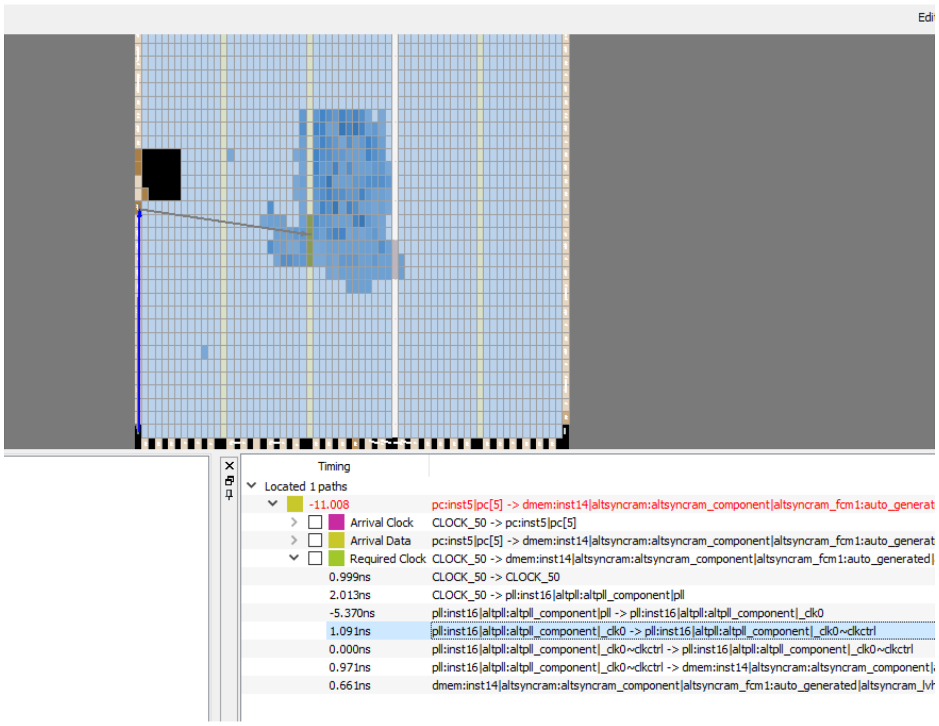
Resource	Color Gradient
Background	⬛
Selection	🟦
Highlight	🟥
Rollover	🟨
Block Border	▨
Connection	▨
Path	⬜
Bundle	⬜
LAB	🟦
Memory	🟩
I/O Pin	🟫
DSP Block	▨
Logic Element	🟫
HPS Interface Bl...	🟨
HPS Peripheral Bl...	🟩
HPS Block	🟧
Wire	🟫
Differential Pin P...	⬜
Location Assignm...	🟦
Registers	🟥
User Assigned Lo...	🟦
Fitter Placed Logi...	🟪
Red/Black Fence ...	⬛
Error overlapping...	🟥
Security Routing ...	🟩
Clock Regions	🟩
Virtual IO	🟨
Routing Utilization	▨

Selected elements: pc[5] -> pc[5]

Path Information:	
Start Node	pc:inst5|pc[5]
End Node	dmem:inst14|altsy
Timing	-11.008

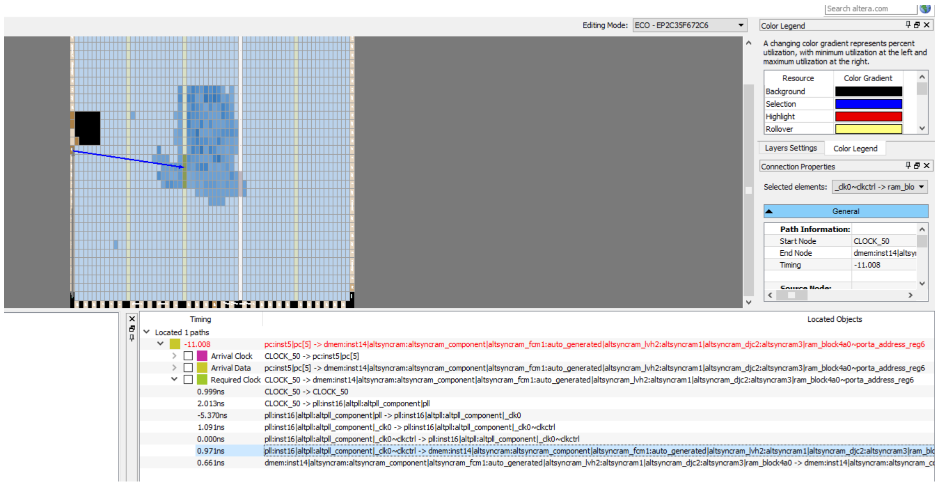
Overview of the worst case path on floorplan with no annotations.

3.2 Clock:



```
Timing
Located 1 paths
  -11.008          pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generat
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generat
    Required Clock CLOCK_50 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|
      0.999ns      CLOCK_50 -> CLOCK_50
      2.013ns      CLOCK_50 -> pll:inst16|altpll:altpll_component|pll
      -5.370ns     pll:inst16|altpll:altpll_component|pll -> pll:inst16|altpll:altpll_component|_clk0
      1.091ns      pll:inst16|altpll:altpll_component|_clk0 -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
      0.000ns      pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
      0.971ns      pll:inst16|altpll:altpll_component|_clk0~clkctrl -> dmem:inst14|altsyncram:altsyncram_component|
      0.661ns      dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh
```

This show the path from the 50Mhz clock to the PLL for the required clock



A changing color gradient represents percent utilization, with minimum utilization at the left and maximum utilization at the right.

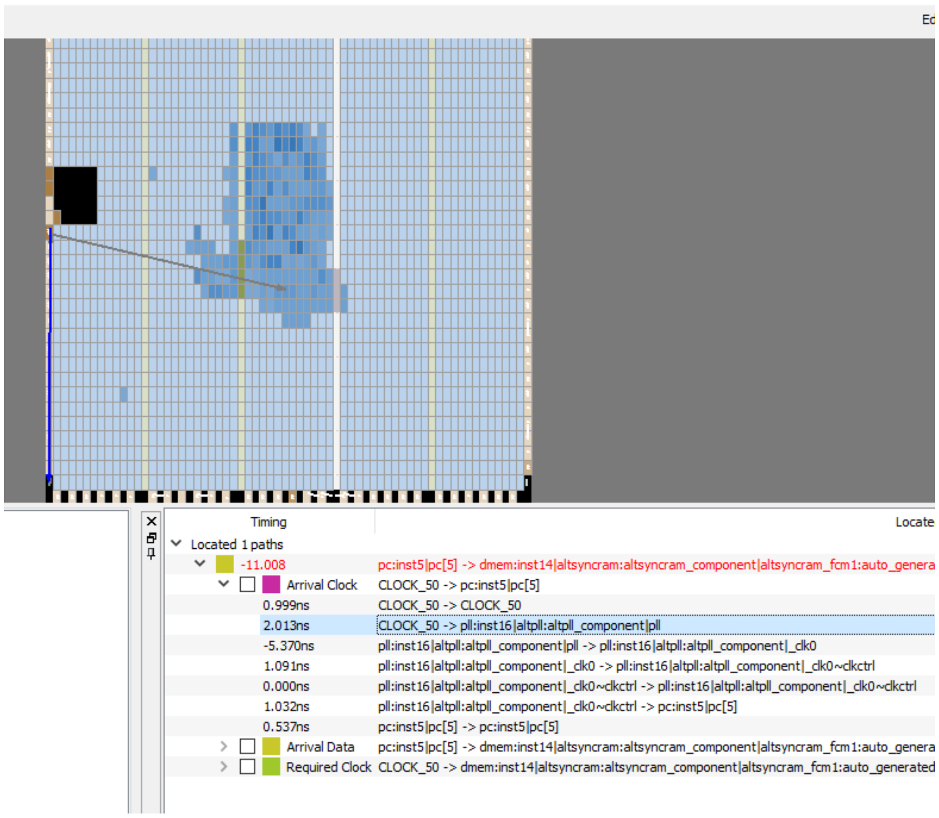
Resource	Color Gradient
Background	⬛
Selection	🟦
Highlight	🟥
Rollover	🟨

Selected elements: _clk0~clkctrl -> ram_blo

Path Information:	
Start Node	CLOCK_50
End Node	dmem:inst14|altsy
Timing	-11.008

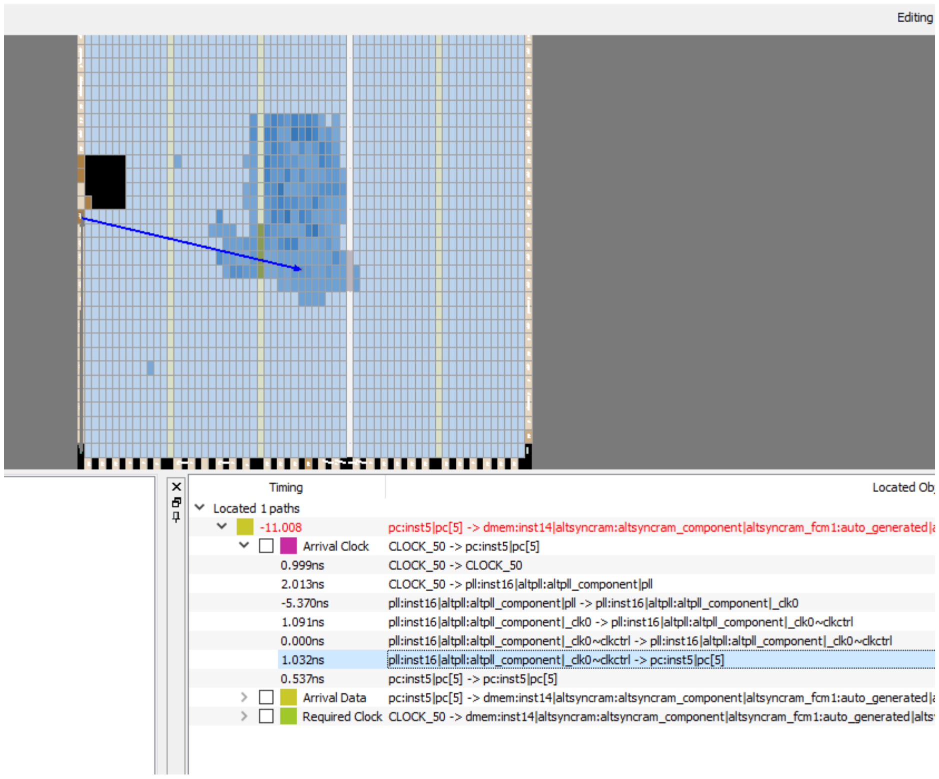
```
Timing                                                                    Located Objects
Located 1 paths
  -11.008          pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0~porta_address_reg6
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0~porta_address_reg6
    Required Clock CLOCK_50 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0~porta_address_reg6
      0.999ns      CLOCK_50 -> CLOCK_50
      2.013ns      CLOCK_50 -> pll:inst16|altpll:altpll_component|pll
      -5.370ns     pll:inst16|altpll:altpll_component|pll -> pll:inst16|altpll:altpll_component|_clk0
      1.091ns      pll:inst16|altpll:altpll_component|_clk0 -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
      0.000ns      pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
      0.971ns      pll:inst16|altpll:altpll_component|_clk0~clkctrl -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_blo
      0.661ns      dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0 -> dmem:inst14|altsyncram:altsyncram_c
```

This show the path from the clock to the RAM memory cell



Timing	Locate
Located 1 paths	
-11.008	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_genera
Arrival Clock	CLOCK_50 -> pc:inst5|pc[5]
0.999ns	CLOCK_50 -> CLOCK_50
2.013ns	CLOCK_50 -> pll:inst16|altpll:altpll_component|pll
-5.370ns	pll:inst16|altpll:altpll_component|pll -> pll:inst16|altpll:altpll_component|_clk0
1.091ns	pll:inst16|altpll:altpll_component|_clk0 -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
0.000ns	pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
1.032ns	pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pc:inst5|pc[5]
0.537ns	pc:inst5|pc[5] -> pc:inst5|pc[5]
Arrival Data	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_genera
Required Clock	CLOCK_50 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated

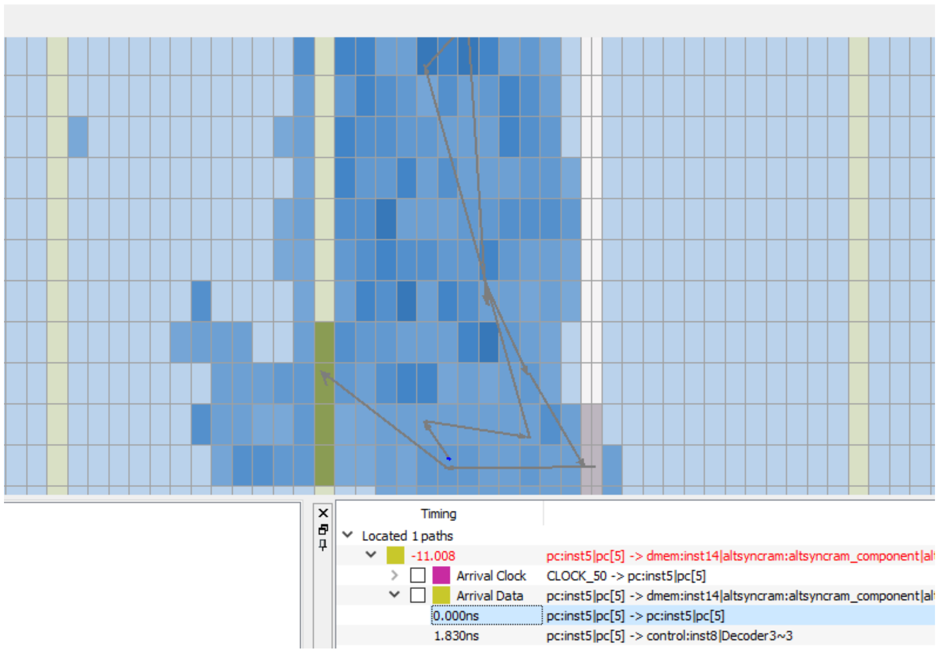
This show the path from the 50Mhz clock to the PLL for the arrival clock



Timing	
Located 1 paths	
-11.008	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|
Arrival Clock	CLOCK_50 -> pc:inst5|pc[5]
0.999ns	CLOCK_50 -> CLOCK_50
2.013ns	CLOCK_50 -> pll:inst16|altpll:altpll_component|pll
-5.370ns	pll:inst16|altpll:altpll_component|pll -> pll:inst16|altpll:altpll_component|_clk0
1.091ns	pll:inst16|altpll:altpll_component|_clk0 -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
0.000ns	pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pll:inst16|altpll:altpll_component|_clk0~clkctrl
1.032ns	pll:inst16|altpll:altpll_component|_clk0~clkctrl -> pc:inst5|pc[5]
0.537ns	pc:inst5|pc[5] -> pc:inst5|pc[5]
Arrival Data	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|
Required Clock	CLOCK_50 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|alts

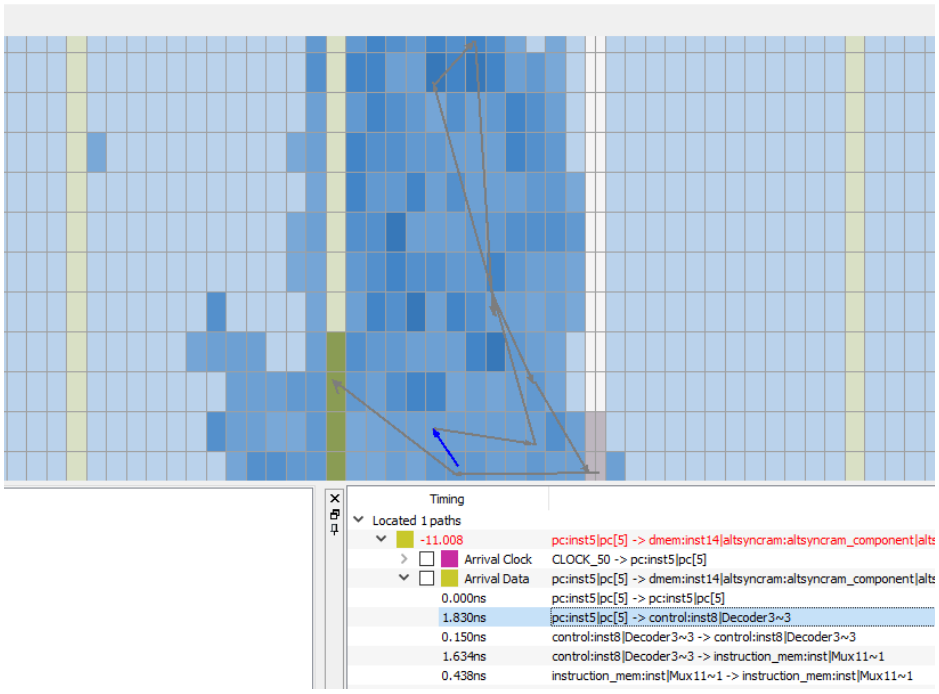
This shows the clock to the program counter cell

3.3 Fetch:



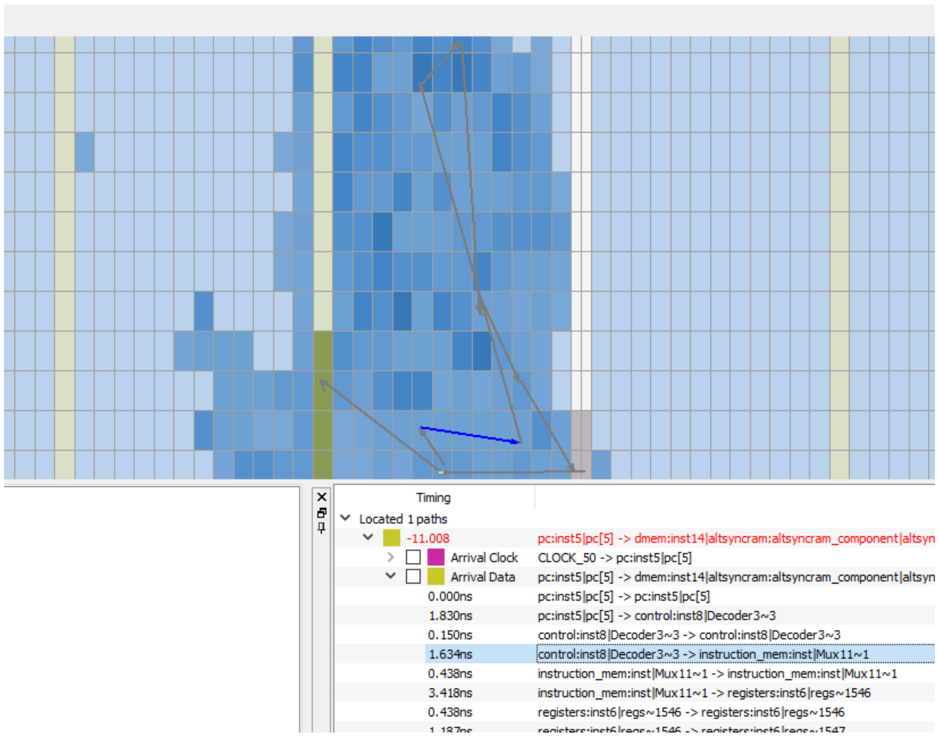
```
Timing
Located 1 paths
  -11.008          pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|al
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|al
      0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
```

Updating the PC (0.000ns)



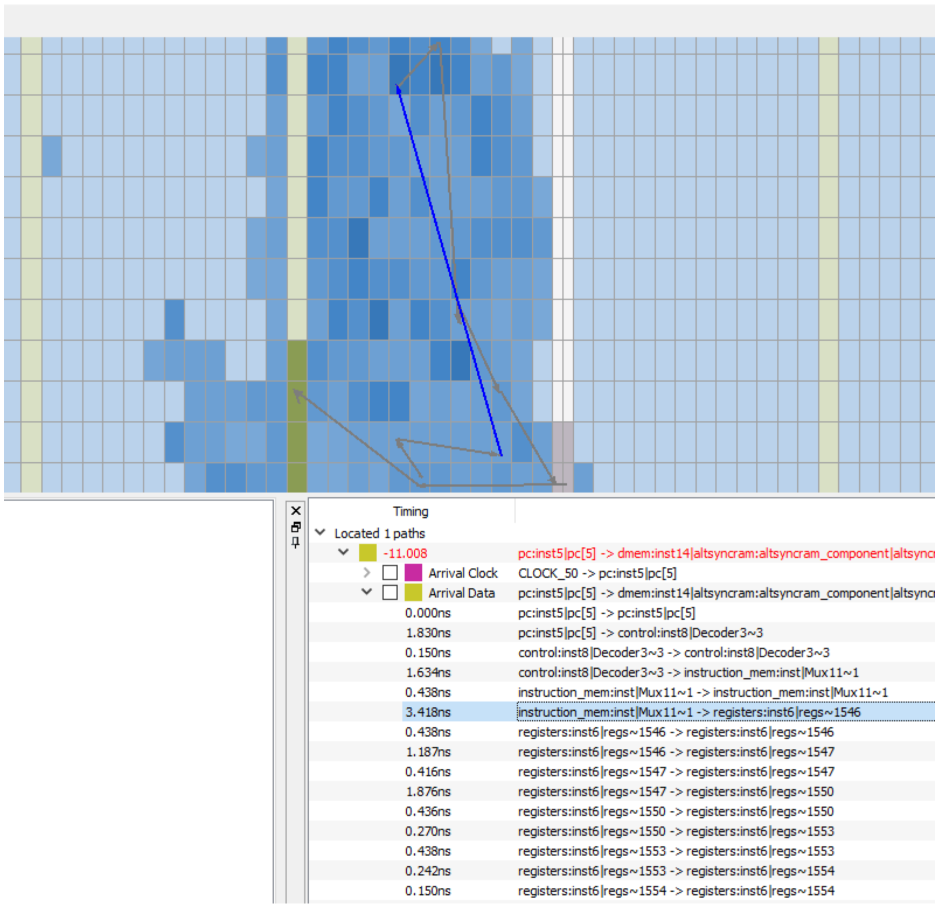
```
Timing
Located 1 paths
  -11.008          pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|alts
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|alts
      0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
```

PC to decoder (1.83ns)



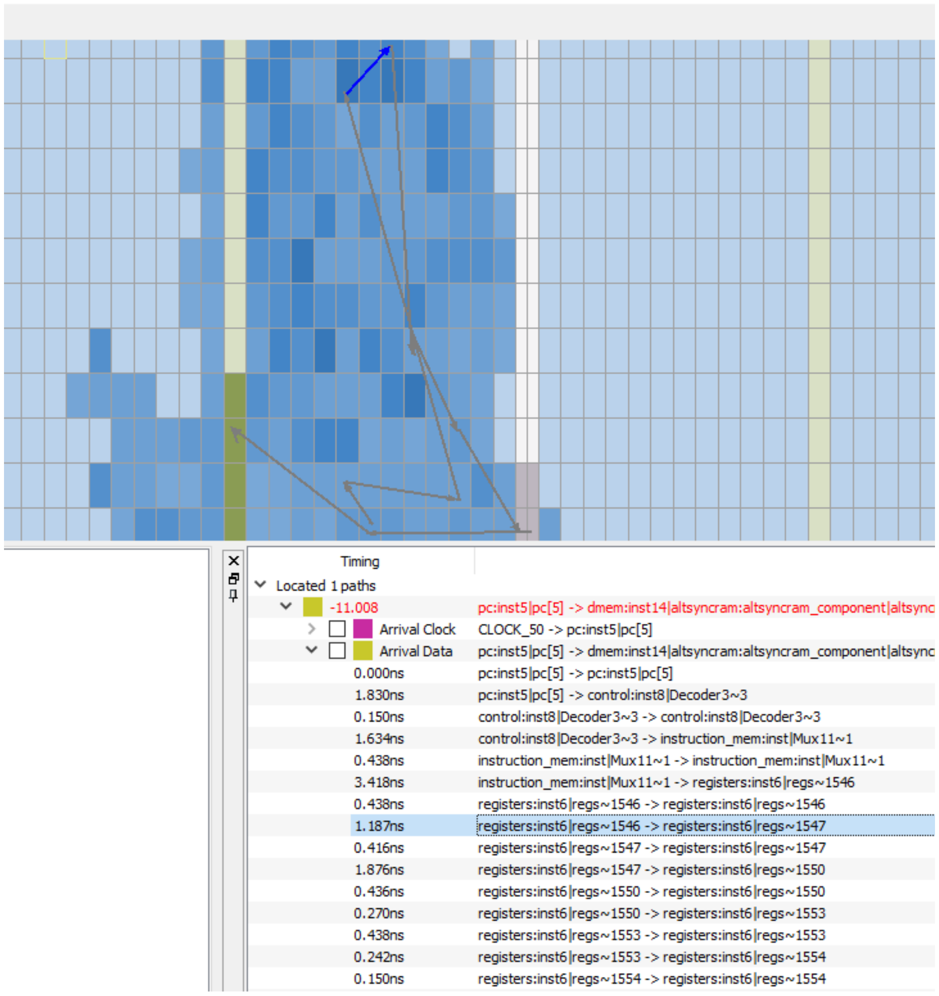
```
Timing
Located 1 paths
  -11.008        pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyn
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyn
      0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
      3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
      0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
      1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
```

Fetching instruction (1.634ns)



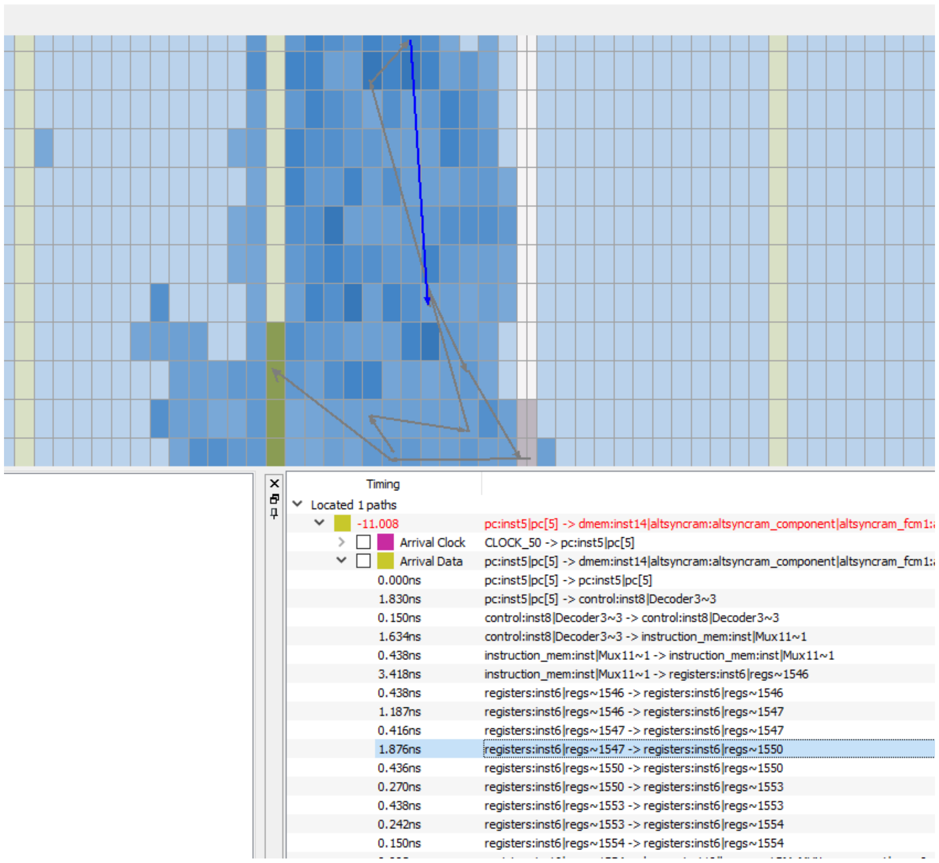
```
Timing
Located 1 paths
    -11.008      pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsync
      Arrival Clock   CLOCK_50 -> pc:inst5|pc[5]
      Arrival Data    pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsync
         0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
         1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
         0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
         1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
         0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
         3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
         0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
         1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
         0.416ns      registers:inst6|regs~1547 -> registers:inst6|regs~1547
         1.876ns      registers:inst6|regs~1547 -> registers:inst6|regs~1550
         0.436ns      registers:inst6|regs~1550 -> registers:inst6|regs~1550
         0.270ns      registers:inst6|regs~1550 -> registers:inst6|regs~1553
         0.438ns      registers:inst6|regs~1553 -> registers:inst6|regs~1553
         0.242ns      registers:inst6|regs~1553 -> registers:inst6|regs~1554
         0.150ns      registers:inst6|regs~1554 -> registers:inst6|regs~1554
```

Register to register (1.187ns)



```
Timing
Located 1 paths
  -11.008      pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsync
    Arrival Clock   CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data    pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsync
      0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
      3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
      0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
      1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
      0.416ns      registers:inst6|regs~1547 -> registers:inst6|regs~1547
      1.876ns      registers:inst6|regs~1547 -> registers:inst6|regs~1550
      0.436ns      registers:inst6|regs~1550 -> registers:inst6|regs~1550
      0.270ns      registers:inst6|regs~1550 -> registers:inst6|regs~1553
      0.438ns      registers:inst6|regs~1553 -> registers:inst6|regs~1553
      0.242ns      registers:inst6|regs~1553 -> registers:inst6|regs~1554
      0.150ns      registers:inst6|regs~1554 -> registers:inst6|regs~1554
```

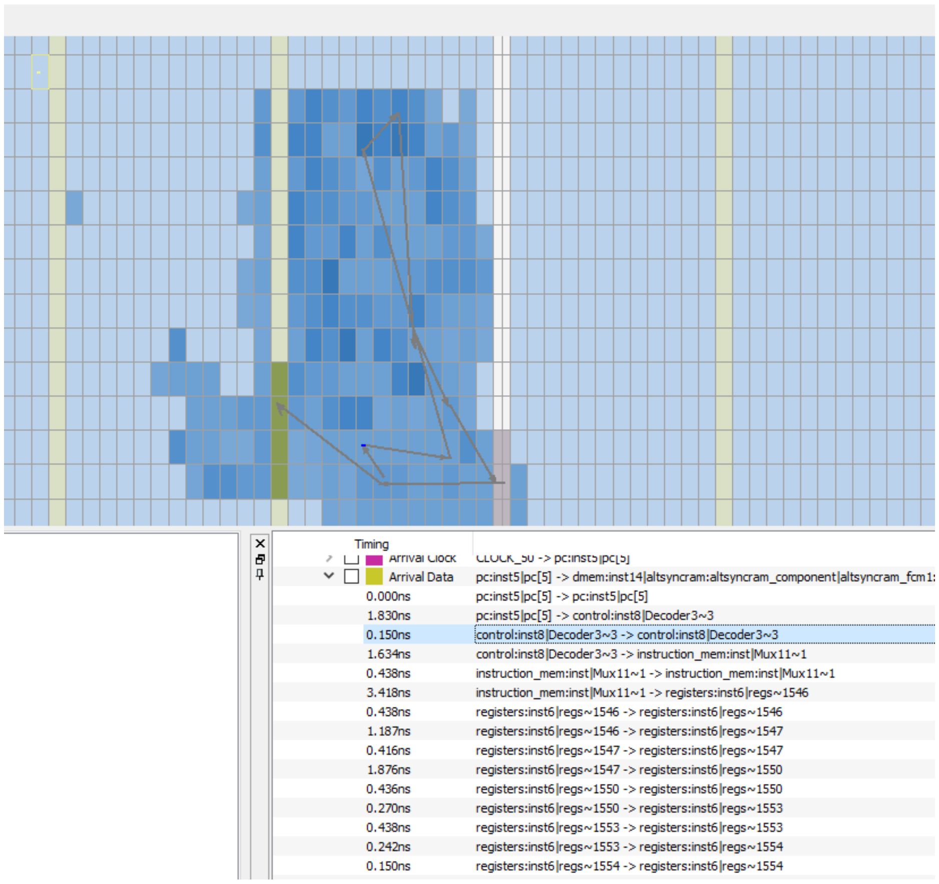
Register to register (1.876ns)



```
Timing
Located 1 paths
  -11.008   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:
    Arrival Clock   CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data    pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:
      0.000ns   pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns   pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns   control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns   control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns   instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
      3.418ns   instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
      0.438ns   registers:inst6|regs~1546 -> registers:inst6|regs~1546
      1.187ns   registers:inst6|regs~1546 -> registers:inst6|regs~1547
      0.416ns   registers:inst6|regs~1547 -> registers:inst6|regs~1547
      1.876ns   registers:inst6|regs~1547 -> registers:inst6|regs~1550
      0.436ns   registers:inst6|regs~1550 -> registers:inst6|regs~1550
      0.270ns   registers:inst6|regs~1550 -> registers:inst6|regs~1553
      0.438ns   registers:inst6|regs~1553 -> registers:inst6|regs~1553
      0.242ns   registers:inst6|regs~1553 -> registers:inst6|regs~1554
      0.150ns   registers:inst6|regs~1554 -> registers:inst6|regs~1554
```

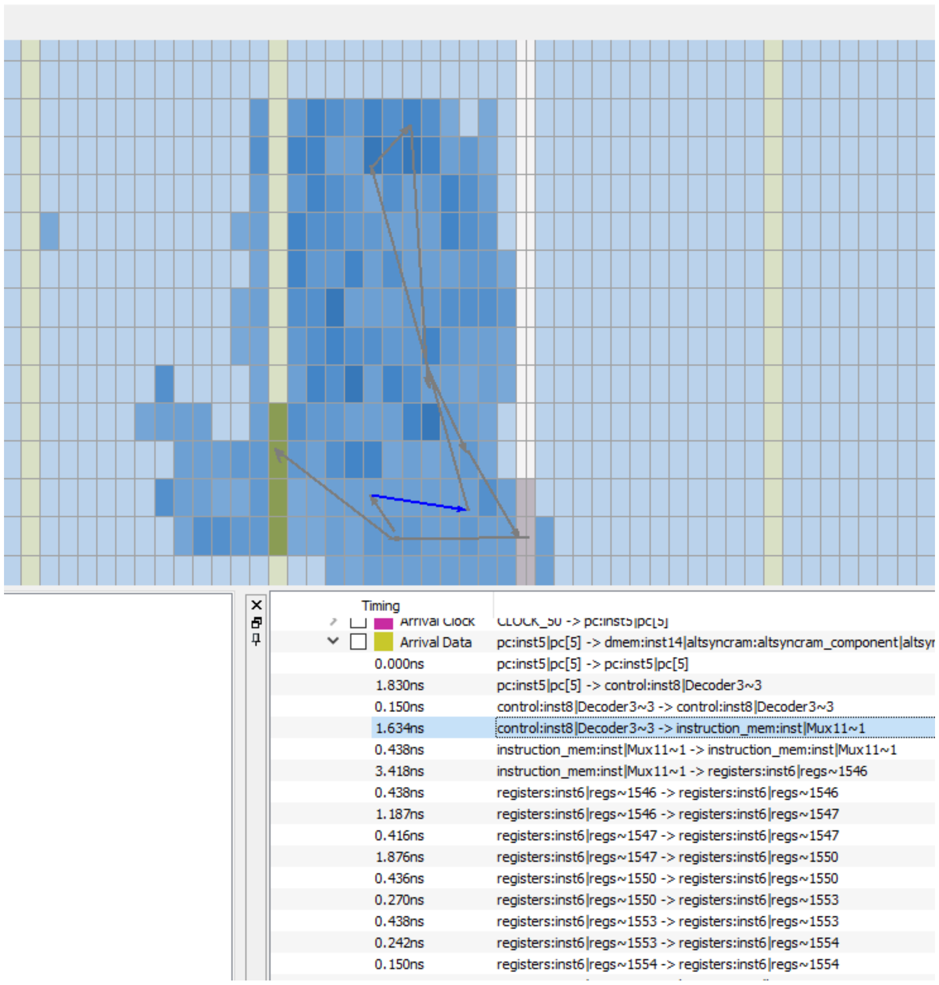
Register to mux (0.993)

3.4 Decode:



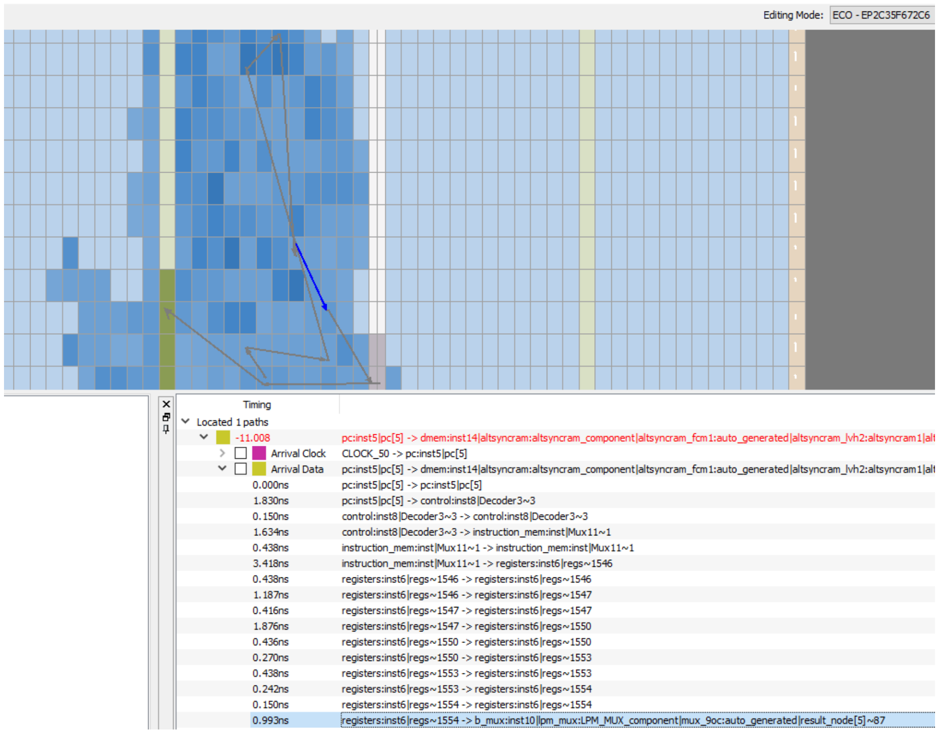
Timing	
🟪 Arrival Clock	CLOCK_50 -> pc:inst5|pc[5]
🟨 Arrival Data	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:
0.000ns	pc:inst5|pc[5] -> pc:inst5|pc[5]
1.830ns	pc:inst5|pc[5] -> control:inst8|Decoder3~3
0.150ns	control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
1.634ns	control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
0.438ns	instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
3.418ns	instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
0.438ns	registers:inst6|regs~1546 -> registers:inst6|regs~1546
1.187ns	registers:inst6|regs~1546 -> registers:inst6|regs~1547
0.416ns	registers:inst6|regs~1547 -> registers:inst6|regs~1547
1.876ns	registers:inst6|regs~1547 -> registers:inst6|regs~1550
0.436ns	registers:inst6|regs~1550 -> registers:inst6|regs~1550
0.270ns	registers:inst6|regs~1550 -> registers:inst6|regs~1553
0.438ns	registers:inst6|regs~1553 -> registers:inst6|regs~1553
0.242ns	registers:inst6|regs~1553 -> registers:inst6|regs~1554
0.150ns	registers:inst6|regs~1554 -> registers:inst6|regs~1554

Control Decoder (0.150ns)



🟪	Arrival Clock	CLOCK_50 -> pc:inst5|pc[5]
🟨	Arrival Data	pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsy
	0.000ns	pc:inst5|pc[5] -> pc:inst5|pc[5]
	1.830ns	pc:inst5|pc[5] -> control:inst8|Decoder3~3
	0.150ns	control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
	1.634ns	control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
	0.438ns	instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
	3.418ns	instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
	0.438ns	registers:inst6|regs~1546 -> registers:inst6|regs~1546
	1.187ns	registers:inst6|regs~1546 -> registers:inst6|regs~1547
	0.416ns	registers:inst6|regs~1547 -> registers:inst6|regs~1547
	1.876ns	registers:inst6|regs~1547 -> registers:inst6|regs~1550
	0.436ns	registers:inst6|regs~1550 -> registers:inst6|regs~1550
	0.270ns	registers:inst6|regs~1550 -> registers:inst6|regs~1553
	0.438ns	registers:inst6|regs~1553 -> registers:inst6|regs~1553
	0.242ns	registers:inst6|regs~1553 -> registers:inst6|regs~1554
	0.150ns	registers:inst6|regs~1554 -> registers:inst6|regs~1554

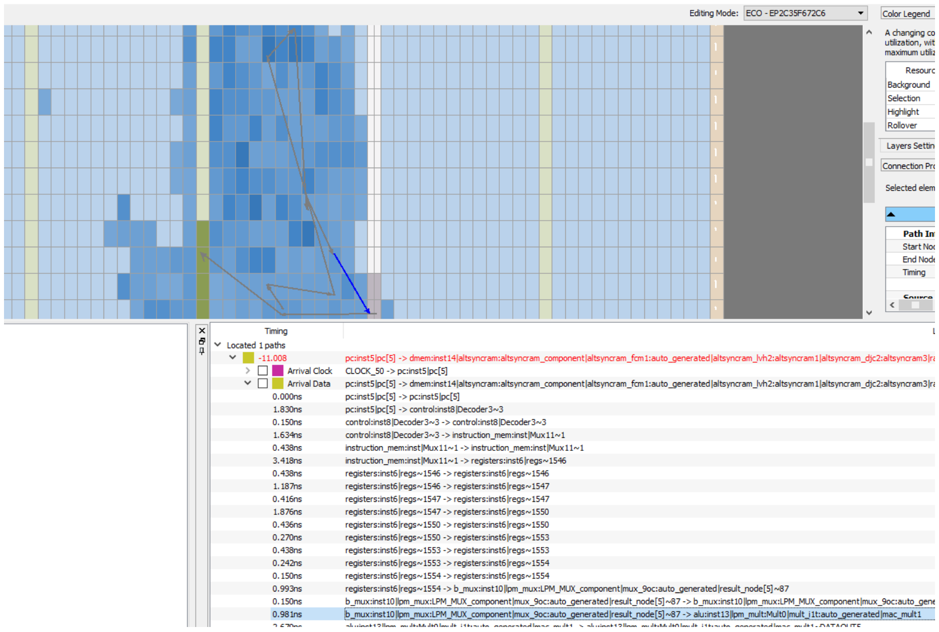
Control to mux (1.634ns)



```
Timing
Located 1 paths
  -11.008        pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|alt
  Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
  Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|alt
    0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
    1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
    0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
    1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
    0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
    3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
    0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
    1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
    0.416ns      registers:inst6|regs~1547 -> registers:inst6|regs~1547
    1.876ns      registers:inst6|regs~1547 -> registers:inst6|regs~1550
    0.436ns      registers:inst6|regs~1550 -> registers:inst6|regs~1550
    0.270ns      registers:inst6|regs~1550 -> registers:inst6|regs~1553
    0.438ns      registers:inst6|regs~1553 -> registers:inst6|regs~1553
    0.242ns      registers:inst6|regs~1553 -> registers:inst6|regs~1554
    0.150ns      registers:inst6|regs~1554 -> registers:inst6|regs~1554
    0.993ns      registers:inst6|regs~1554 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87
```

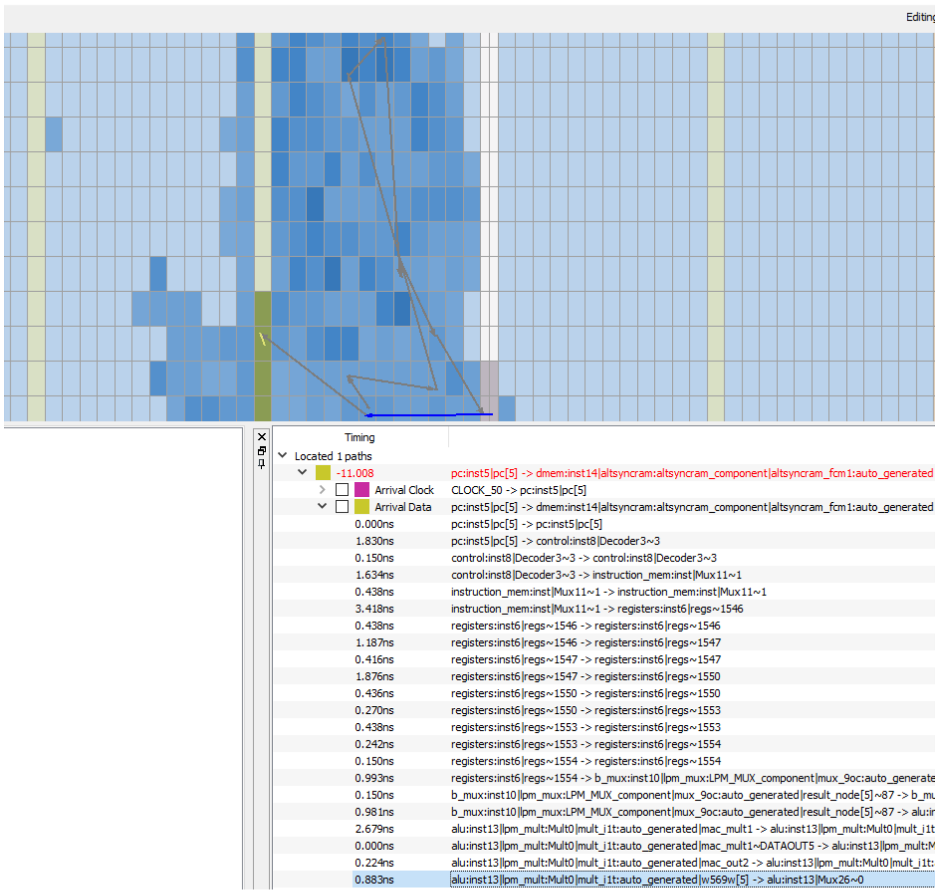
Registers to Bmux path (0.992ns)

3.5 Execution:



```
Timing
Located 1 paths
  -11.008        pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ra
  Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
  Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ra
    0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
    1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
    0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
    1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
    0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
    3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
    0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
    1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
    0.416ns      registers:inst6|regs~1547 -> registers:inst6|regs~1547
    1.876ns      registers:inst6|regs~1547 -> registers:inst6|regs~1550
    0.436ns      registers:inst6|regs~1550 -> registers:inst6|regs~1550
    0.270ns      registers:inst6|regs~1550 -> registers:inst6|regs~1553
    0.438ns      registers:inst6|regs~1553 -> registers:inst6|regs~1553
    0.242ns      registers:inst6|regs~1553 -> registers:inst6|regs~1554
    0.150ns      registers:inst6|regs~1554 -> registers:inst6|regs~1554
    0.993ns      registers:inst6|regs~1554 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87
    0.150ns      b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_gene
    0.981ns      b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1
```

Bmux to ALU Multiplier

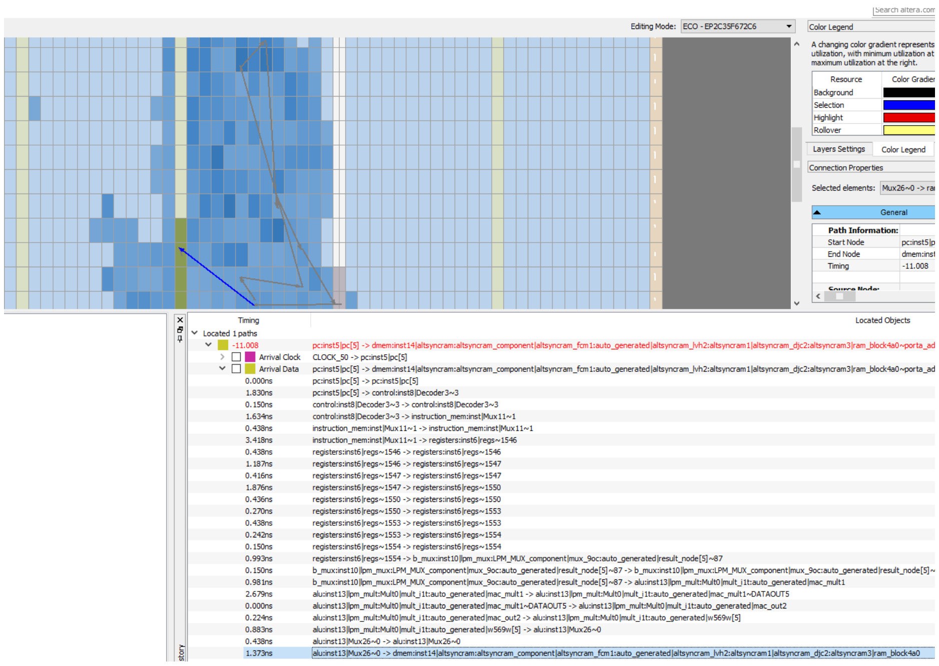


```
Timing
Located 1 paths
  -11.008        pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated
    Arrival Clock  CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data   pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated
      0.000ns      pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns      pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns      control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns      control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns      instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
      3.418ns      instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
      0.438ns      registers:inst6|regs~1546 -> registers:inst6|regs~1546
      1.187ns      registers:inst6|regs~1546 -> registers:inst6|regs~1547
      0.416ns      registers:inst6|regs~1547 -> registers:inst6|regs~1547
      1.876ns      registers:inst6|regs~1547 -> registers:inst6|regs~1550
      0.436ns      registers:inst6|regs~1550 -> registers:inst6|regs~1550
      0.270ns      registers:inst6|regs~1550 -> registers:inst6|regs~1553
      0.438ns      registers:inst6|regs~1553 -> registers:inst6|regs~1553
      0.242ns      registers:inst6|regs~1553 -> registers:inst6|regs~1554
      0.150ns      registers:inst6|regs~1554 -> registers:inst6|regs~1554
      0.993ns      registers:inst6|regs~1554 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generate
      0.150ns      b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> b_mu
      0.981ns      b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> alu:ir
      2.679ns      alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1 -> alu:inst13|lpm_mult:Mult0|mult_i1t
      0.000ns      alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1~DATAOUT5 -> alu:inst13|lpm_mult:M
      0.224ns      alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_out2 -> alu:inst13|lpm_mult:Mult0|mult_i1t:
      0.883ns      alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|w569w[5] -> alu:inst13|Mux26~0
```

Multiplier

Multiplication has a delay of 2.679ns for execution. The delay report states the time from the bmux to the alu multiplier to be 0.981ns. The result of the alu takes 0.883ns to go to the wb mux.

3.6 Memory:



Editing Mode: ECO - EP2C35F672C6

Color Legend

A changing color gradient represents
utilization, with minimum utilization at
maximum utilization at the right.

Resource	Color Gradier
Background	⬛
Selection	🟦
Highlight	🟥
Rollover	🟨

Connection Properties

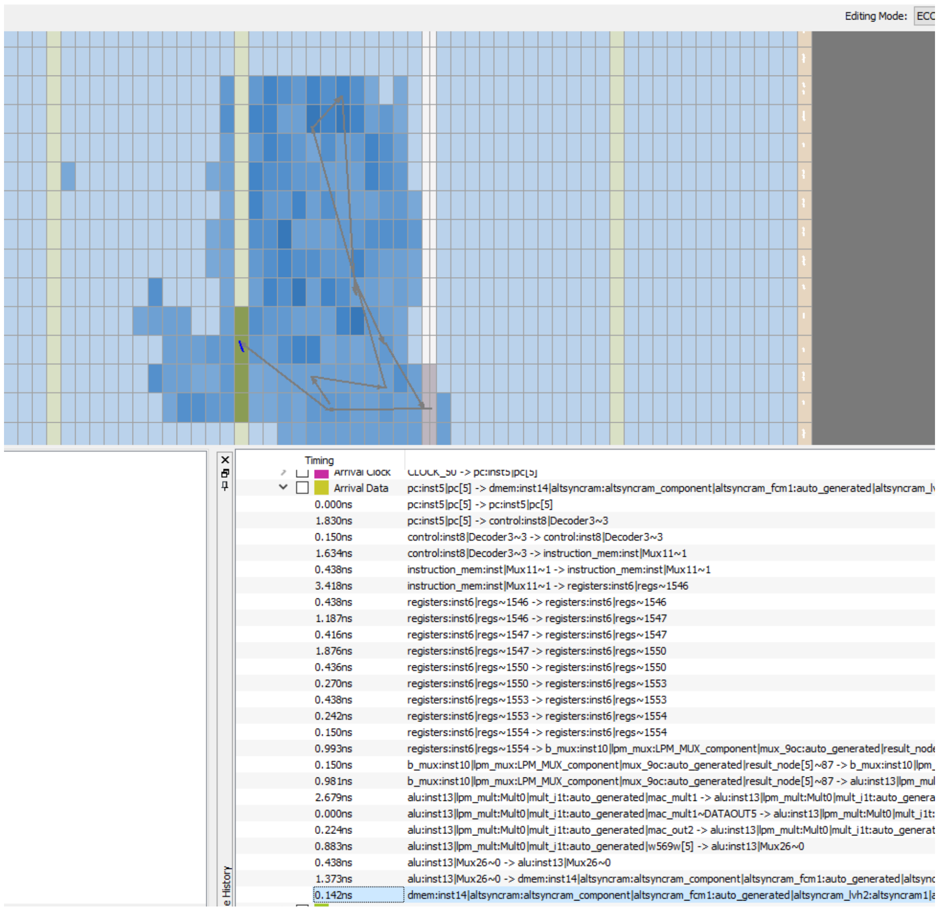
Selected elements: Mux26~0 -> ra

Path Information:	
Start Node	pc:inst5|p
End Node	dmem:inst
Timing	-11.008

```
Timing          Located Objects
Located 1 paths
  -11.008       pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0~porta_ad
    Arrival Clock   CLOCK_50 -> pc:inst5|pc[5]
    Arrival Data    pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0~porta_ad
      0.000ns   pc:inst5|pc[5] -> pc:inst5|pc[5]
      1.830ns   pc:inst5|pc[5] -> control:inst8|Decoder3~3
      0.150ns   control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
      1.634ns   control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
      0.438ns   instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
      3.418ns   instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
      0.438ns   registers:inst6|regs~1546 -> registers:inst6|regs~1546
      1.187ns   registers:inst6|regs~1546 -> registers:inst6|regs~1547
      0.416ns   registers:inst6|regs~1547 -> registers:inst6|regs~1547
      1.876ns   registers:inst6|regs~1547 -> registers:inst6|regs~1550
      0.436ns   registers:inst6|regs~1550 -> registers:inst6|regs~1550
      0.270ns   registers:inst6|regs~1550 -> registers:inst6|regs~1553
      0.438ns   registers:inst6|regs~1553 -> registers:inst6|regs~1553
      0.242ns   registers:inst6|regs~1553 -> registers:inst6|regs~1554
      0.150ns   registers:inst6|regs~1554 -> registers:inst6|regs~1554
      0.993ns   registers:inst6|regs~1554 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87
      0.150ns   b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~
      0.981ns   b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1
      2.679ns   alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1~DATAOUT5
      0.000ns   alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1~DATAOUT5 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_out2
      0.224ns   alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_out2 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|w569w[5]
      0.883ns   alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|w569w[5] -> alu:inst13|Mux26~0
      0.438ns   alu:inst13|Mux26~0 -> alu:inst13|Mux26~0
      1.373ns   alu:inst13|Mux26~0 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|altsyncram_djc2:altsyncram3|ram_block4a0
```

Mux to RAM (1.373ns)

3.7 Writeback:



```
        Arrival Clock   CLOCK_50 -> pc:inst5|pc[5]
        Arrival Data    pc:inst5|pc[5] -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_l
          0.000ns       pc:inst5|pc[5] -> pc:inst5|pc[5]
          1.830ns       pc:inst5|pc[5] -> control:inst8|Decoder3~3
          0.150ns       control:inst8|Decoder3~3 -> control:inst8|Decoder3~3
          1.634ns       control:inst8|Decoder3~3 -> instruction_mem:inst|Mux11~1
          0.438ns       instruction_mem:inst|Mux11~1 -> instruction_mem:inst|Mux11~1
          3.418ns       instruction_mem:inst|Mux11~1 -> registers:inst6|regs~1546
          0.438ns       registers:inst6|regs~1546 -> registers:inst6|regs~1546
          1.187ns       registers:inst6|regs~1546 -> registers:inst6|regs~1547
          0.416ns       registers:inst6|regs~1547 -> registers:inst6|regs~1547
          1.876ns       registers:inst6|regs~1547 -> registers:inst6|regs~1550
          0.436ns       registers:inst6|regs~1550 -> registers:inst6|regs~1550
          0.270ns       registers:inst6|regs~1550 -> registers:inst6|regs~1553
          0.438ns       registers:inst6|regs~1553 -> registers:inst6|regs~1553
          0.242ns       registers:inst6|regs~1553 -> registers:inst6|regs~1554
          0.150ns       registers:inst6|regs~1554 -> registers:inst6|regs~1554
          0.993ns       registers:inst6|regs~1554 -> b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node
          0.150ns       b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> b_mux:inst10|lpm_
          0.981ns       b_mux:inst10|lpm_mux:LPM_MUX_component|mux_9oc:auto_generated|result_node[5]~87 -> alu:inst13|lpm_mul
          2.679ns       alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_genera
          0.000ns       alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_mult1~DATAOUT5 -> alu:inst13|lpm_mult:Mult0|mult_i1t:
          0.224ns       alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|mac_out2 -> alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generat
          0.883ns       alu:inst13|lpm_mult:Mult0|mult_i1t:auto_generated|w569w[5] -> alu:inst13|Mux26~0
          0.438ns       alu:inst13|Mux26~0 -> alu:inst13|Mux26~0
          1.373ns       alu:inst13|Mux26~0 -> dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsync
          0.142ns       dmem:inst14|altsyncram:altsyncram_component|altsyncram_fcm1:auto_generated|altsyncram_lvh2:altsyncram1|a
```

Writeback to RAM (0.142ns)

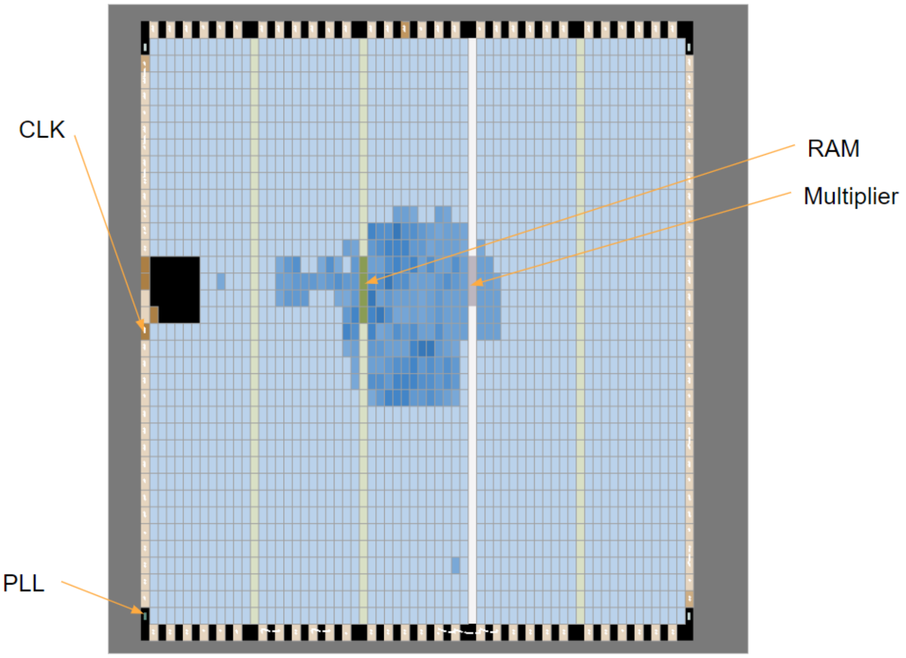
4 Part 4

Using the actual board, find the actual maximum frequency that your processor can sustain without producing incorrect results. You need to keep on incrementing the frequency of the design, and re-running your experiments. Once the processors fails in booting, report the lowest frequency in which such failure occurs. Contrast the actual maximum frequency to the estimated Fmax from the TimingQuest tool. If there are differences between the predicted and actual maximum frequency, explain potential reasons for these discrepancies.

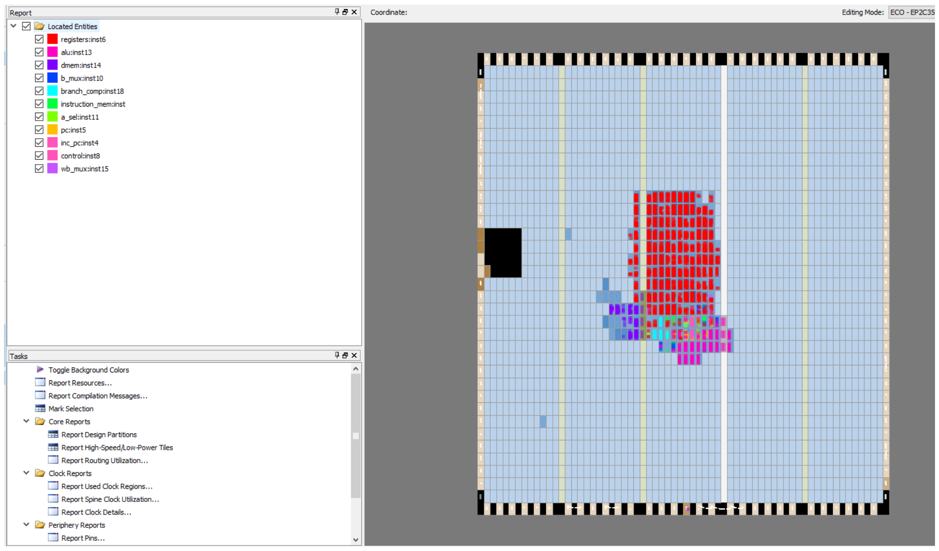
The actual maximum frequency the processor can sustain is 50MHz. This is higher than the predicted Fmax from the TimingQuest tool possibly because of differences in the processor and the fact that only factorial 6 is being calculated. When I ran the factorial program for larger values of the Fib program for example with the 50MHz, the output was not valid. But halfing the clock to 25MHz and rerunning these programs resulted in the correct memory inputs.

5 Part 5

Print and annotate the floorplan of your design.



Here is an overview of some floor plan components.



Report

- ✓ Located Entities
  - ✓ 🟥 registers:inst6
  - ✓ 🟪 alu:inst13
  - ✓ 🟪 dmem:inst14
  - ✓ 🟦 b_mux:inst10
  - ✓ 🟦 branch_comp:inst18
  - ✓ 🟩 instruction_mem:inst
  - ✓ 🟩 a_sel:inst11
  - ✓ 🟧 pc:inst5
  - ✓ 🟪 inc_pc:inst4
  - ✓ 🟪 control:inst8
  - ✓ 🟪 wb_mux:inst15

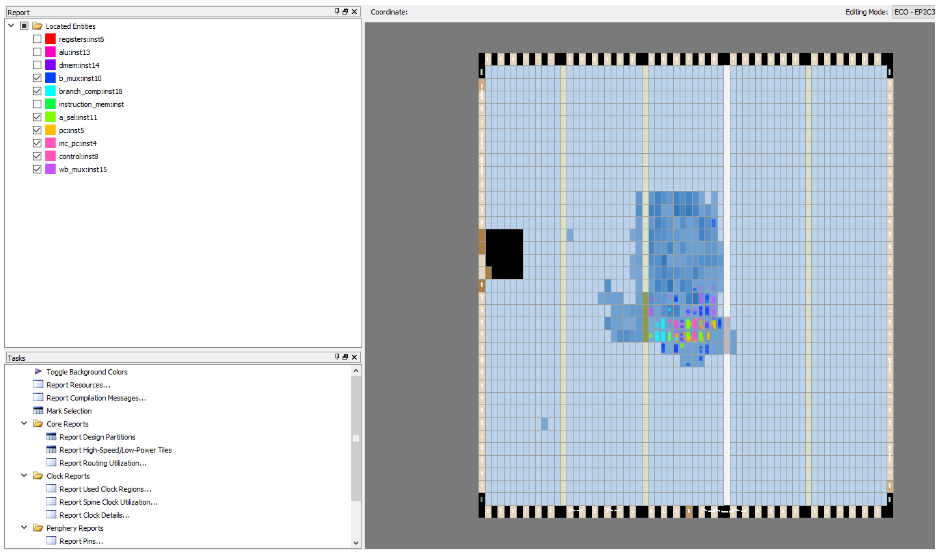
Tasks

- Toggle Background Colors
- Report Resources...
- Report Compilation Messages...
- Mark Selection
- Core Reports
  - Report Design Partitions
  - Report High-Speed/Low-Power Tiles
  - Report Routing Utilization...
- Clock Reports
  - Report Used Clock Regions...
  - Report Spine Clock Utilization...
  - Report Clock Details...
- Periphery Reports
  - Report Pins...

Coordinate:

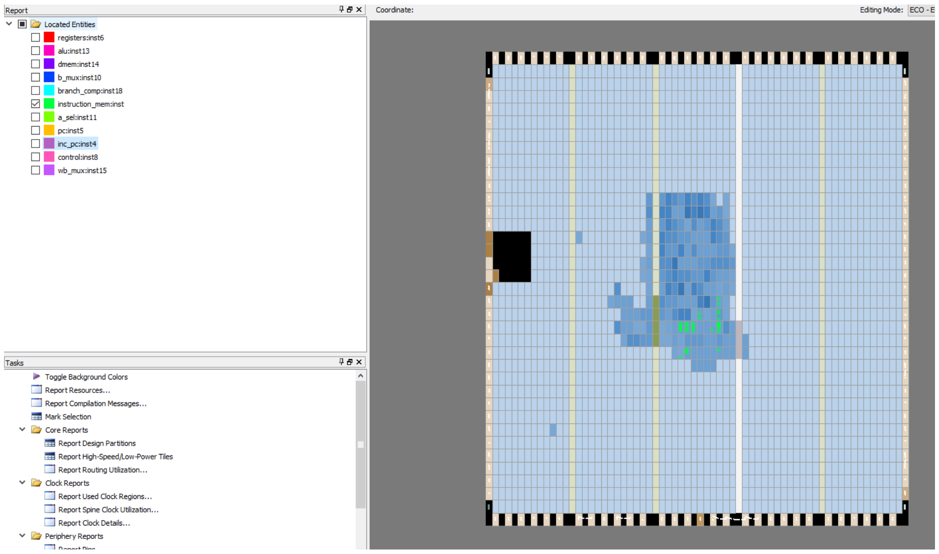
Editing Mode: ECO - EP2C35

Floor plan fully annotated.


Report

Located Entities
- ☐ 🟥 registers:inst6
- ☐ 🟪 alu:inst13
- ☐ 🟪 dmem:inst14
- ☑ 🟦 b_mux:inst10
- ☑ 🟦 branch_comp:inst18
- ☐ 🟩 instruction_mem:inst
- ☑ 🟩 a_sel:inst11
- ☑ 🟧 pc:inst5
- ☑ 🟪 inc_pc:inst4
- ☑ 🟪 control:inst8
- ☑ 🟪 wb_mux:inst15

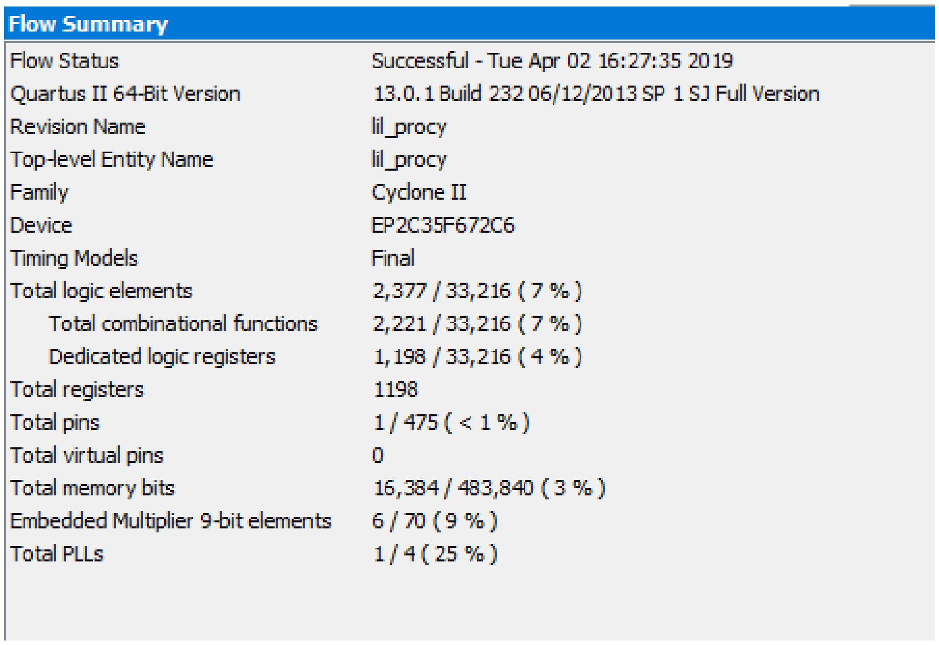
Smaller components annotated to make it easier to see on floor plan.


Report

Located Entities
- ☐ 🟥 registers:inst6
- ☐ 🟪 alu:inst13
- ☐ 🟪 dmem:inst14
- ☐ 🟦 b_mux:inst10
- ☐ 🟦 branch_comp:inst18
- ☑ 🟩 instruction_mem:inst
- ☐ 🟩 a_sel:inst11
- ☐ 🟧 pc:inst5
- ☐ 🟪 inc_pc:inst4
- ☐ 🟪 control:inst8
- ☐ 🟪 wb_mux:inst15

Instruction Memory annotated to make it easier to see on floor plan.

Report the resources being used by your processor: LEs (combinational and dedicated registers), PLL, embedded multipliers, memory blocks, and routing resources. Make sure to remove any SignalTap logic if you used it.



Flow Summary

Flow Status	Successful - Tue Apr 02 16:27:35 2019
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	lil_procy
Top-level Entity Name	lil_procy
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	2,377 / 33,216 (7 %)
Total combinational functions	2,221 / 33,216 (7 %)
Dedicated logic registers	1,198 / 33,216 (4 %)
Total registers	1198
Total pins	1 / 475 (< 1 %)
Total virtual pins	0
Total memory bits	16,384 / 483,840 (3 %)
Embedded Multiplier 9-bit elements	6 / 70 (9 %)
Total PLLs	1 / 4 (25 %)