Digital Logic

Implementation Technology

Ru Han

1

Digital Logic and Verilog

Appendix B

How do transistors work as a switch?

How are devices actually built?

B.1, B.2, B.3, B.8.1, B.8.7, B.8.8

Implementation Technology

- MOS Transistors
- How Do MOS Transistors Work?
- Use MOS to Build Gates
- Design Procedure

2

MOS Transistors

MOSFET:

- Metal-Oxide Silicon Field-Effect Transistor
- A 3-terminal device that acts as a voltage-controlled switch.
- Two flavors:
  - NMOS (n-type, n-channel)
  - PMOS (p-type, p-channel)

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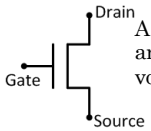
B.1 Transistor Switches

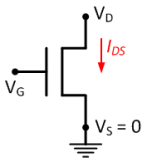
NMOS Transistor

- **Symbol**



A switch between ***Source*** and ***Drain***, controlled by voltage at ***Gate***.

- **Circuit**



Switch Model

V_G = High (+5V)	V_G = Low (0V)
$V_D \approx 0$	$V_D \neq 0$
$I_{DS} > 0$	$I_{DS} \approx 0$
$V_S = 0$	$V_S = 0$
ON	**OFF**

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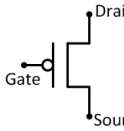
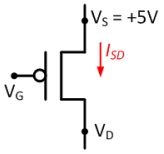
PMOS Transistor

- **Symbol**



A switch between ***Source*** and ***Drain***, controlled by voltage at ***Gate***.

- **Circuit**



Switch Model

V_G = High (+5V)	V_G = Low (0V)
$V_S = +5V$	$V_S = +5V$
$I_{SD} \approx 0$	$I_{SD} > 0$
$V_D \neq +5V$	$V_D \approx +5V$
OFF	**ON**

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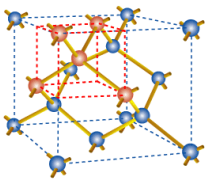
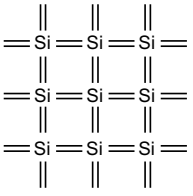
How Do MOS Transistors Work?

- **Semiconductor**: A material (e.g., silicon) that normally does not conduct electricity, unless something is done to cause a concentration of charged particles, forming a conducting region.
- **Silicon** is a Group IV material, forming crystal lattice with bonds to four neighbors





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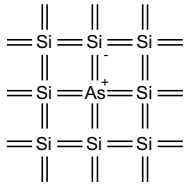
How Do MOS Transistors Work?

- **n-type**: A semiconductor which contains *a net excess of electrons*
  ⇒ Negative charges
- **p-type**: A semiconductor in which the ions have *a lack of electrons*
  ⇒ Positive charges (holes)



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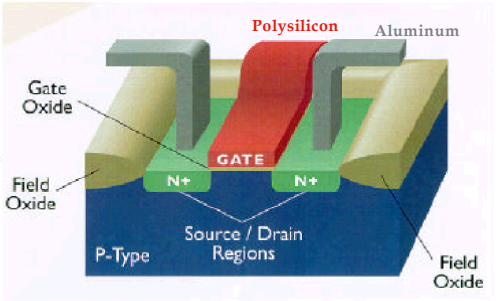
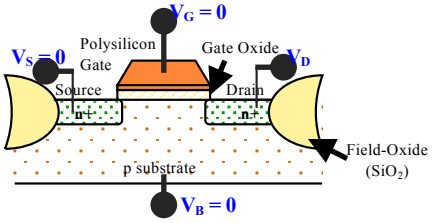
The MOS Transistor



8

N-type MOS Operation

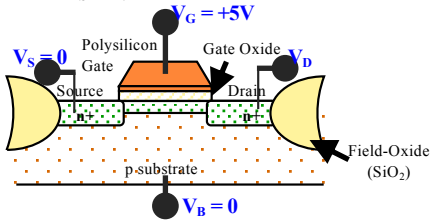
- V_G = Low ⇒ Transistor is OFF
- In this state, the p-channel region does not conduct
  ⇒ $I_{DS} \approx 0$; $V_D \neq 0$



9

N-type MOS Operation Cont.

- V_G = High ⇒ Transistor is ON
- Negative charge attracted to body
- Inverts a channel under gate to n-type
- Current can flow through channel between drain and source ⇒ $I_{DS} > 0$; $V_D \approx 0$



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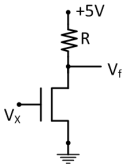
B.2 NMOS Logic Gates

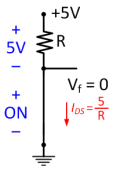
Use MOSFET's to Build Gates

NMOS Inverter

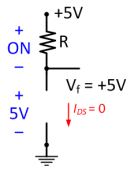


V_X	V_f
0	1
1	0

V_X = High ⇒ FET is ON



V_X = Low ⇒ FET is OFF



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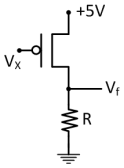
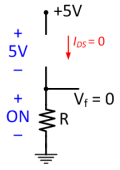
Use MOSFET's to Build Gates

PMOS Inverter

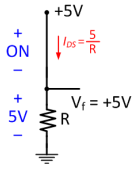


V_X	V_f
0	1
1	0

V_X = High ⇒ FET is OFF



V_X = Low ⇒ FET is ON



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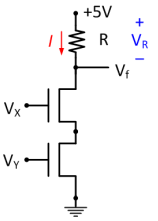
USE MOSFET'S TO BUILD GATES

NMOS NAND Gate

V_X	V_Y	V_f
0	0	1
0	1	1
1	0	1
1	1	0



If both V_X and V_Y are High
⇒ Both FET's are ON
⇒ V_f connected to Ground
⇒ $V_f = 0$

If either V_X or V_Y is low
⇒ No path to Ground
⇒ $I = 0$
⇒ $V_R = 0$
⇒ $V_f = +5V$

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B.3 CMOS LOGIC GATES

- We can proceed to show NMOS versions of AND, NOR, OR, etc.
- However, these gates experience problems:
  - Achieving proper logic levels at V_f (High ≈ +5V, Low ≈ 0V) is critically dependent on the value of R.
  - When FET's are ON, significant current may pass through R & FET ⇒ Power dissipation, heat
  - Gates are often used to drive other gates. This means we have many R values to choose simultaneously, and many opportunities for heating.
- Solution: **CMOS** – Complementary MOS
  - NMOS + PMOS FET's are arranged in complementary pairs.

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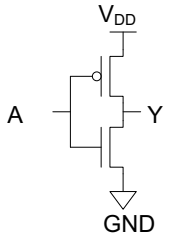
CMOS INVERTER

A	Y
0	
1	



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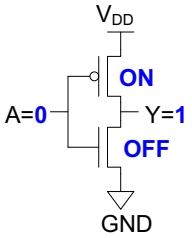
CMOS INVERTER

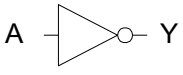
A	Y
0	1
1	

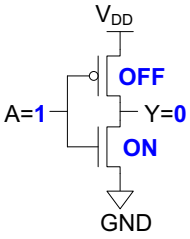


16

CMOS INVERTER

A	Y
0	1
1	0





Advantages over NMOS & PMOS:
(a) No R value to choose;
(b) Small current drain in either state.

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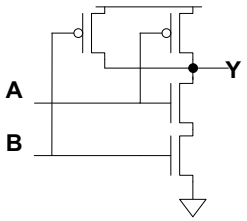
CMOS 2-INPUT NAND GATE

A	B	Y
0	0	
0	1	
1	0	
1	1	



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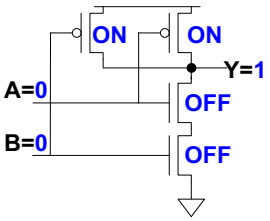
CMOS 2-Input NAND Gate

A	B	Y
0	0	1
0	1	
1	0	
1	1	



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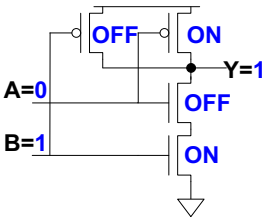
CMOS 2-Input NAND Gate

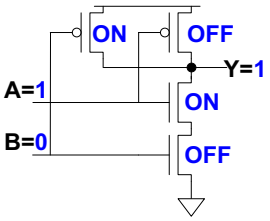
A	B	Y
0	0	1
0	1	1
1	0	
1	1	



20

CMOS 2-Input NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	



Output Y is '1' only when either inputs A OR B is '0'.
⇒ PMOS FET's are connected in parallel.

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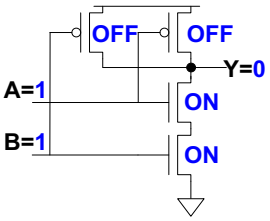
CMOS 2-Input NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Output Y is '0' only when inputs A AND B both are '1'.
⇒ NMOS FET's are connected in series.

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CMOS NOR Gate

Design Considerations

- Truth Table

V_X	V_Y	V_f
0	0	1
0	1	0
1	0	0
1	1	0

- $V_f = 1$ (Pulled up) only when both $V_X = 0$ AND $V_Y = 0$
  - $= 0$: p-type
  - AND: in series
- $V_f = 0$ (Pulled down) whenever $V_X = 1$ OR $V_Y = 1$
  - $=1$: n-type
  - OR: in parallel

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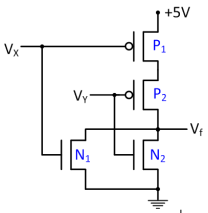
CMOS NOR Gate

Circuit Diagram



Verification

V_X	V_Y	P_1	P_2	N_1	N_2	V_f
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

CMOS OR Gate

Take output from CMOS NOR, connect to input of CMOS invertor.

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Other Logic Functions

A. By appropriate choice of a PMOS PUN (pull-up network) and a complementary NMOS PDN (pull-down network), we can find a CMOS circuit for any logical function, provided that all variables in the expression are complemented.

Ex: (a) $f = \overline{A}\,\overline{B} + \overline{A}\,\overline{C}$ √

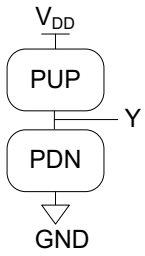
(b) $f = A\,\overline{B} + \overline{A}\,\overline{C}$ X

B. Other logic functions can be realized by placing CMOS inverters on the inputs and/or outputs as needed.

Other Logic Functions

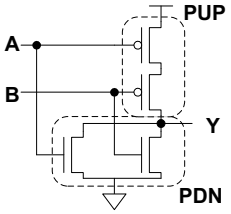
C. The PUN and PDN must be complementary.

- If two PMOS FETs are connected ***in series*** in the PUN, then the corresponding NMOS FETs must be connected ***in parallel*** in the PDN.
- If two PMOS FETs are connected ***in parallel*** in the PUN, then the corresponding NMOS FETs must be connected ***in series*** in the PDN.



Other Logic Functions

- Pull-up net (PUP) off when pull-down (PDN) on
- PUP implemented as complement of PDN (Complementary MOS)
- If two FETs in parallel in PDN, counterparts in series in PUP
- Output (Y) connected to VDD or GND, never both



Design Procedure

1) Manipulate f into proper form:
   - All variables complemented
   - Appear as few times as possible

   Example: $f = \overline{A}\,\overline{B} + \overline{A}\,\overline{C} = \overline{A}\,(\overline{B} + \overline{C})$

2) PUN: If two expressions are joined by **OR**, then their PMOS FETS should be connected **in parallel**.
   AND ⇒ in series.

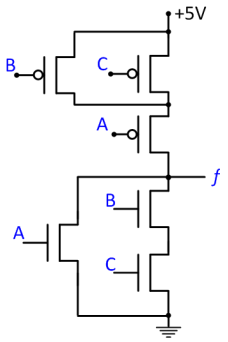
3) PDN: Determine $\overline{f}$ using DeMorgan's Theorem.
   OR ⇒ in parallel. AND ⇒ in series.

Design Procedure

4) Example 1:

$f = \overline{A}\,(\overline{B} + \overline{C})$

$\overline{f} = A + B\,C$



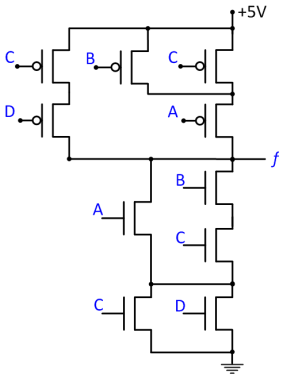
Design Procedure

4) Example 2:

$f = \overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{C}\,\overline{D}$

$= \overline{A}\,(\overline{B} + \overline{C}) + \overline{C}\,\overline{D}$

$\overline{f} = (A + BC)\,(C + D)$

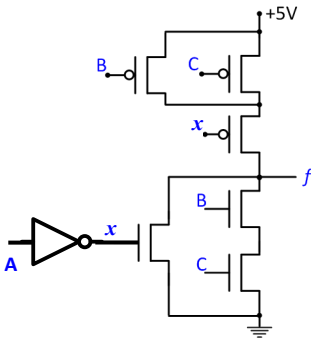


Other Logic Functions

- Example 3:
  $f = A\,\overline{B} + A\,\overline{C}$

  Let $x = \overline{A}$,

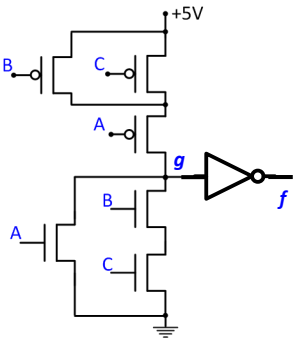
  $f = \overline{x}\,\overline{B} + \overline{x}\,\overline{C}$
  $= \overline{x}\,(\overline{B} + \overline{C})$
  $\overline{f} = x + BC$



Other Logic Functions

- Example 4:
  $f = A + BC$

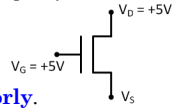
  Let $g = \overline{f}$,
  $g = \overline{A}\,(\overline{B} + \overline{C})$
  $\overline{g} = A + B\,C$



Why Use PMOS in PUN and NMOS in PDN?

- An NMOS transistor turns ON by forming an n-type conducting channel.
  - This channel will only conduct efficiently if $V_G > V_S$
  - Consider NMOS in PUN, V_S should be pulled up to +5V. Then $V_S \approx V_G$ and the channel conducts poorly.

  ⇒ Bad logic levels at output.
  +5V → 3.5V
  0V → 0V

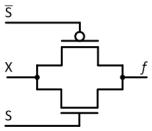


  NMOS passes 0s well and 1s poorly.

- Similarly, a PMOS will function poorly in a PDN.
  PMOS passes 1s well and 0s poorly.

B.8.8 Transmission Gate

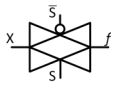
- **Basic Circuit**



  S and $\overline{S}$ must be complements

- **Operations**
  (a) S=0 & $\overline{S}$=1: PMOS & NMOS OFF ⇒ **open circuit**
  (b) S=1 & $\overline{S}$=0: PMOS & NMOS ON ⇒ **short circuit**
  (c) Need both PMOS and NMOS so that both 0s and 1s are "passed".

- **Symbol**



S	f	
0	Z	*High Impedance*
1	X	

XOR Gate

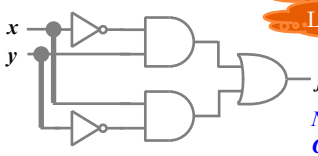
- Truth Table

x	y	x ⊕ y
0	0	0
0	1	1
1	0	1
1	1	0

$f = \overline{x}\,y + x\,\overline{y}$

- SOP Realization

Less transistors?
Less transistors?
Less transistors?



$f = x \oplus y$

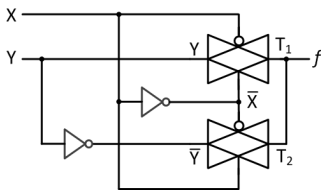
Number of transistors ?
Cost ?

XOR Gate

- Transmission Gate Realization

$$f = \overline{x}\,y + x\,\overline{y} = \begin{cases} y & \text{if } x = 0 \\ \overline{y} & \text{if } x = 1 \end{cases}$$

Number of transistors ?



$x = 0$: T_1 on, T_2 off
$\Rightarrow f = y$

$x = 1$: T_1 off, T_2 on
$\Rightarrow f = \overline{y}$

CONCLUSION

- Understanding the operation scheme of MOSFET
- Can build simple circuit using CMOS

- Assignment:
- B.1, B.6 ,B.8 , B.10, B.12 on Pages 814-818:

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XNOR GATE

- 1. Design the simplest POS circuits.
- 2. Implement the XNOR function using only NOR gates.
- 3. Derive a CMOS complex gate for XNOR. Use as few transistors as possible.
- 4. Could you give a circuit that use less transistors than CMOS complex gate? If yes, please give us the circuit.

Write down answers on one single paper .
Hand out it with your name and student number .

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