SHORT PRESENTATION

OFFSET CANCELLATION TECHNIQUE

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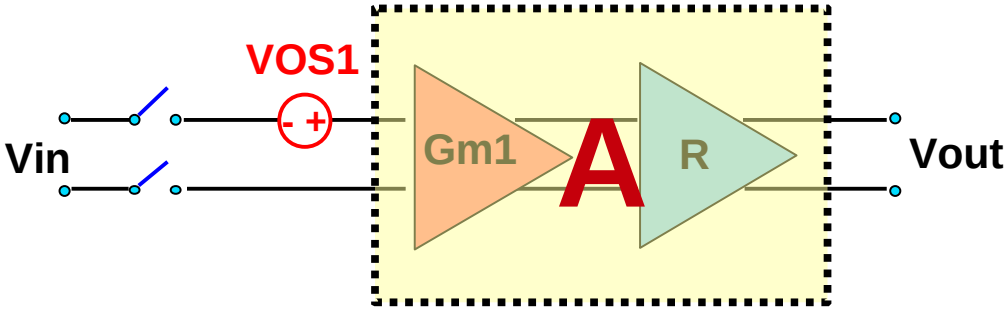
Outline

1. DC offset
2. Effects of DC offset
3. Offset Cancellation Technique using G_m and R stages
4. Realization of offset cancellation using G_m and R stages
5. Conclusion

1) DC offset

In ideal differential pair, with perfect symmetry ,when Vin=0, Vout=0

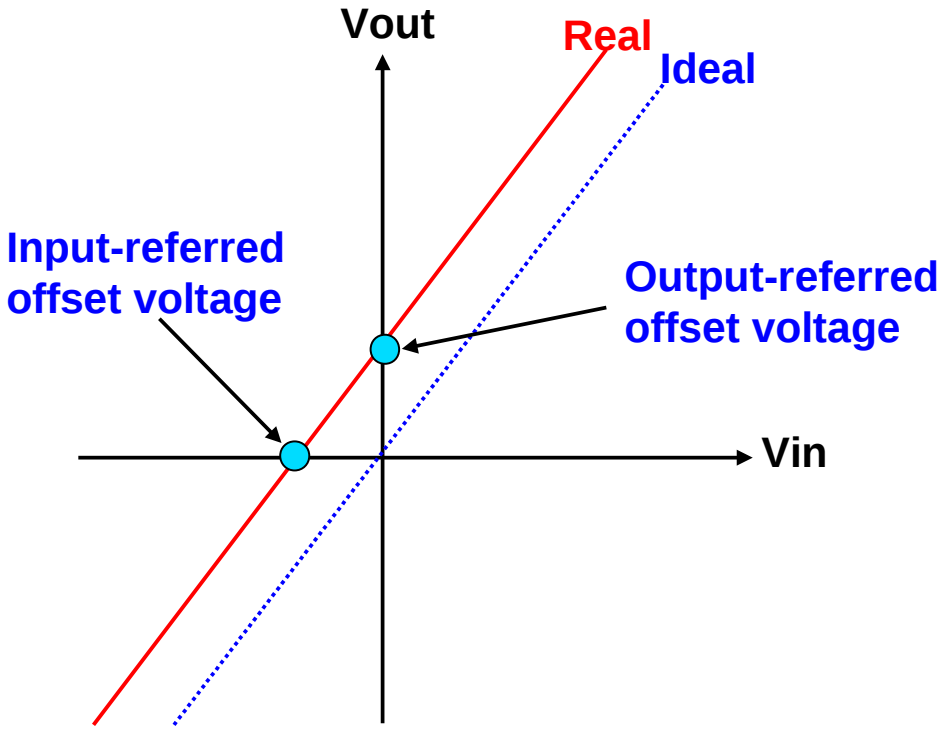
However , in real differential pair, with the presence of mismatches, when Vin=0 , Vout≠0 => The circuit suffer from a DC offset.



VOS1: Input-referred offset voltage

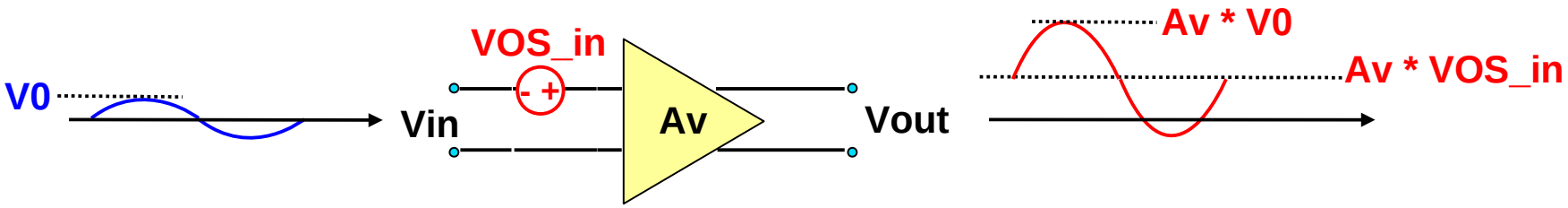
VOS_out= A * VOS_in

VOS_out: output-referred offset voltage
VOS_in: input-referred offset voltage
A : voltage gain

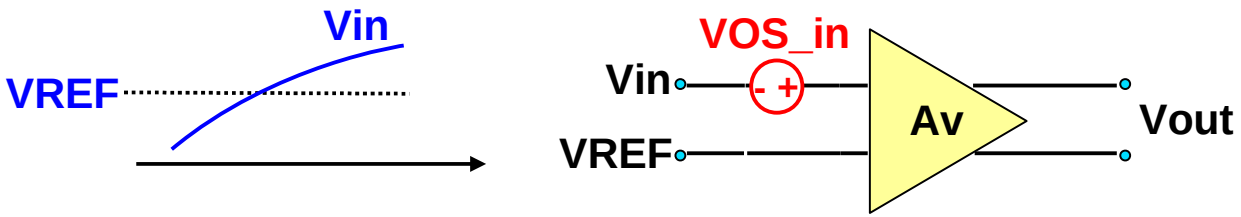


2) Effects of DC offset

The DC offset may experience so much gain that it drives the latter stages into nonlinear operation.



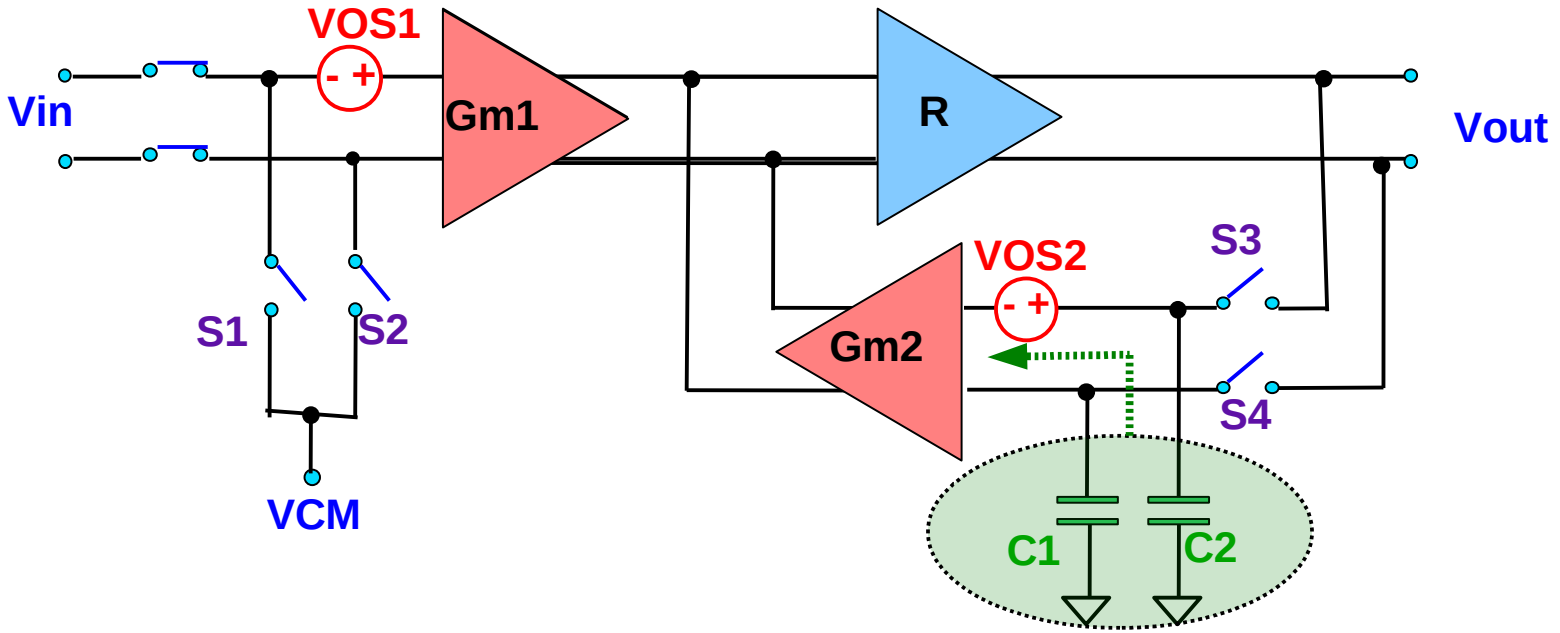
Precision limitation of an amplifier due to DC offset.



=> Many high-precision systems require electronic cancellation of the offsets. Offset cancellation can also reduce 1/f noise of amplifier considerably.

3) Offset Cancellation Technique using G_m and R stages (1)

General



Two storage capacitors C1 and C2 is used to measure and store the output-referred offset voltage. The storage voltage contributes to cancel the DC offset.

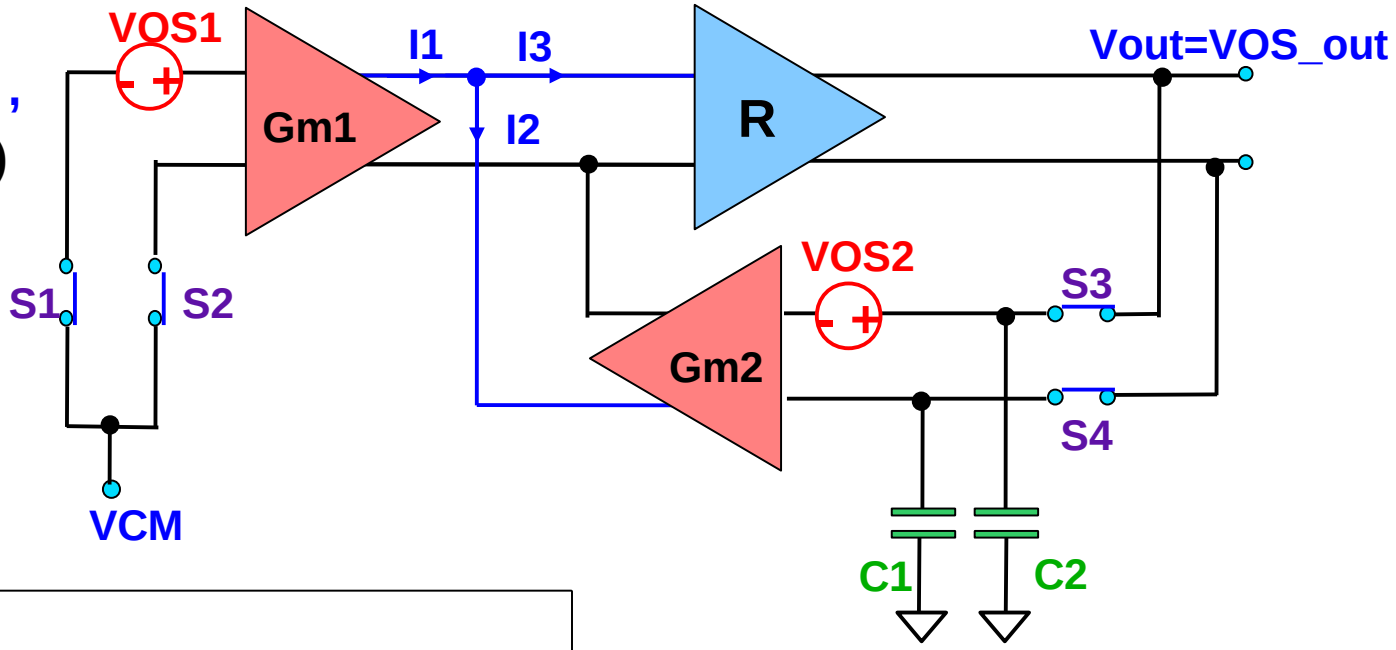
_ **Sensing period:** *Vin is disable and all switches are ON , **C1 and C2 sense the voltage of Vout.***

_ **Storing period:** *Vin is enable and all switches are OFF, the voltage store in **C1 and C2 contribute to cancel the offset voltage.***

3) Offset Cancellation Technique using G_m and R stages (2)

Sensing period

Vin is disable and S1, S2 , S3 , S4 are ON , (Vin = 0)



I1 = Gm1 * VOS1
I2 = Gm2 * (Vout-VOS2)
I3 = I1 - I2 = Gm1 * VOS1 - Gm2 * (Vout-VOS2)
Vout= I3 * R = {Gm1 * VOS1 - Gm2 * (Vout-VOS2) } * R

$$V_{out} = VOS_{out} = \frac{G_{m1} R V_{OS1} + G_{m2} R V_{OS2}}{1 + G_{m2} R}$$

C1 and C2 sense and store V output-referred offset voltage.

3) Offset Cancellation Technique using G_m and R stages (3)

Storing period

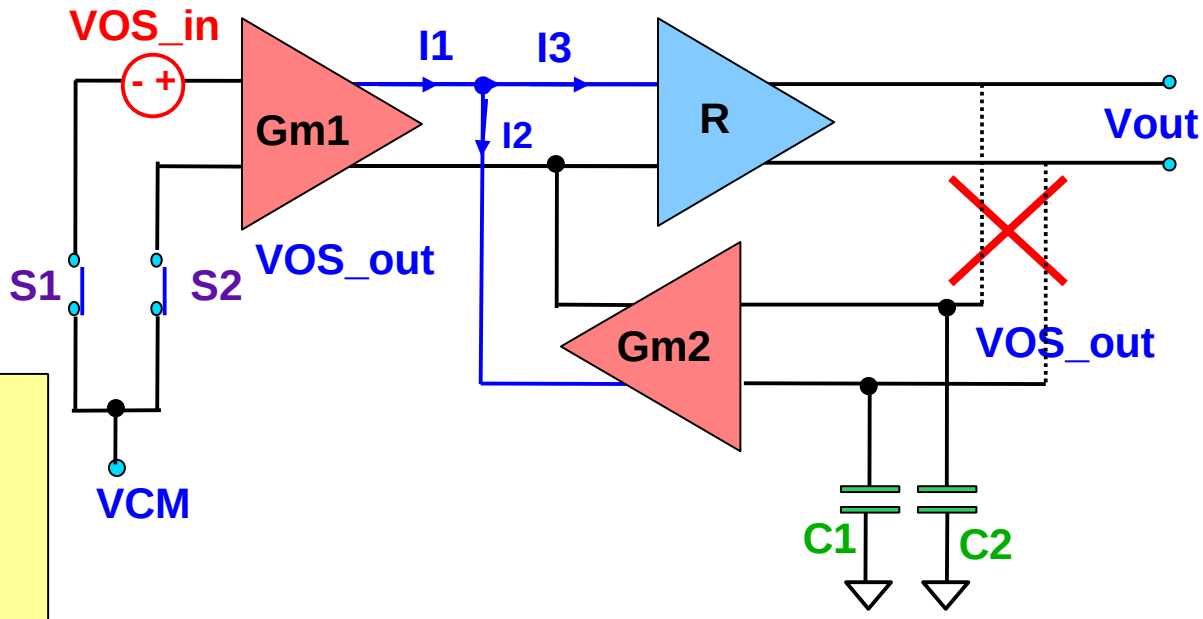
S3, S4 is OFF , S1, S2 is still ON (Vin = 0)

VOS_out = VOS_in * Gm1 * R => Let find the input-referred offset voltage VOS_in

$$V_{out} = VOS_{out} = \frac{G_{m1} R V_{OS1} + G_{m2} R V_{OS2}}{1 + G_{m2} R}$$

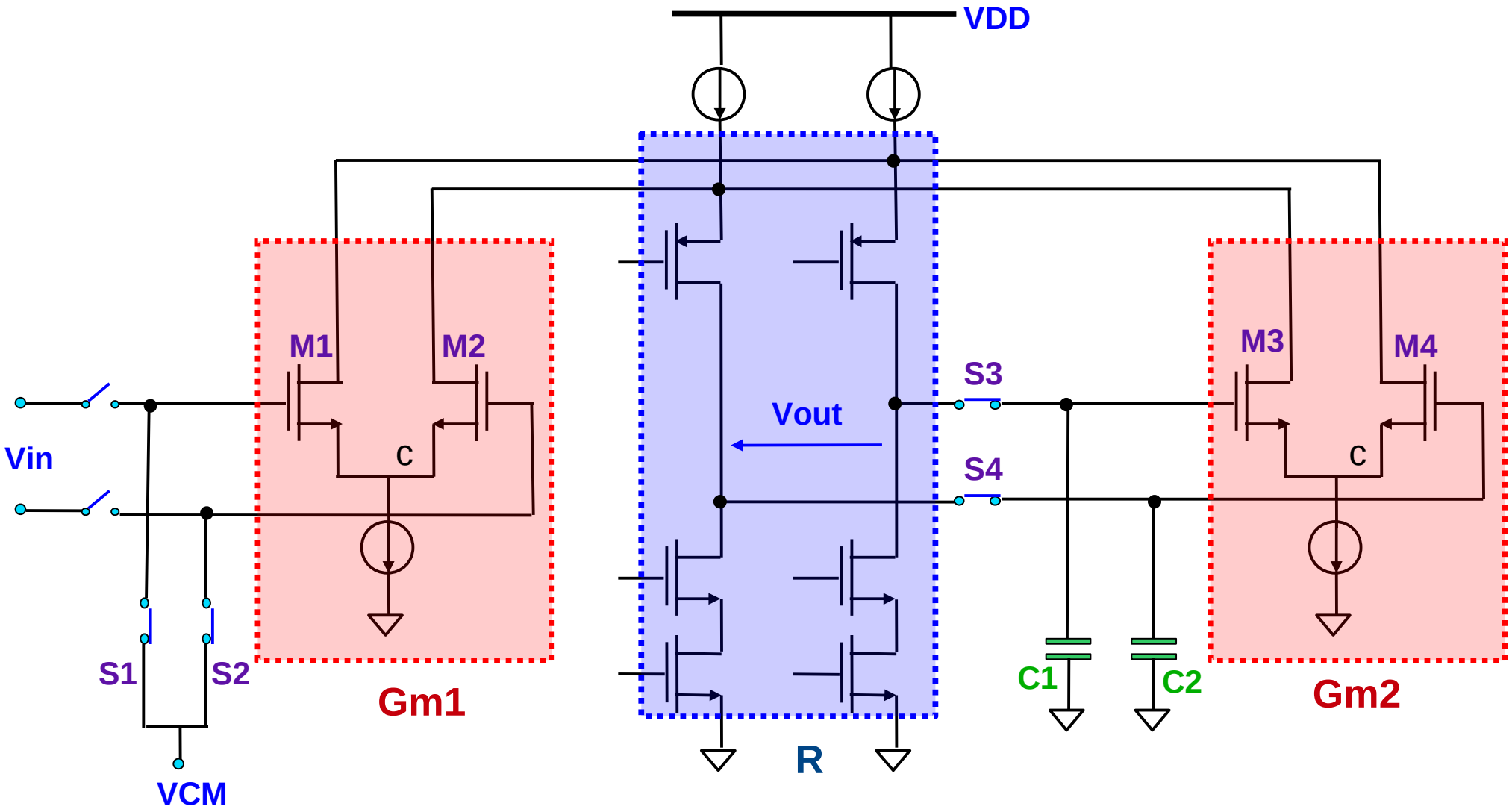
$$V_{OS\ in} = \frac{V_{out}}{G_{m1} R} = \frac{V_{OS1}}{1 + G_{m2} R} + \frac{G_{m2}}{G_{m1}} \frac{V_{OS2}}{1 + G_{m2} R}$$

$$V_{OS\ in} \approx \frac{V_{OS1}}{G_{m2} R} + \frac{V_{OS2}}{G_{m1} R}$$



Because Gm * R >>1 , VOS_in is very small, the input offset is canceled.

4) Realization of offset cancellation using Gm and R stages



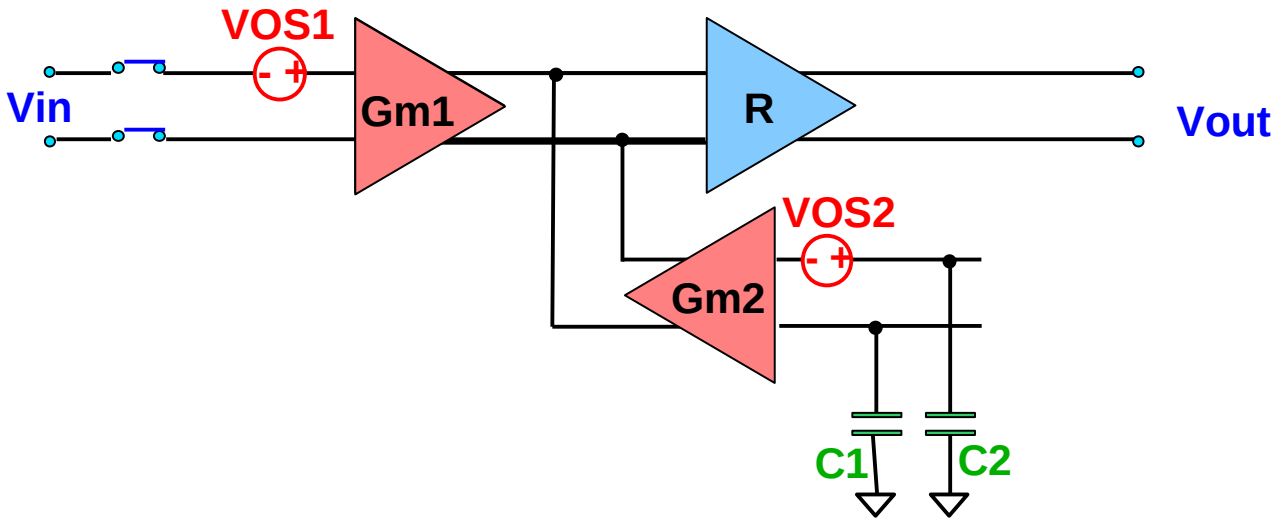
5) Conclusion (1)

Advantage

_ This offset cancellation scheme can isolate the signal path from the offset storage capacitors, prevent the circuit from phase margin degrading and settling speed limiting.

_ This offset cancellation technique uses only one voltage gain stage and therefore, it is suitable in a high-speed op amp.

_ Offset cancellation can reduce low frequency noise.

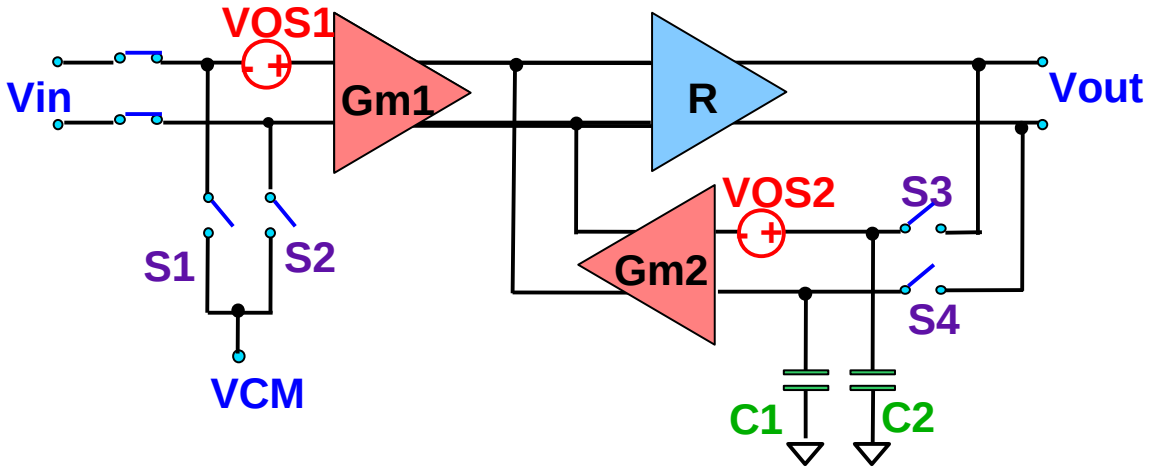


5) Conclusion (2)

Disadvantage and Issues

_ **S3 and S4 may inject slightly unequal charges onto C1 and C2, respectively, creating an error voltage. To solve this issue, Gm2 ≈ 0.1 Gm1 is chosen => Trade-off between off-set voltage and injection error.**

_ **A periodic refreshing is required because the junction and sub-threshold leakage of the switches eventually corrupts the correction voltage stored across the capacitors. In typical design, the offset must be refreshed at a rate of at least a few kHz.**



Thank you for listening!!!