Short presentation

ESD protection devices

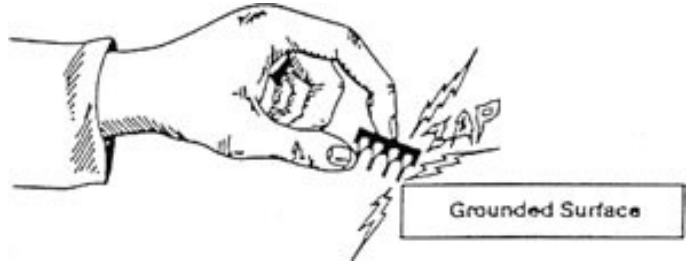
Renesas Design Vietnam Co., Ltd.
Circuit Design Group
Vuong Hoang

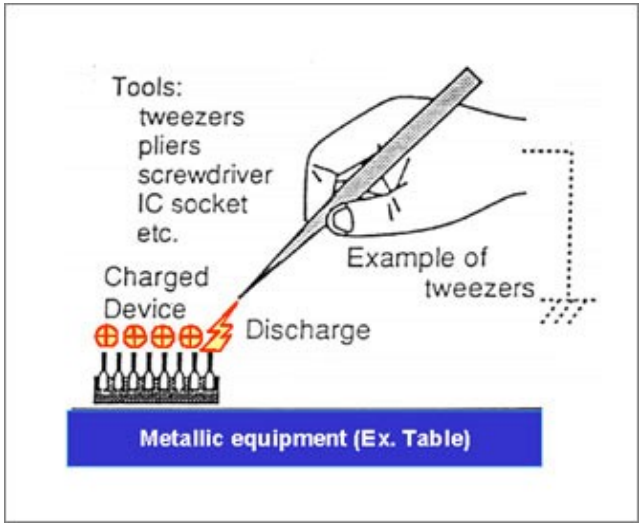
April 18th, 2014

Outline

Outline

1. Overview of ESD





ESD – Electrostatic Discharge

- A sudden flow of electricity between 2 electrically charged objects caused by contact.
- Occur only when the *voltage differential between 2 objects is sufficiently high*.

---> ***High voltage*** and ***large current*** due to ESD can destroy gate oxide, metal line and junction.

ESD can occur in one of following ways:

- a charged body touches an IC
- a charged IC touches a grounded surface.
- a charged machine touches an IC.
- an electrostatic field induces a voltage across a dielectric sufficient to break it down.

→ Some additional devices are used to protect internal circuit from ESD event.
To understand how these devices can protect circuit under ESD event, this material introduce 4 kinds of ESD protection device and their operation.

Outline

2. ESD protection device

Purpose:

- Providing a *low-impedance path* from input to supply *during ESD event* → absorb current.

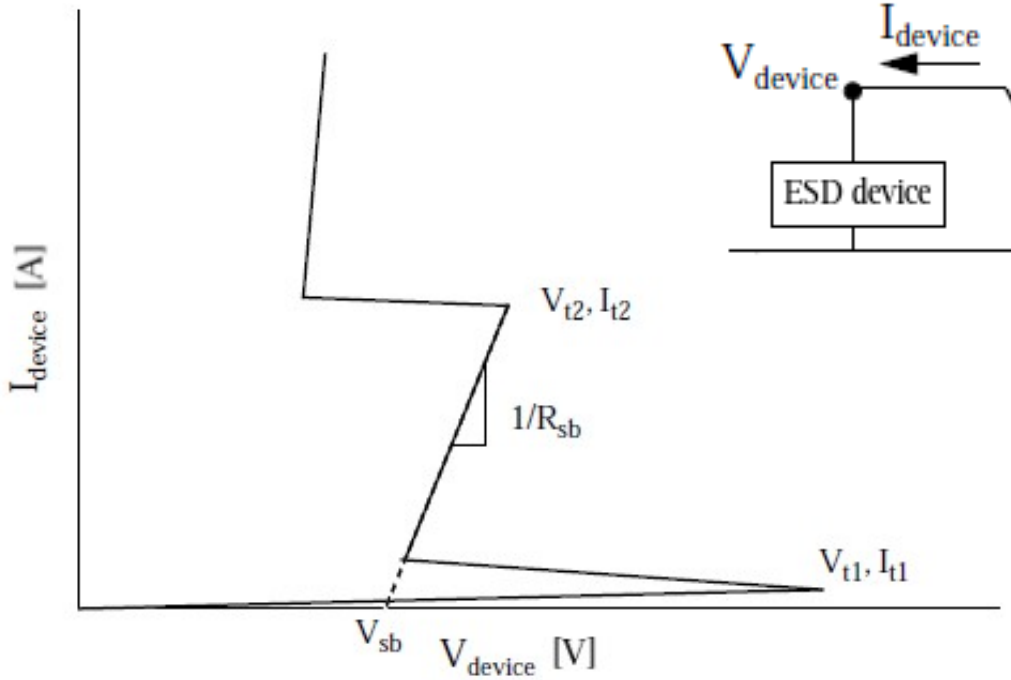
- Providing a *very high impedance* (*) during *normal operating condition* → don't affect circuit performance.

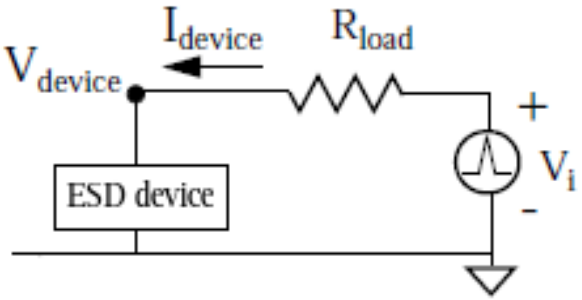
- Clamping input voltage at a safe level - below the dielectric breakdown voltage of gate-oxide.

(*) - ESD device connect to: + the thin gate of input buffer trans → require high impedance input.
+ the drain of output buffer trans → require low impedance output.

2. ESD protection device

Characterizing ESD device: extract I-V (current vs. voltage) curve of ESD device.





V_{t1}, I_{t1} - snapback trigger point

V_{SB} - snapback voltage

R_{SB} - on resistance

V_{t2}, I_{t2} - 2nd breakdown strigger point

I-V curve of NMOS trans under a positive ESD pulse

There 4 main models to do that:

- Human Body Model – HBM
- Machine Model – MM
- Charged Device Model – CDM
- **Transmission Line Pulsing – TLP ← widely accepted model**

(See more detail at Appendix)

Outline

1. Overview of ESD

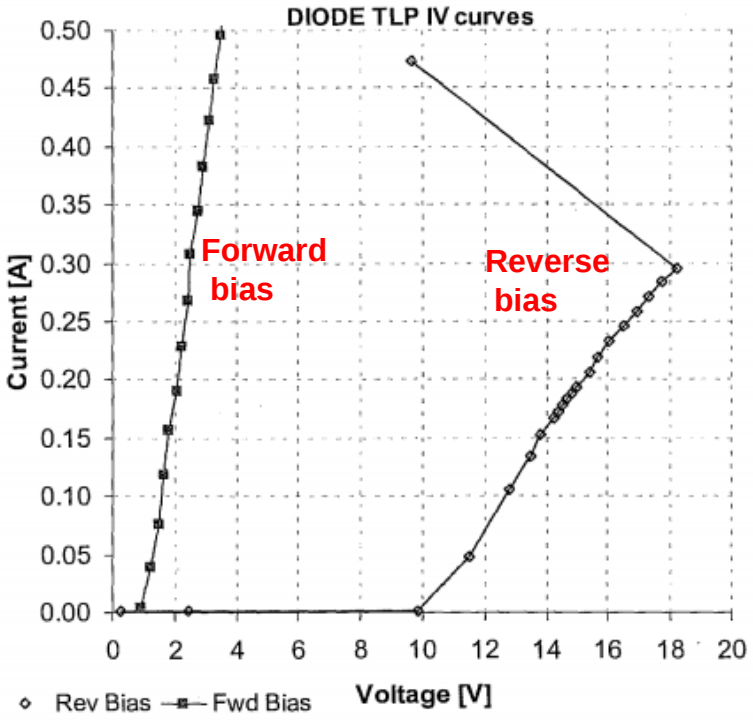
2. ESD protection devices

- 2.1 – Diode
- 2.2 – MOSFET
- 2.3 – Thick Field Oxide device - TFO
- 2.4 – Silicon Controlled Rectifier – SCR

3. Conclusion

2.1 - ESD protection device – Diode (1/2)

- The most simple ESD protection device.
- Formed by N+ diffusion on P-sub ***or*** P+ diffusion on N-well.
- Must be in ***reverse bias***.



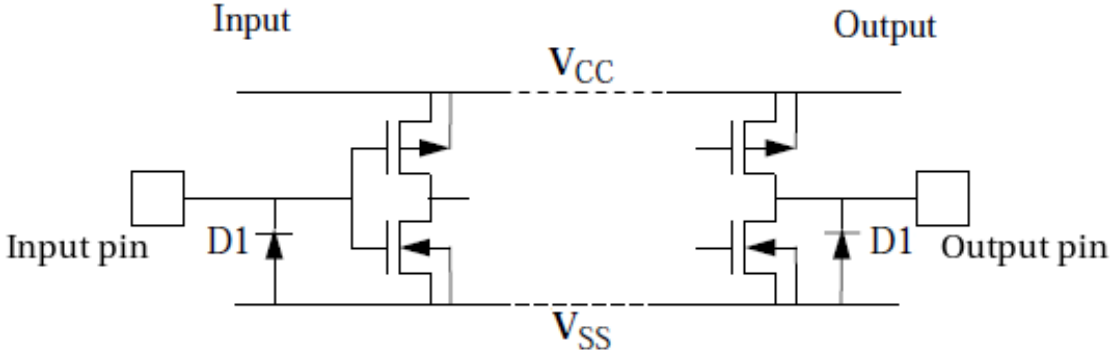
I-V curve (TLP) of a diode

Forward bias:

Clamp voltage: ~ 1V

Reverse bias:

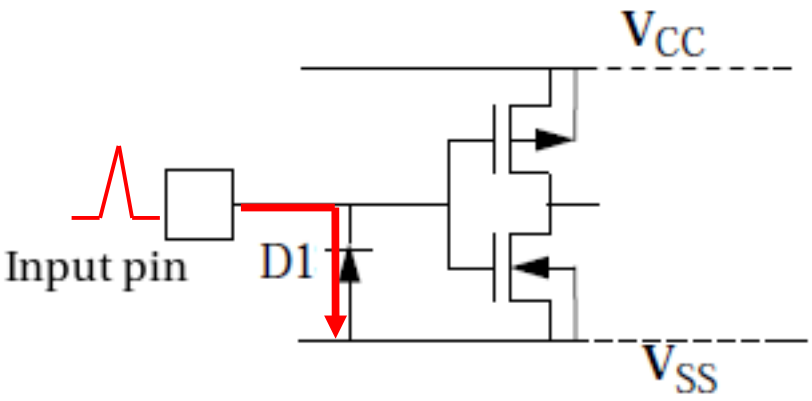
Snapback voltage: ~ 10V



Example of using diode as ESD protection device

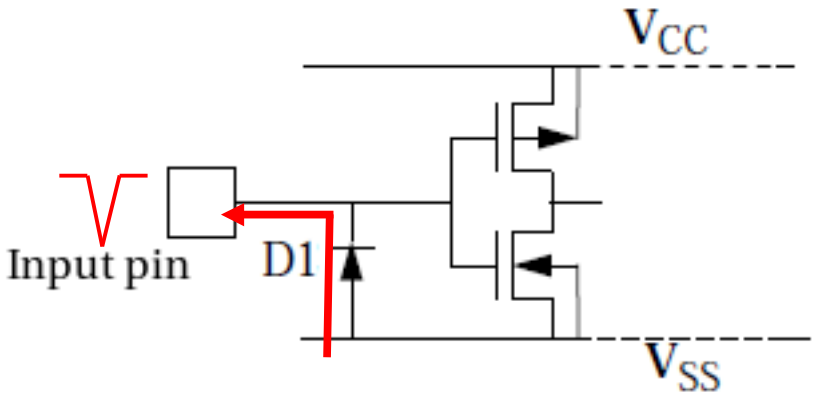
2.1 - ESD protection device - Diode (2/2)

Positive pulse



- Input voltage is clamped at breakdown voltage of D1

Negative pulse



Input voltage is clamped at -0.6V

Advantage:

- Simple to implement.

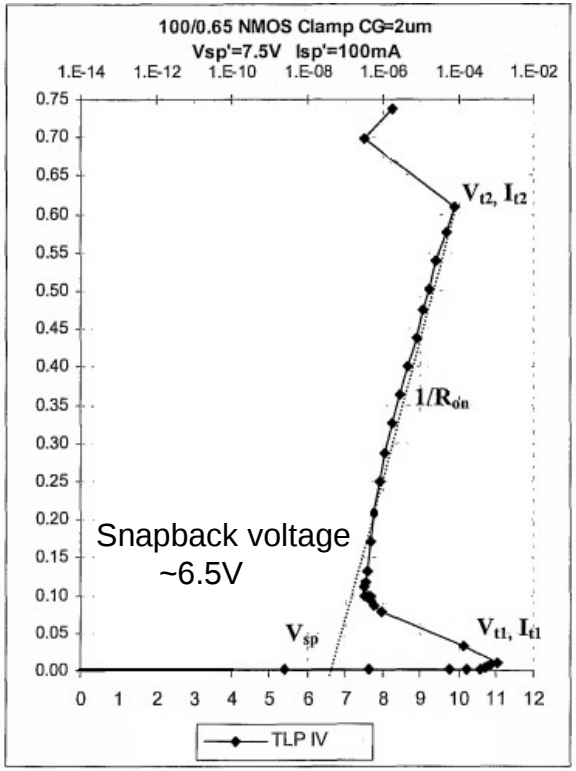
Disadvantage:

- High breakdown voltage
- Cannot breakdown quickly enough to protect a circuit from a fast-rising pulse.

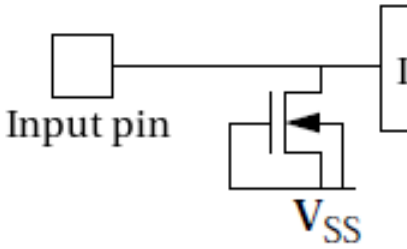
2.2 - ESD protection device – MOSFET (1/3)

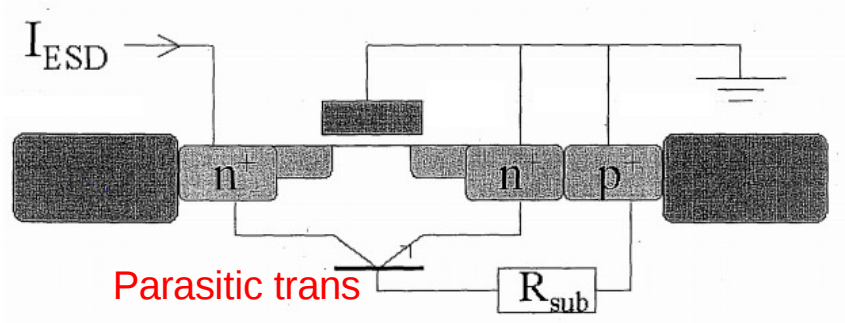
NMOS:

- Drain is connected to input/output terminal.
- Gate & Source are connect to GND → NMOS is ***OFF*** at normal operation.
- When ESD occurs, conduction of parasitic npn bipolar trans will protect internal circuit.



I-V curve of NMOS under positive ESD pulse



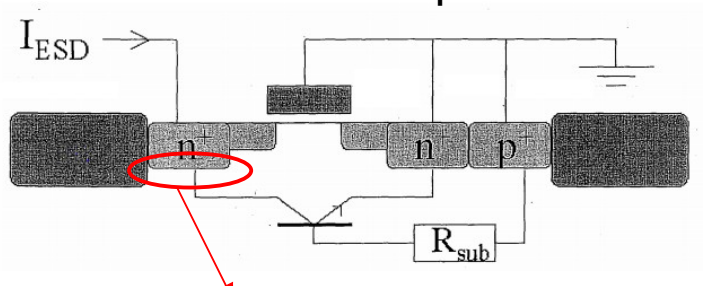


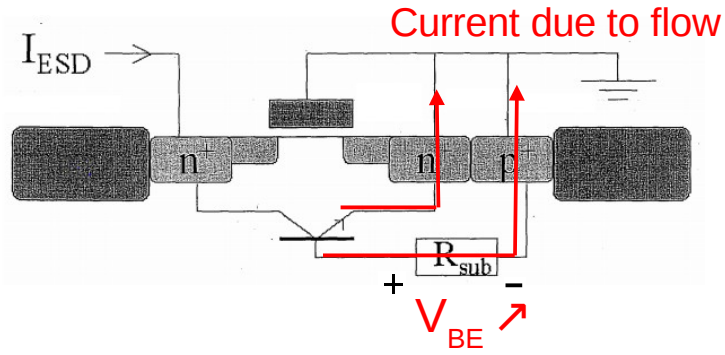
Parasitic resistance of P-sub

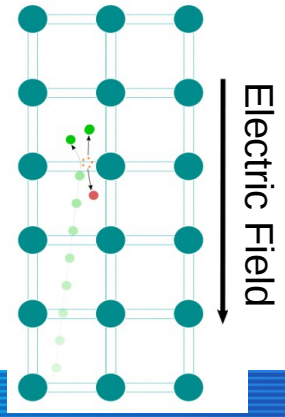
2.2 - ESD protection device – MOSFET (2/3)

- High positive pulse of ESD occurs → drain-substrate junction is broken down due to impact-ionization (*)
- New free holes is attracted to GND though Source and P+ terminal → current flow occurs.
- When V_{BE} > 0.6V, npn transistor turns on
  - → allow large current from collector to emitter of bipolar trans.
  - → drain voltage of MOS is clamped at V_{CE} of bipolar trans.

==> Internal circuit is protected.







(*) impact-ionization: 1 electron (hole) with enough energy can break the electron connection between 2 atoms
→ create 1 pair of free electron-hole

2.2 - ESD protection device – MOSFET (3/3)

Advantage:

- Can be turn-on more quickly (comparing with diode) at a lower voltage by using a gate-bouncing technique *(See detail at Appendix).*

- Using standard chip process without additional implant or masking steps.

Disadvantage:

Become unsuitable with recent technology

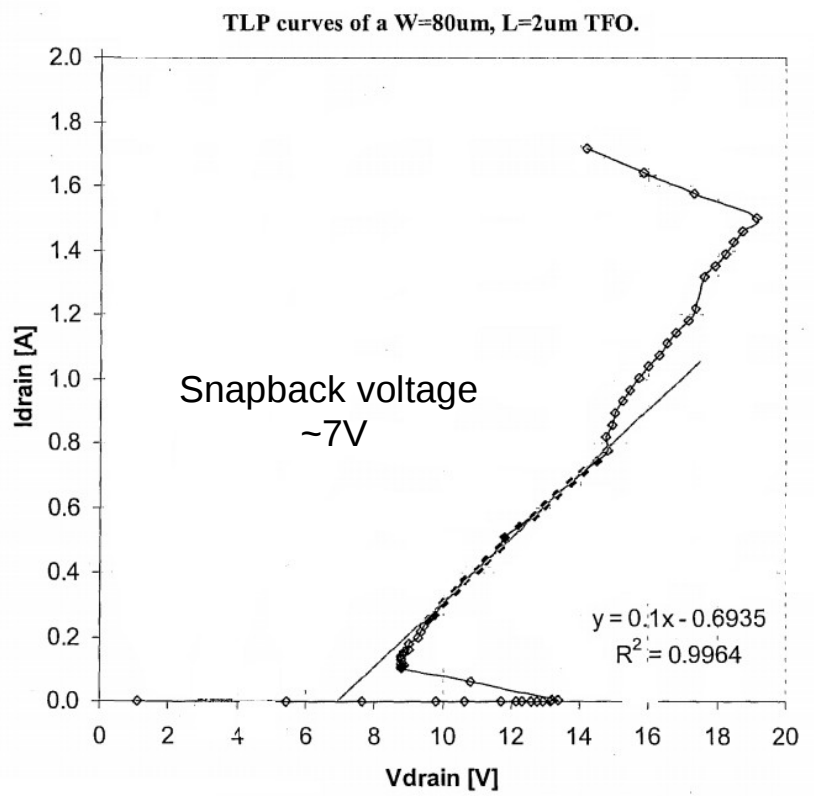
- Because of LDD structure, current drive capability of parasitic lateral BJT is reduced. This causes breakdown voltage higher

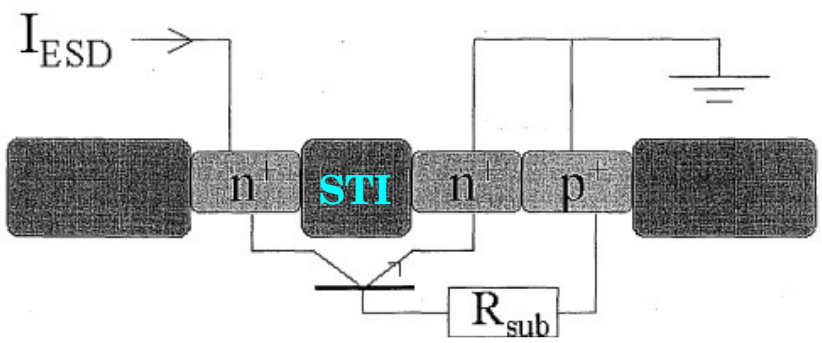
LDD: Lightly Drop Drain

2.3 - ESD protection device – TFO

Thick Field Oxide device – TFO:

- This is very old device structure to prevent ESD (about 1980s).
- Nowadays performance of this device was found to decrease significantly due to new process or techniques (STI, Lightly Doped Drain...).
- In modern process, particularly on high voltage pins, this device is still being used.



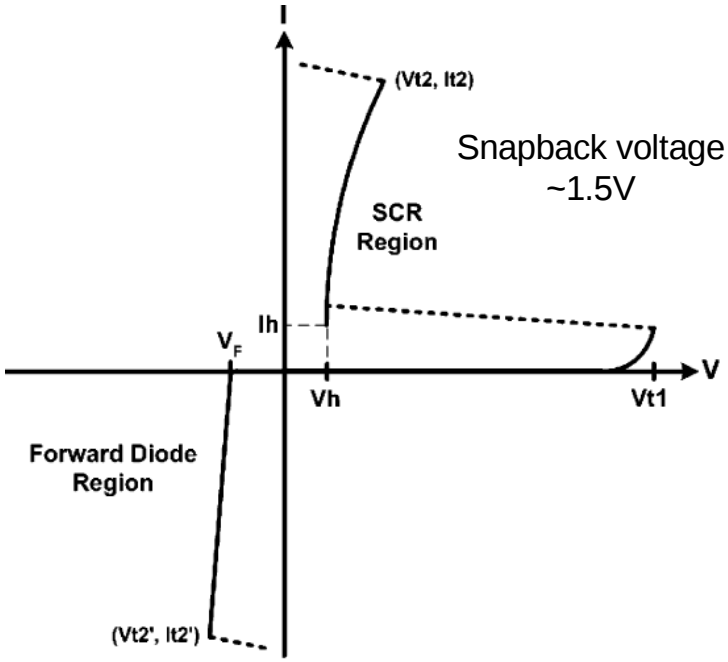


Cross section of Thick Field Oxide device

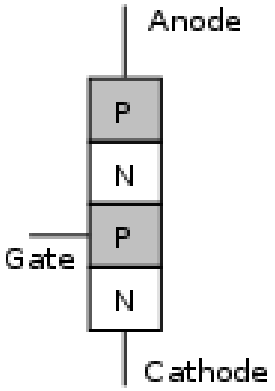
Operation under ESD event is similar to NMOS device.

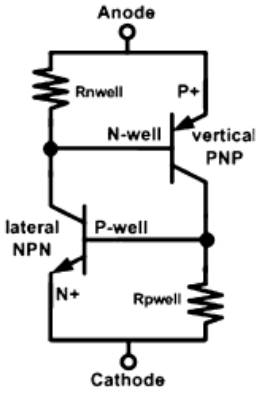
2.3 - ESD protection device – SCR (1/2)

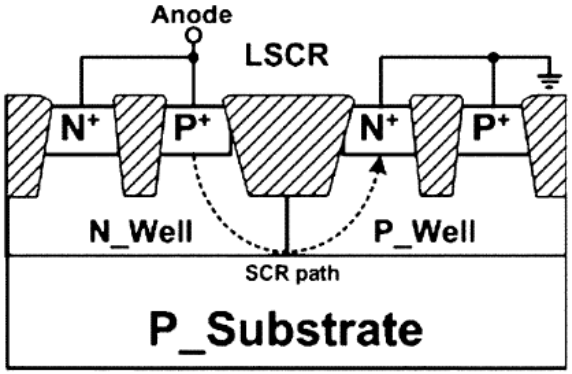
Silicon Controlled Rectifier – SCR:



I-V curve of SRC under positive and negative voltage bias







LSCR: *Lateral SCR*

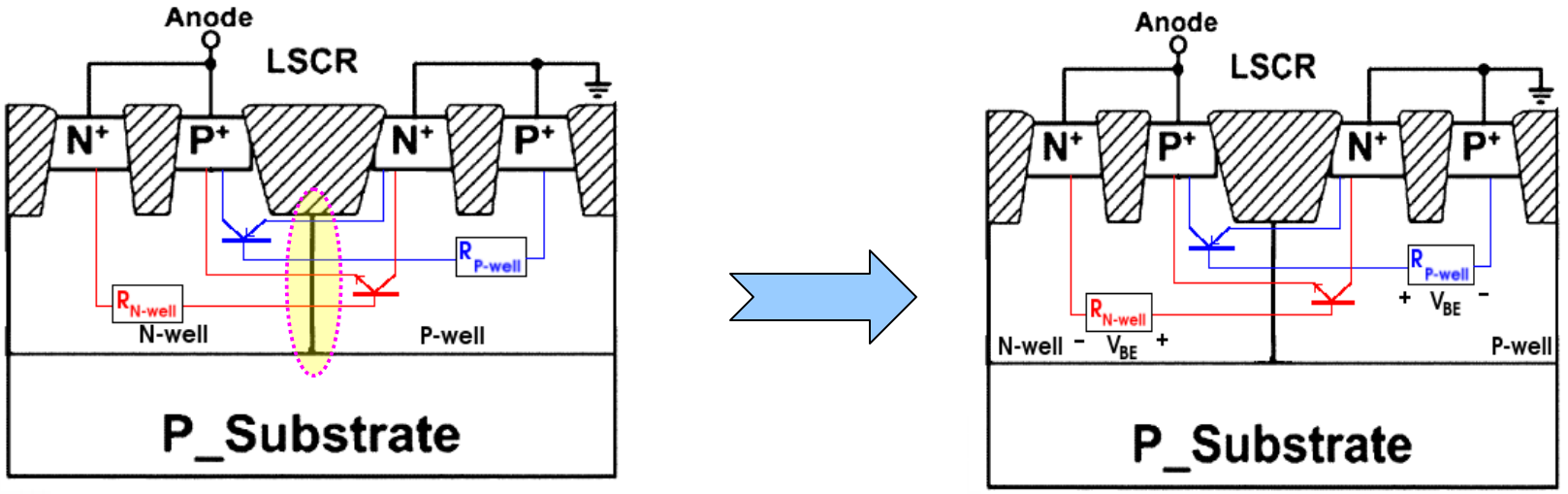
Advantage:

- Low snapback voltage → low power dissipation.
- Can sustain higher level of ESD level within small layout area.

Disadvantage:

- Easy to cause latch-up problem ← can be eliminated *(See Appendix).*

2.3 - ESD protection device – SCR (2/2)



- High voltage applies to junction of Nwell – Pwell.
→ impact-ionization creates more free electron – hole pairs.

- Electrons are attracted to Anode
Holes are attracted to Cathode

- When voltage drops through $R_{P\text{-well}}$ (or $R_{N\text{-well}}$) larger than 0.6V → parasitic pnp (or npn) bipolar transistor is ON.
==> Conduct large current
Clamp voltage between Anode – Cathode at V_{CE} of bipolar transistors.

3 - Conclusion

ESD device	Advantage	Disadvantage
Diode	- Simple to implement.	- High breakdown voltage. - Cannot breakdown quickly.
CMOS	- Can be turn-on quickly. - Simple to implement.	- Hot carrier relaxation (LDD) makes trade-off with ESD.
TFO	- Apply on high voltage pin.	- Performance decreases significantly with current process.
SCR	- Low snapback voltage (low power dissipation) - Sustain higher level of ESD.	- Latch-up problem.

- The protection method explained here are general ones.
- Depending on process technology/device structure, practical measure differs.

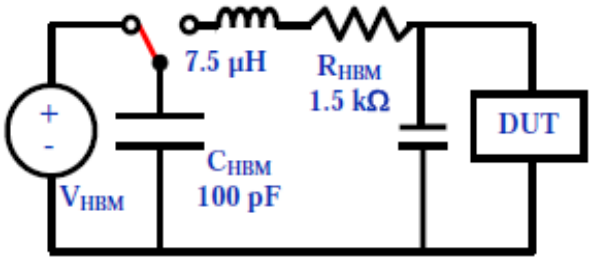
→ So we have to take care of the latest information.

Thank you for your listening

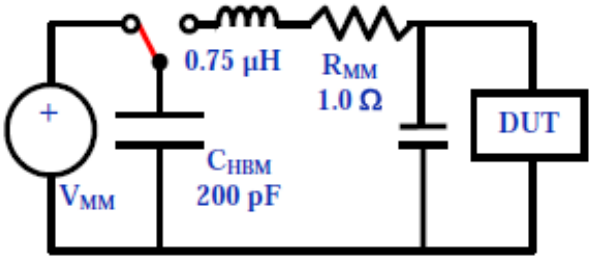
RENESAS

Appendix (1/3)

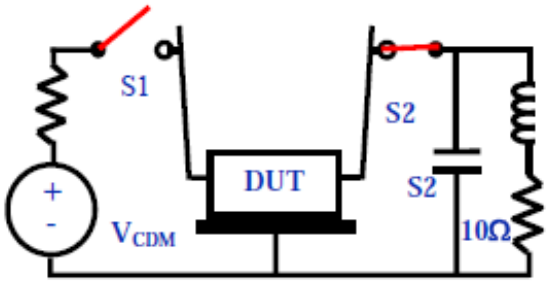
Models used to obtain I-V curve of ESD device



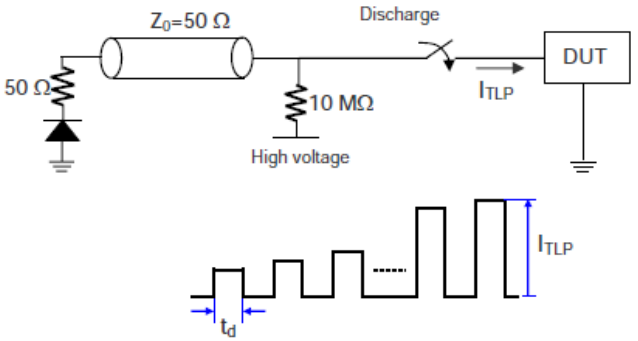
Human Body Model - HBM



Machine Model – MM



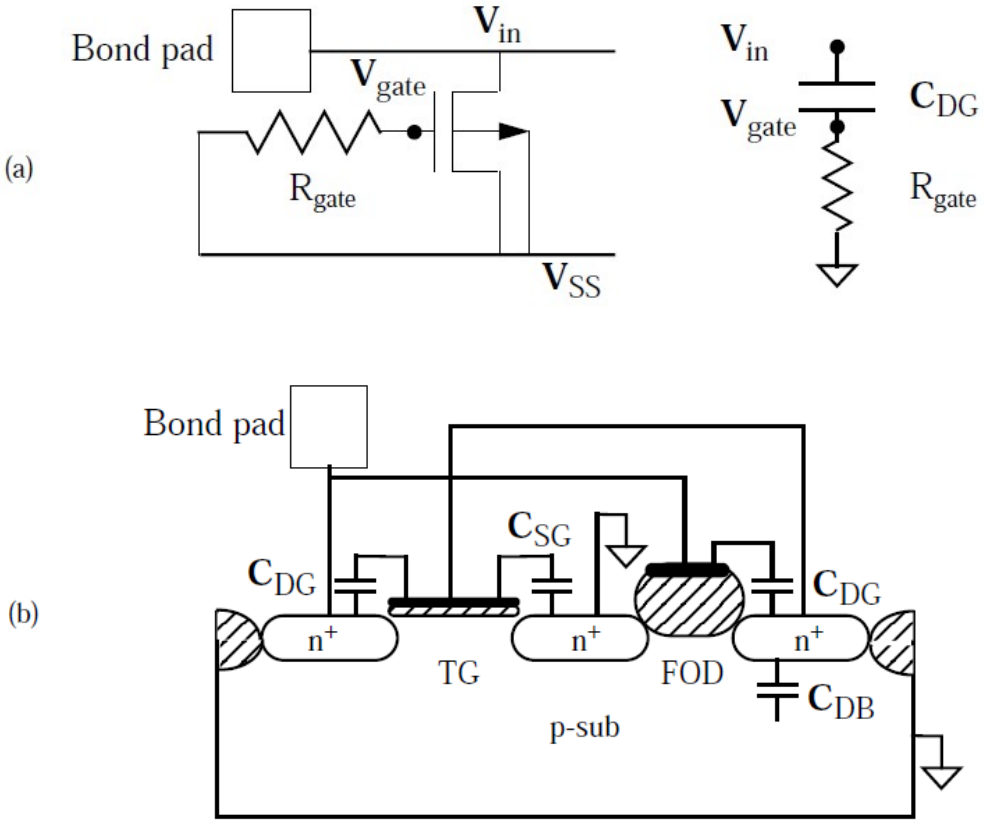
Charged Device Model - CDM



Transmission Line Pulsing - TLP

Appendix (2/3)

Gate-bouncing technique



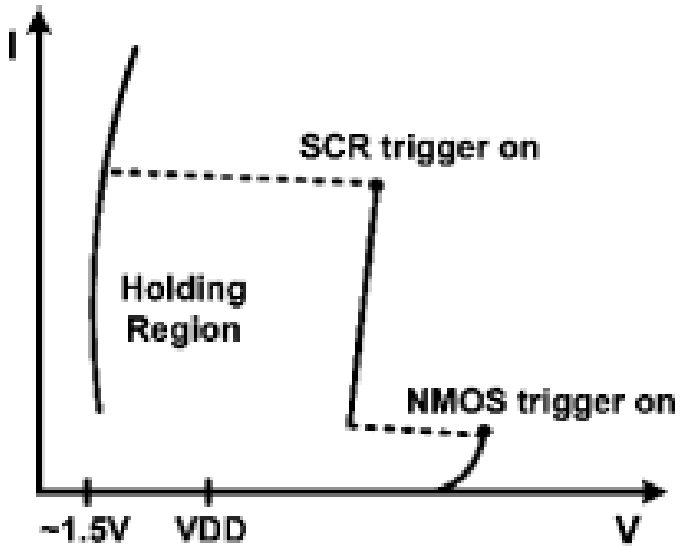
Gate-bouncing techniques: (a) employment of a gate-bounce resistor and equivalent circuit; (b) dynamic gate coupling method.

Appendix (3/3)

Methods to eliminate latch-up problem for SCR ESD device

There are 2 solutions to avoid the SCR with low switching voltage being accidentally triggered on by noise pulse when CMOS ICs are in normal circuit operating condition.

Method 1:
Increasing the triggering current of SCR



Method 2:
Increase holding voltage of SCR to be greater than VDD