Negative bias temperature instability effect

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RENESAS Group CONFIDENTIAL

OUTLINE

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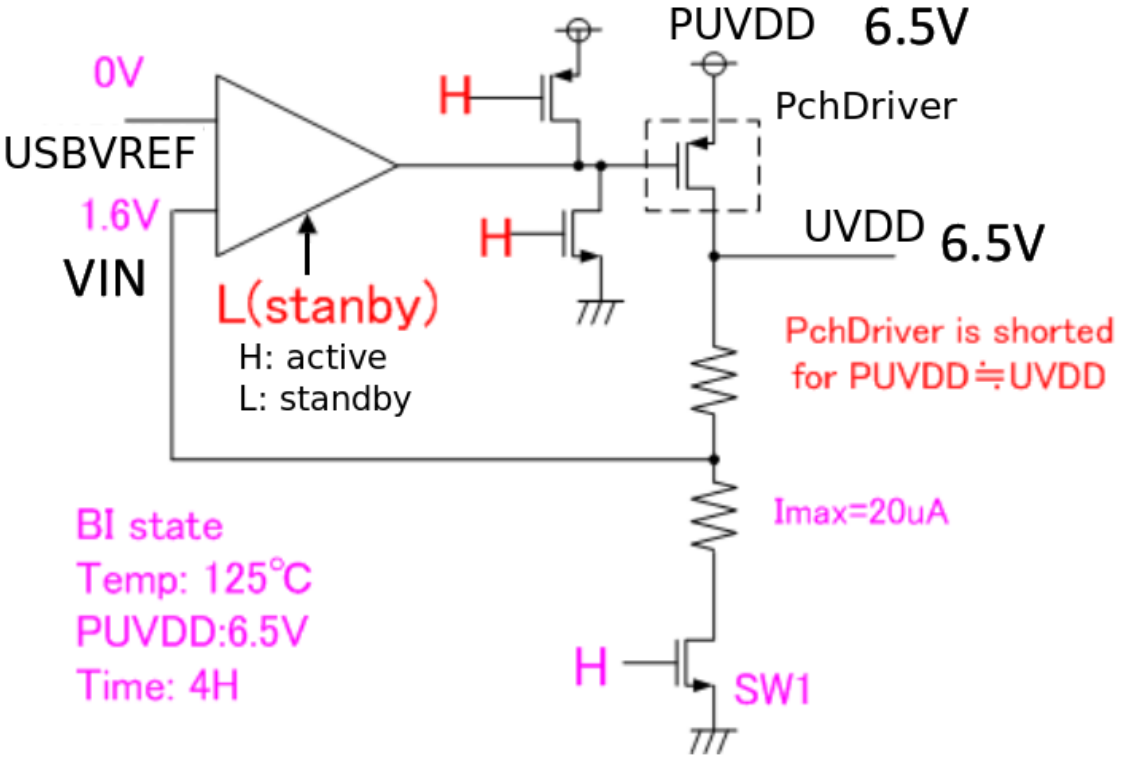
Introduction (1/3)

NBTI issue in USBVDC circuit

Burn In mode:

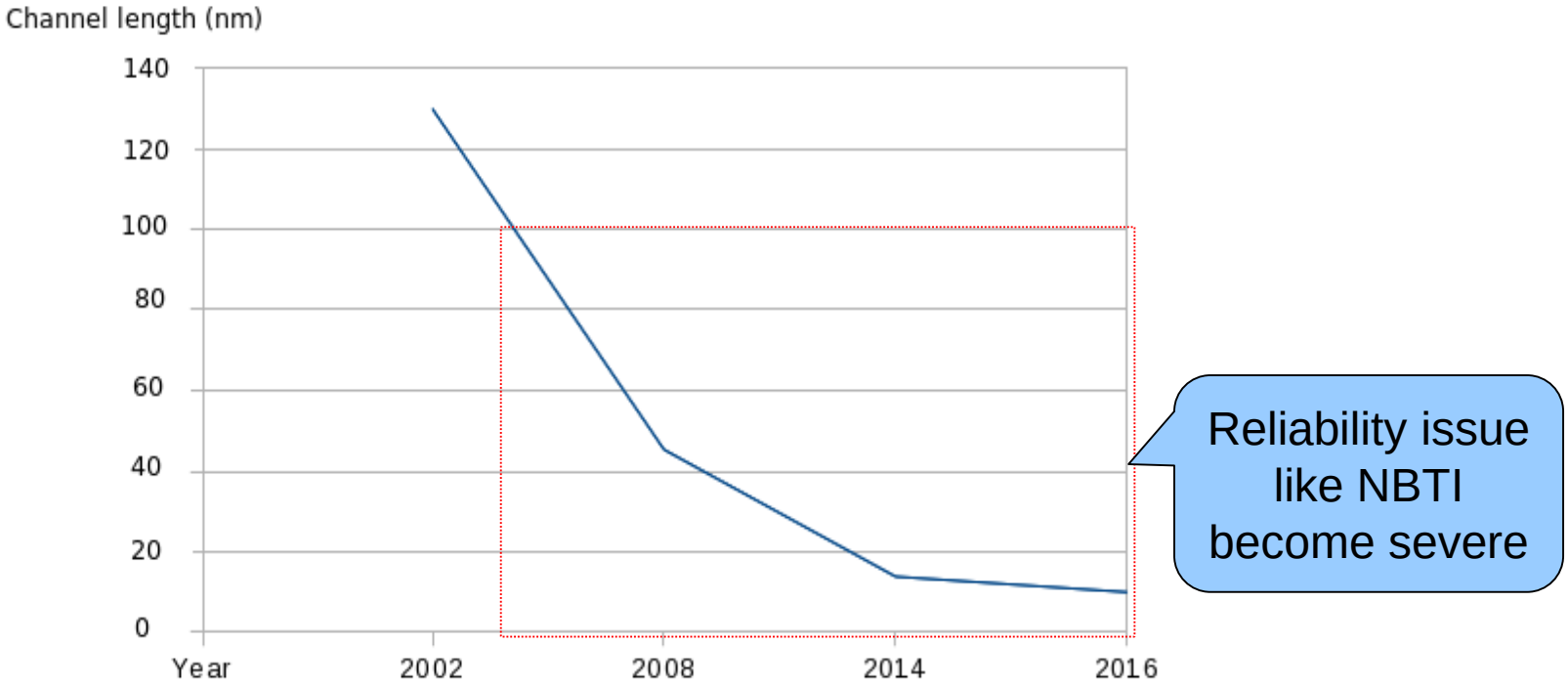


For NBTI, VIN is needed same as USBVREF. But, we do not have same voltage. So, VIN is as low as possible. The problem here is if SW1 is OFF, VIN is 6.5V while USBVREF = 0.

Different **NBTI stress** cause the **mismatch** in Vth of PMOS differential pair in amplifier. Then the circuit performance get worse.

Introduction (2/3)

Challenge of scaling down process



Scaling down CMOS process into 100nm regimes has brought about new reliability challenges in MOSFET device such as hot carrier injection, **Negative Bias Temperature Instability (NBTI),** Time Dependent Dielectric Breakdown TDDB...

NBTI in PMOS gets worse due to **higher operation temperature** and **ultra thin oxide** 10Å (higher oxide field).

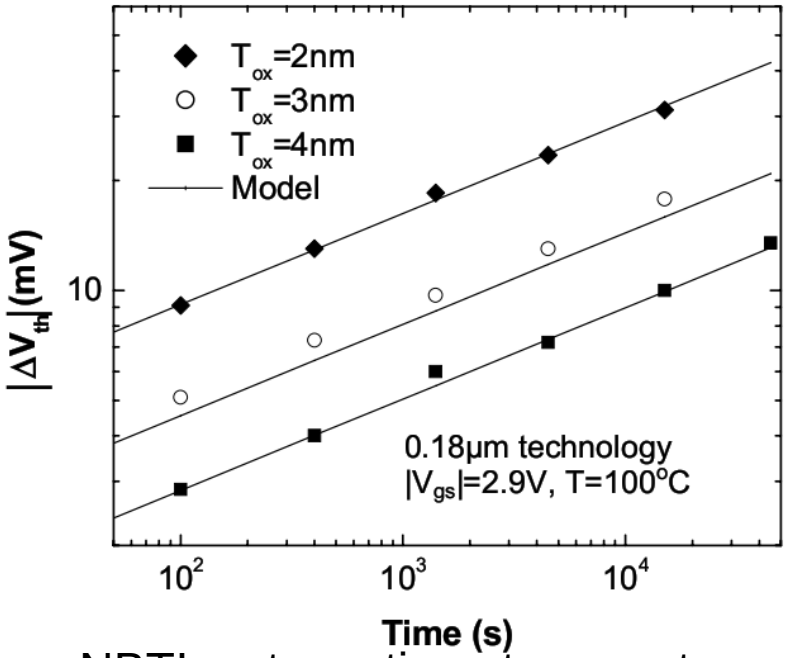
Introduction (3/3)

NBTI reliability issue

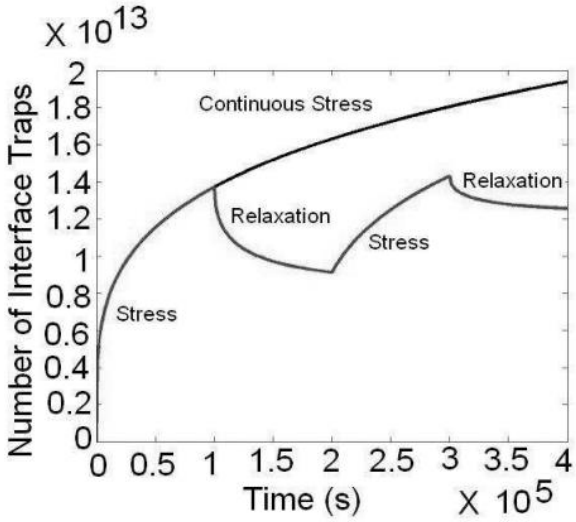
Negative-bias temperature instability (NBTI) is a key reliability issue in MOSFETs. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance of a MOSFET.

Concern in p-channel MOS devices which always operate with negative gate-to-source voltage.

However, same mechanism also affects nMOS transistors when biased in the accumulation regime (w/i negative bias applied to the gate).



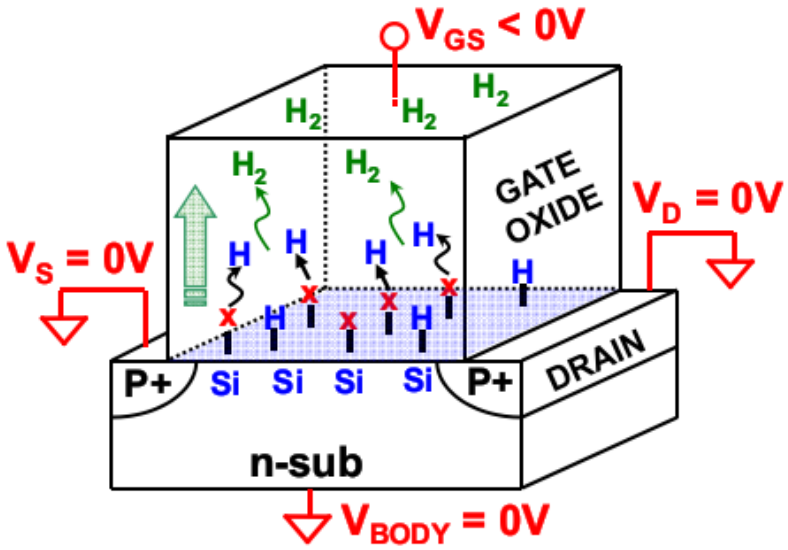
NBTI ~ stress time, temperature (100°C – 250°C), negative bias...

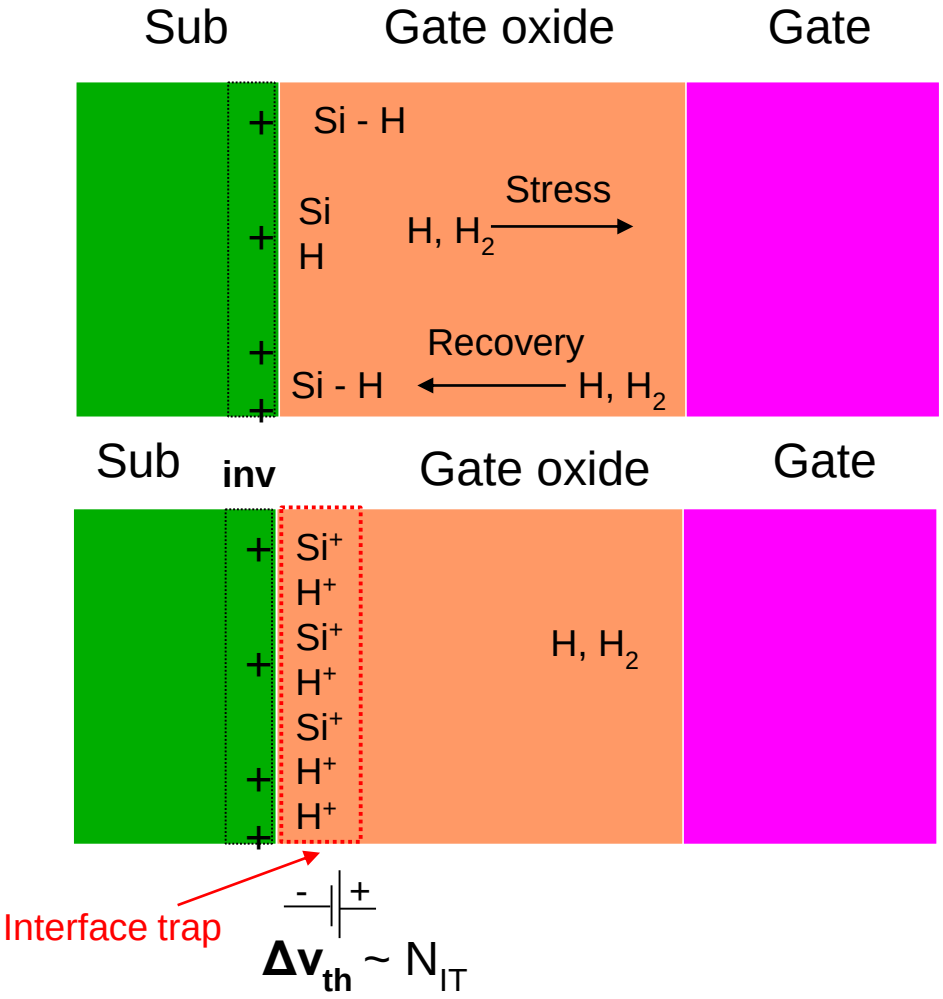


Mechanism (1/2)

$$Si_3 \equiv Si - H + h^+ \leftrightarrow Si_3 \equiv Si^* + H_i^*$$

$$O_3 \equiv Si - H + h^+ \leftrightarrow O_3 \equiv Si^* + H_i$$



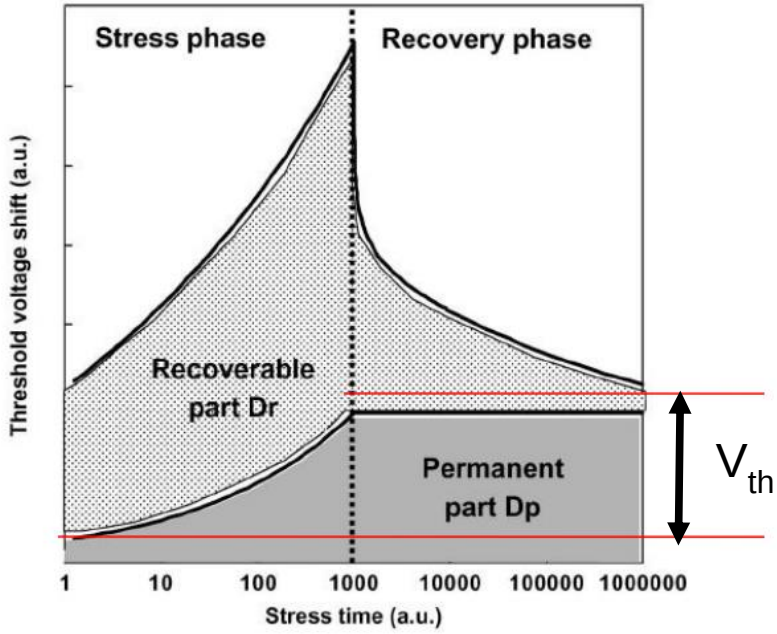


Mechanism (2/2)

NBTI has 2 phases:

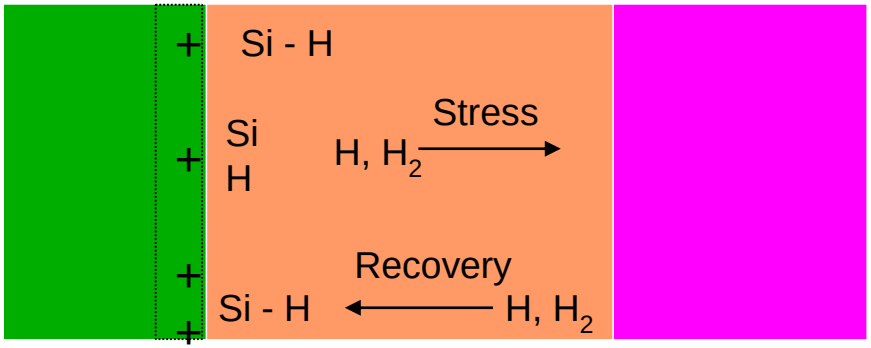
Phase 1: Vg = 0 (Vgs = -VDD), positive interface traps are accumulation over the stress time with H diffusing towards the gate
-> “stress” or “static NBTI”.

Phase 2: Vg = VDD (Vgs = 0), hole are not present in the channel
-> no new interface traps are generated, H diffuse back and anneals the broken Si-H
-> number of interface taps is reduced & NBTI degradation is recovered
-> “recovery”.

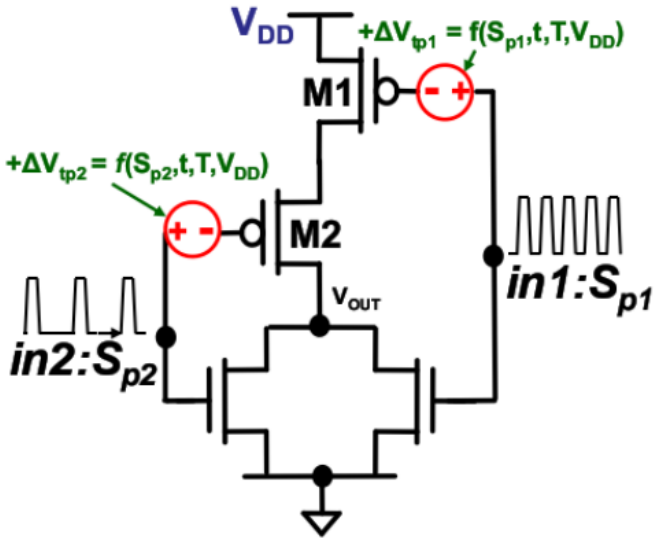


$$\Delta V_{th} = qN_{it}/C_{ox}, \text{ where } C_{ox} = \varepsilon_{ox}/T_{ox}$$

Sub Gate oxide Gate



Modeling



Circuit simulation model:
NBTI represented as voltage source.

Reaction diffusion based model

Reaction

$$\frac{dN_{IT}}{dt} = k_F[N_0 - N_{IT}] - k_R N_{IT} N_H^{(0)} \approx 0$$

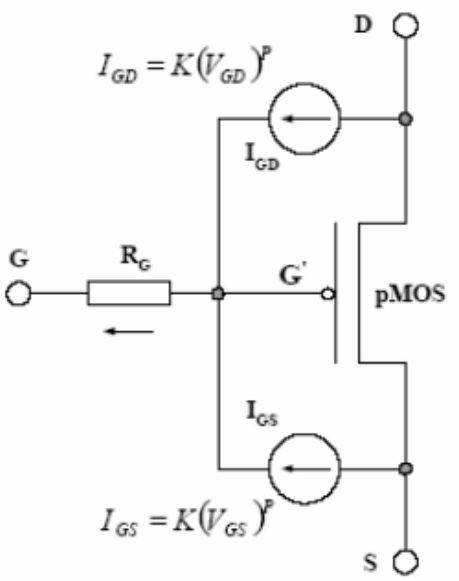
Diffusion

$$N_{IT}(t) = \frac{1}{2} N_{H_2}^{(0)} \cdot \sqrt{D_{H_2} t}$$

H-H_2 Conversion

$$N_{H_2}^{(0)} = k_H \left(N_H^{(0)}\right)^2$$

$$N_{IT}(t) = \left(\frac{k_F N_0}{k_R}\right)^{2/3} \left(2k_H^2 D_{H_2} t\right)^{1/6}$$



MaCRO NBTI circuit model.

Effect

Threshold voltage increase

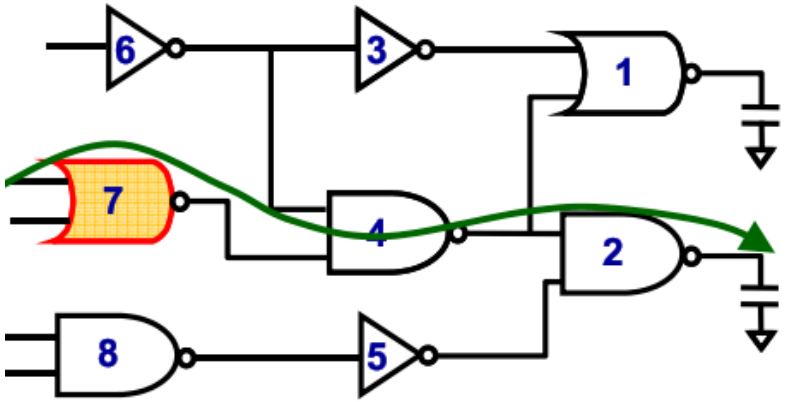
-> Drive current decrease

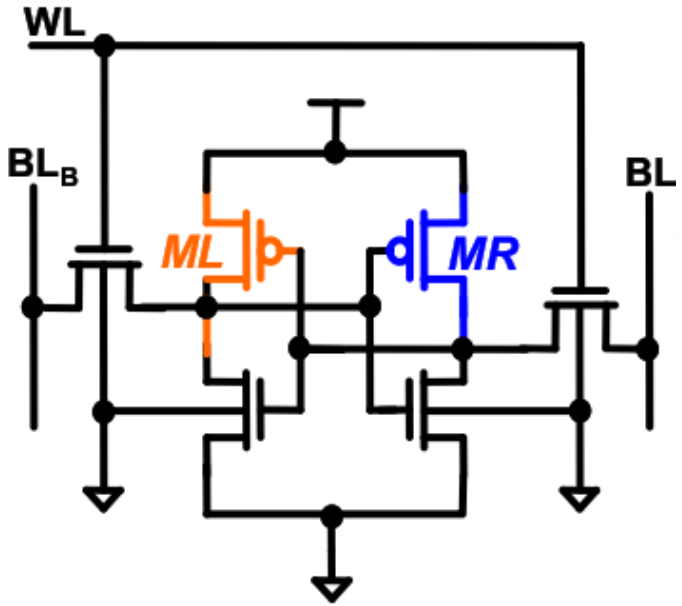
-> Delay increase.

-> Failure/error in Memory,
CPU operation.

Threshold voltage change differently

-> Effect matching property
(pair MOS).





Countermeasure

Power:

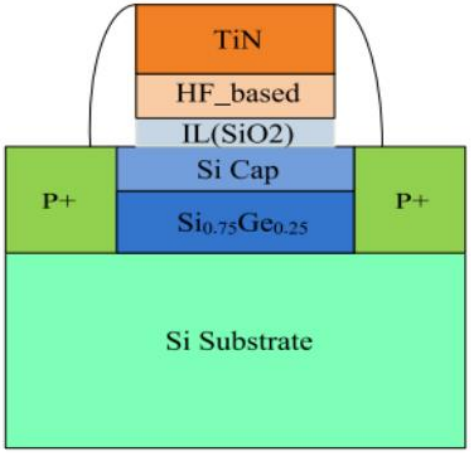
Power gating, Input vector control (duty cycle)...

Circuit design:

Sense & Correction, Gate/TR sizing...

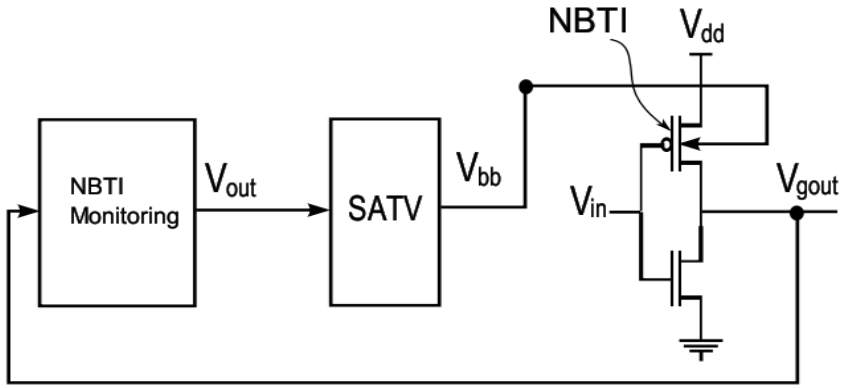
Others:

Improve MOSFET structure...

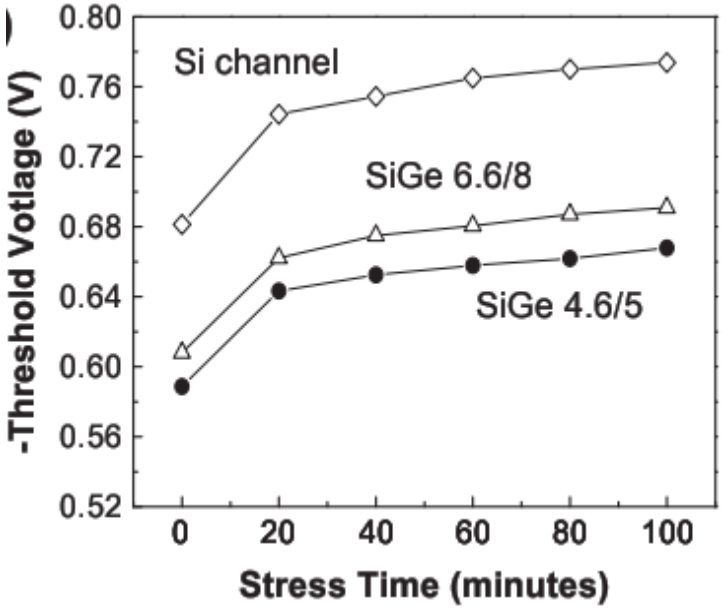


Schematic of HfO_2 metal gate SiGe pMOSFET.

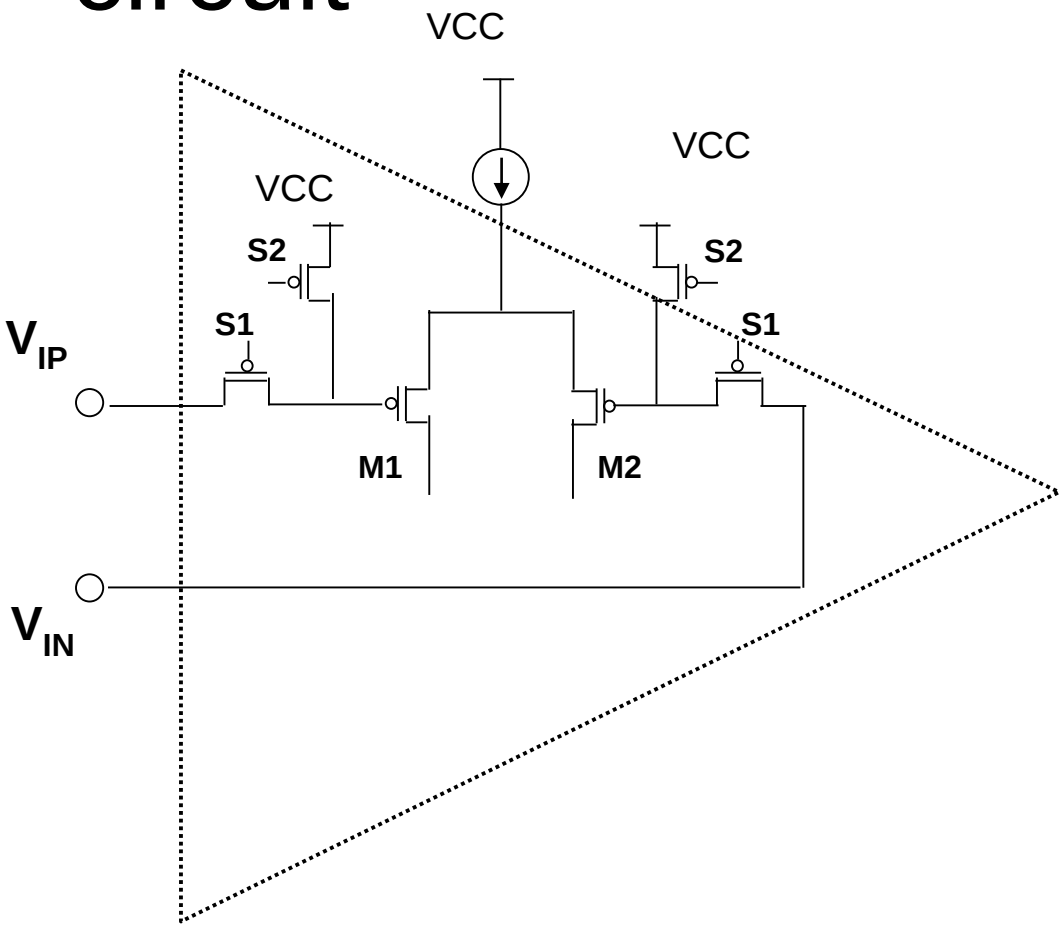
Self Adjusting Threshold Voltage



$$V_{TB} = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\varphi_B} - \sqrt{2\varphi_B}\right)$$



NBTI consideration for analog circuit



+ Normal operation : $V_{IP} = V_{IN}$
S1: L
S2: H
→ switches have influence ON circuit operation.

+ Standby operation:
S1: H
S2: L
→ Gate of M1 & M2 = VCC.
→ $Vgs_{M1} = Vgs_{M2} = 0$
→ can avoid mismatch degradation due to NBTI.

Thank you

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Burn In

Burn-in is the process by which components of a system are **exercised prior** to being placed in **service** (and often, prior to the system being completely assembled from those components).

The intention is to **detect** those particular components that would **fail** as a result of the initial, high-failure rate portion of the bathtub curve of component reliability.

For electronic components, burn-in is frequently conducted at **elevated temperature** and perhaps **elevated voltage**.

Threshold voltage

The threshold voltage Vth is the value of the gate–source voltage when the conducting channel just begins to connect the source and drain contacts of the transistor, allowing significant current.