Short presentation

ANTENNA EFFECTS

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PRESENTATION OUTLINE

I/ Mechanism of antenna condition

I.1) Define “antenna”

I.2) Describe plasma charging damage (PID)

II/ Evolution of the definition of the Antenna Ratio

III/ Design solutions to reduce Antenna effects

III.1) Description of each solution

III.2) Comparison of solutions

III.3) Antenna Rules

IV/ Practical IP Layout Consideration

I/ Mechanism of antenna condition

I.1) Plasma Induced Damage (PID) – Antenna Effect

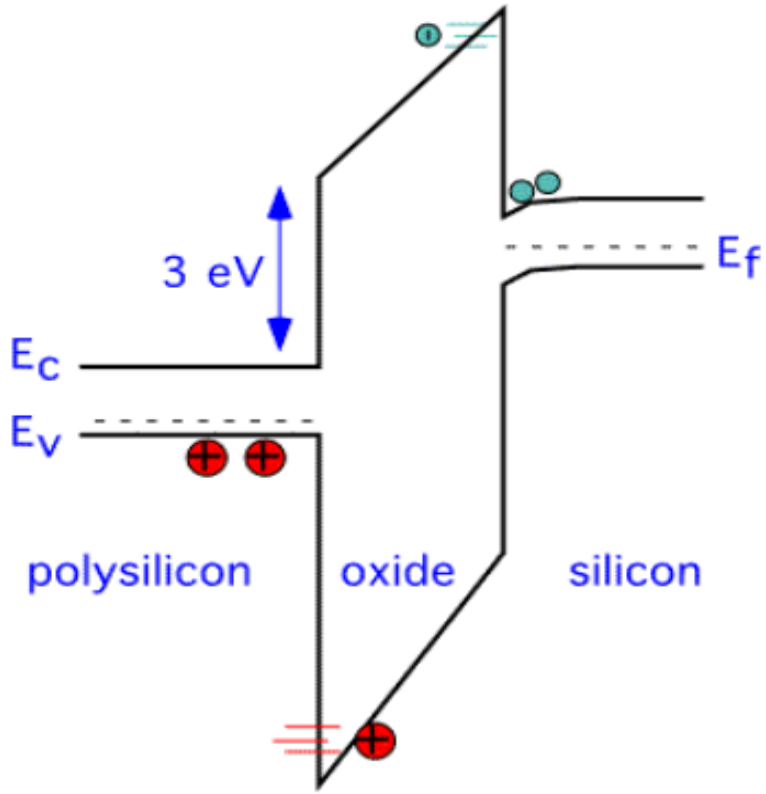
. Occur during manufacturing process

. Antenna are floating conduction layers without shielding layers of oxide – effect poly and metal layers

. The random discharge of the floating node could permanently damage the transistor

I.2) Describe plasma charging damage

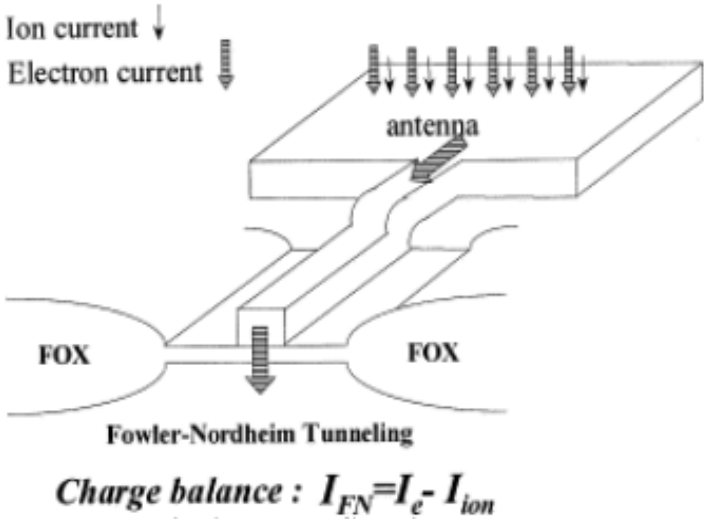
. Oxide tunneling current (F-N) introduces more trap states
. e- tunnel through the oxide-semiconductor barrier
. e- gather energy and do damage (break bonds) as they proceed – Due to high electric fields
. Affects gate oxide breakdown and Transistor threshold voltages
. Defects enhance this effect
. Mechanism is not well understood



The stress voltage that develops across the gate and substrate of a MOSFET during plasma processing basically comes from three sources.

- Non uniform distribution of plasma potential across the wafer.
- Charging filtering (shading) due to microscopic topography on the wafe
- AC effects due to the nature of RF discharge that sustain the plasma.

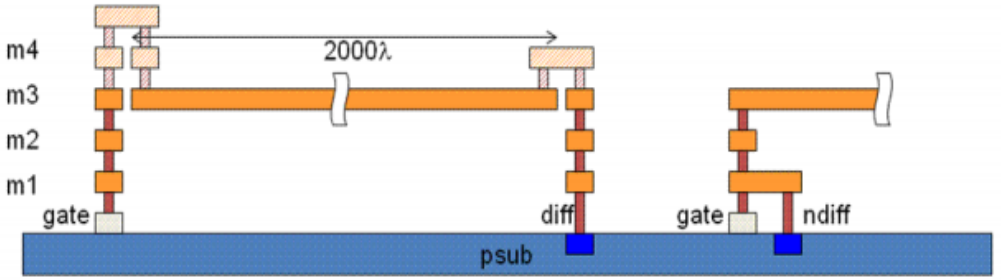
  (quite small in all cases --> negligible)



The size of the conductor exposed to the plasma plays a role in determining the magnitude of the net charge collection rate and therefore the tunneling current. This is the so called “antenna effect”.

Simplification:

- Charge builds up (DC) on the metal wires (antenna) during the application of the plasma etch
- Because the gate of a MOSFET is like a capacitor
- If the potential on the gate reaches a certain value it will ‘break down’
- ‘Punch through’ occurs
- The gate is damaged irreparably



Charge Build up is affected by:

- Diffusion path
  - There is an NP diode to substrate at the drain/source of any output pin
  - During plasma-etch this diode is reverse biased and at high temp
  - This causes the diode to behave like a resistor
- Gate Area
  - Larger gate_area == larger gate ‘capacitor’
  - At fixed ‘charge’, voltage potential reduces as cap size increases
  - Reducing the voltage prevents ‘punch through’
- Diffusion Area
  - Bigger diffusion == Smaller resistor
  - Smaller R allows more current to pass
- Wire length
  - Longer wires act as antennas to ‘pick up’ more charge

II/ Antenna ratio

Classical definition of antenna ratio (AR)

.To avoid antenna problems, you must design all net topologies so that no gate is vulnerable to a large amount of floating charge.

.This ratio indirectly states how much floating charge a transistor gate can handle by specifying how much wire can be connected to the input of the logic gate before antenna problems occur.

$$AR = \frac{Total\ Exposed\ Floating\ Conductor\ Area\ and\ Perimeter}{Total\ Gate\ Area}$$

The antenna ratio, in a rough sense, is a current multiplier that amplifie tunneling current density across the gate-oxide. For a given antenna ra larger tunneling current is supported when the plasma density is higher. H tunneling current means higher damage.

New Model of Antenna Effect

- Etch time factor needs to be taken into account

$$AR = \frac{Q}{A_{gate}} \quad [14]$$

-Q is the total accumulated injected charge into the gate oxide during the etching time

- Better predictor of antenna effect:

$$v_g = v_{g\,\max} + \frac{\alpha J}{c}\frac{2\pi}{\omega}\frac{(P + p)}{(A + \alpha a)} \quad [11]$$

-**A** is the area of the conducting layer with capacitance **C** exposed to plasma of current density **J**
-**a** is the area of the gate with capacitance a exposed to plasma of current density **j**
-**α** is the capacitance ratio
-**P** is the perimeter of the antenna capacitor
-**p** is the perimeter of the gate capacitor
-***w*** is the angular frequency of the plasma power source

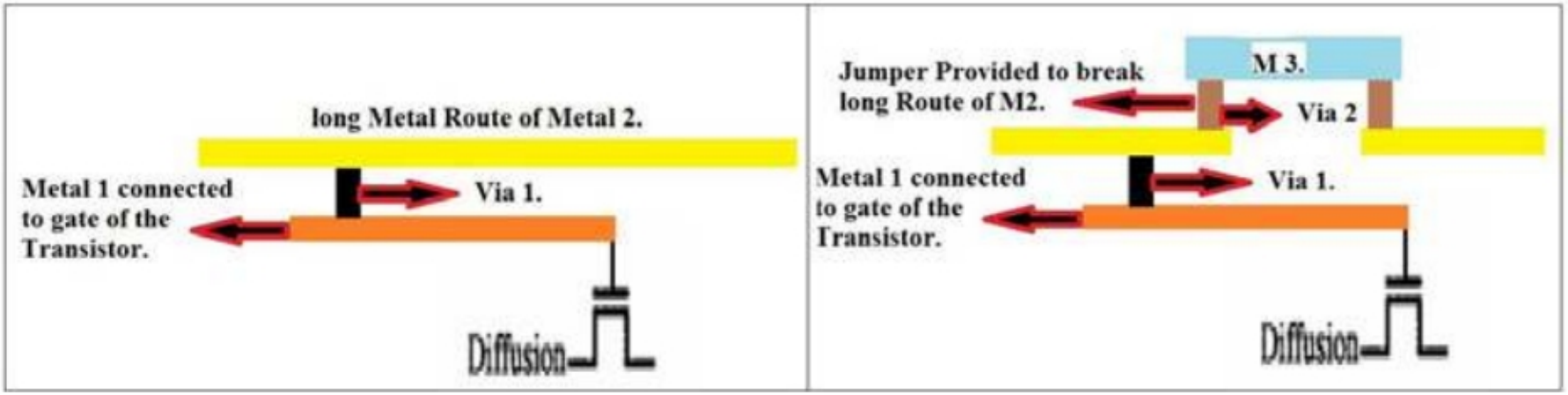
III/ Design Solution to reduce Antenna Effects

- Router options
  - Break signal wires and route to upper metal layers by jumper insertion
  - All metal being etched is not connected to a gate until the last metal layer is etched.
- Dummy transistors
  - Addition of extra gates will reduce the capacitance ratio.
  - PFETs more susceptible than NFETs
  - Problem of reverse Antenna Effects.
- Embedded Protection Diode
  - Connect reverse biased diodes to the gate of transistor (during normal circuit operation, the diode does not affect functionality).
- Diode insertion after placement and route
  - Connect diodes only to those layers with antenna violations.
  - One diode can be used to protect all input ports that are connected to the same output ports.

Most important methods are jumper insertion and diode insertion to remove antenna violation. Jumper techniques are the most effective method of avoiding antenna-effect problems. Diode insertion can repair the remaining antenna problems. However, it is costly in terms of cell area size and it complicates the netlist verification process.

Jumper Insertion

A jumper is a forced layer change from one metal layer to another, and then back to the same layer. Jumper insertion breaks up a long wire so that the wire connected to the gate input is shorter and less capable of collecting charge, as shown in Figure.

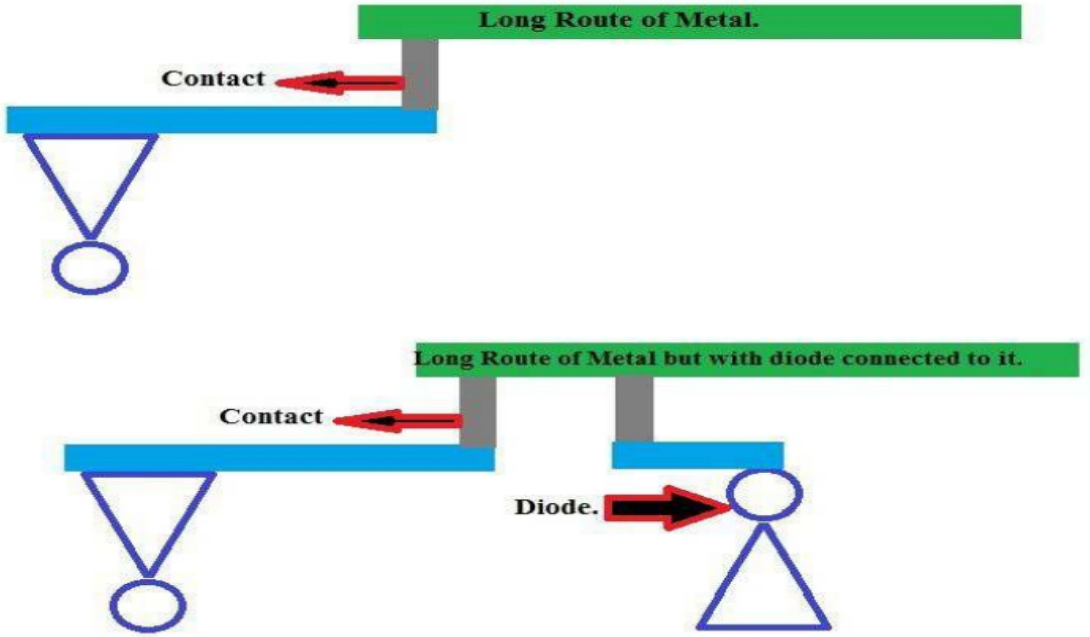


Jumper insertion breaks up a long wire so that the wire connected to the gate input is shorter and less capable of collecting charge.

.The advantage of jumper insertion is that it is fully controlled by the routing tool.

.The disadvantage is that it can potentially contribute to routing congestion problems in upper metal layers

Diode Insertion

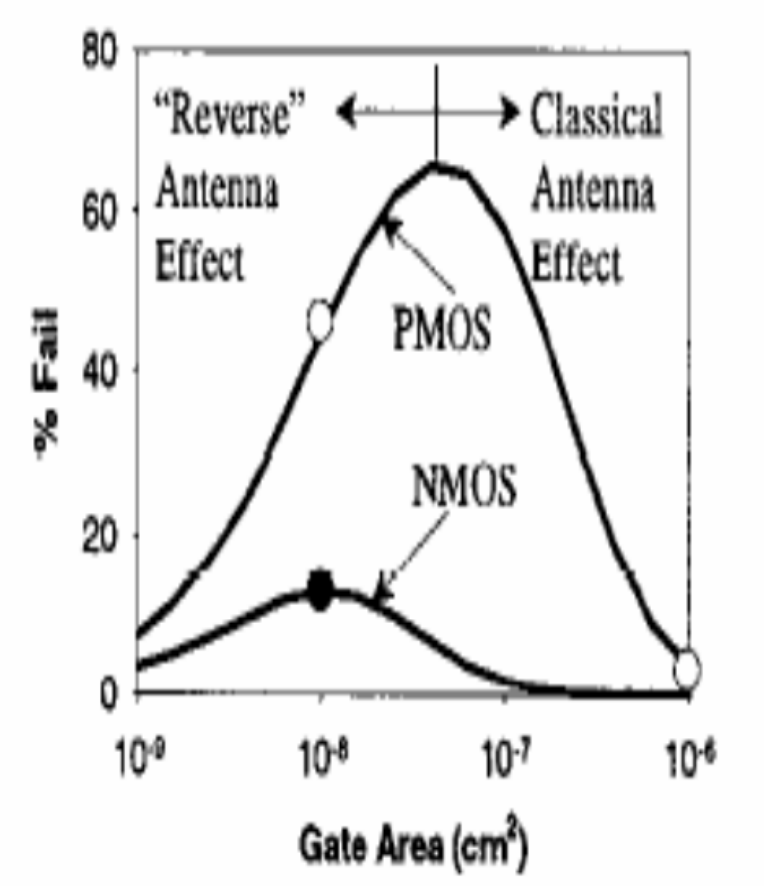


- As shown in Figure, diode insertion near a logic gate input pin on a net provides a discharge path to the substrate so that built-up charges cannot damage the transistor gate.
- Unfortunately, diode insertion increases cell area and slows timing due to the increase of logic gate input load. Moreover, diode insertion is not feasible in regions with very high placement utilization.

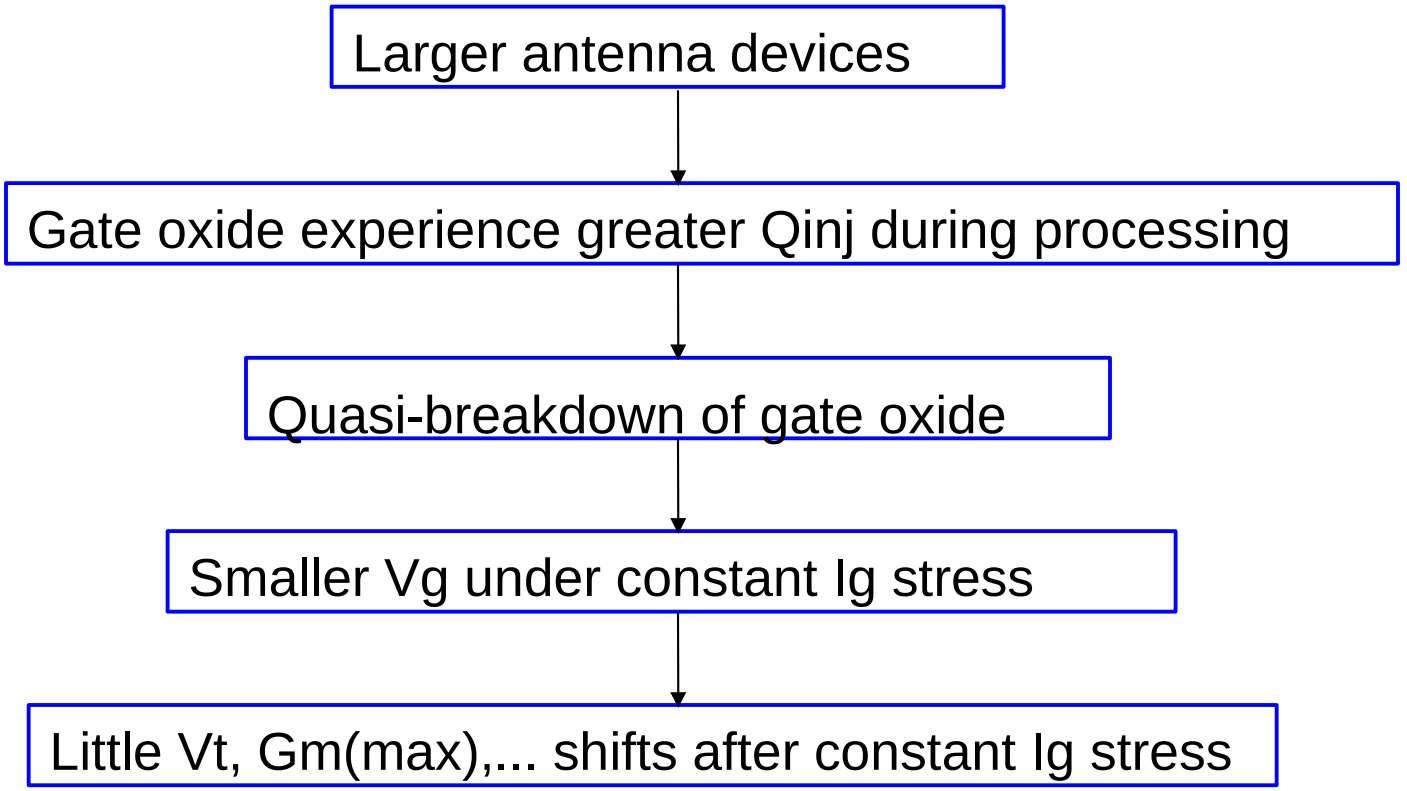
Design Solutions to Reduce Antenna Effect (cont.)

Dummy transistors

- Addition of extra gates will reduce the capacitance ratio
- Problem of “Reverse “ Antenna Effect [5]
- PFETs more susceptible than NFETs

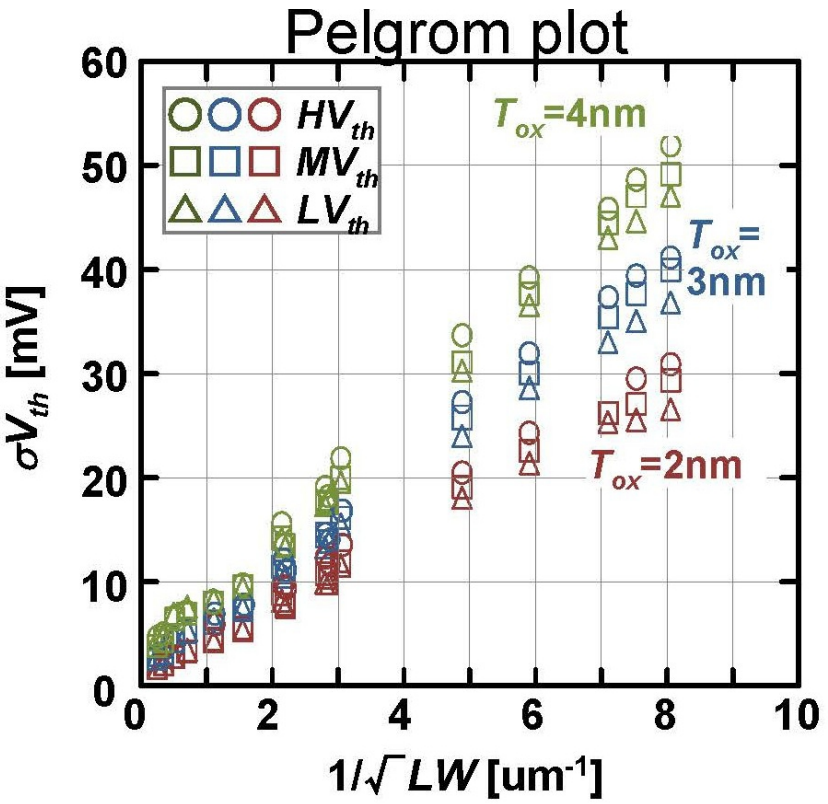


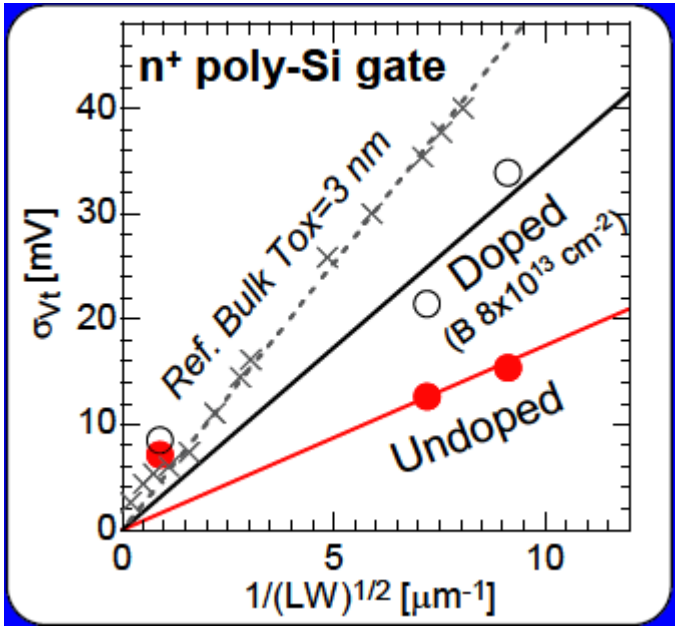
Reverse Antenna Effect



-Simplified explanation about reverse antenna effect -

Pelgrom Plot





>> Pelgrom coefficient is more sensitive when channel width and channel length are smaller --> dummy transistors need to be added in these cases to reduce capacitance ratio

Antenna Rules

In most cases, antenna rules are in the form of:
(antenna-area) / (gate-area) < (max-antenna-ratio)

- Gate-area
  - Boolean AND of the ‘poly’ and the ‘diffusion’ layers
  - Recognized as gate area of the transistors by essentially all foundrie
- Antenna-area
  - Amount of metal area attached to the input pin
  - Calculation method varies for different processes
- Max-antenna-ratio
  - Represents max allowed ratio of antenna area to gate area
  - Calculation method varies for different processes
- There are 2 ways to calculate antenna area:
  - Side-Wall Area = (W + L) * 2 * Thickness
  - Polygon Area = W * L

Practical IP Layout Consideration
- Antenna Effect -

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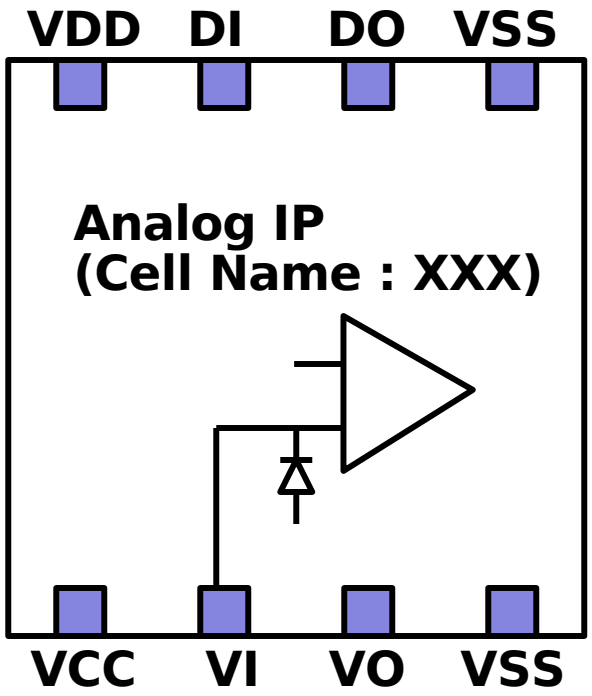
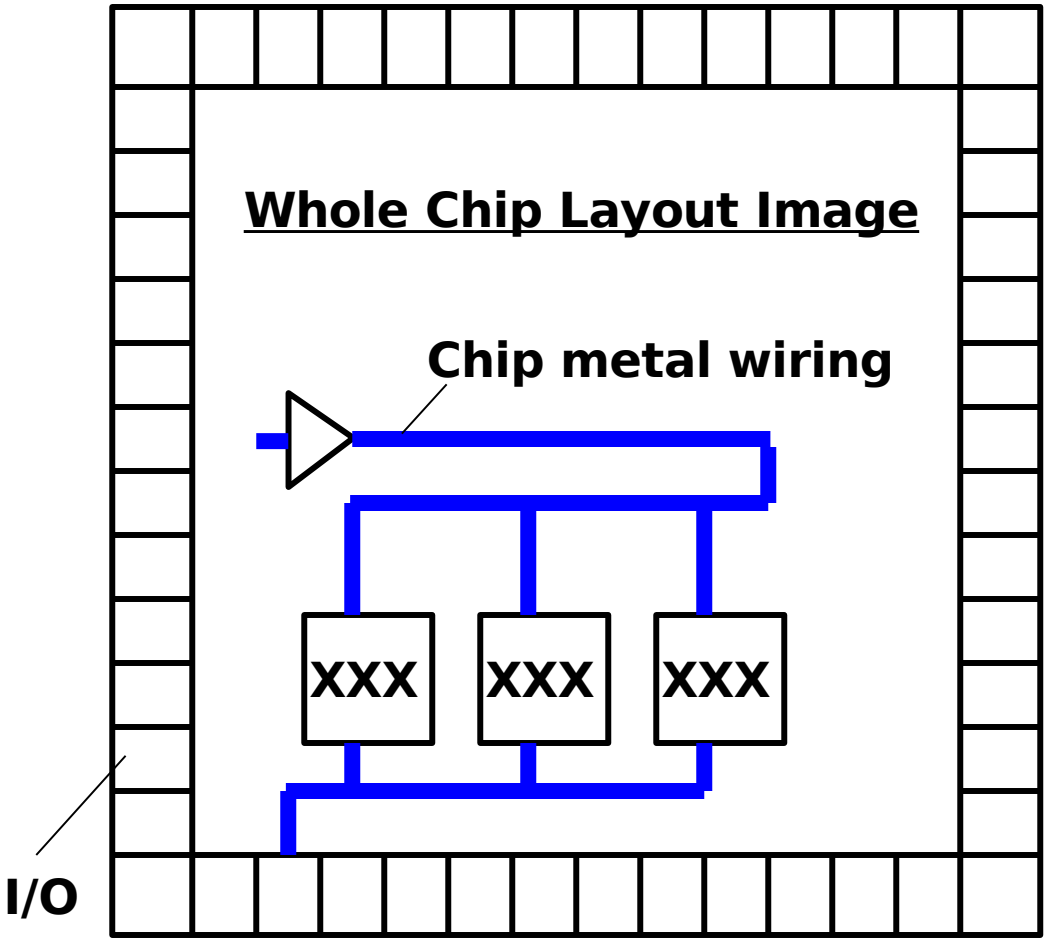
Issue at Whole Chip Layout

- IP designer always release GDS : Antenna DRC clean.
- However, sometimes send back occur from whole chip layout.
- Antenna ratio may exceed spec because of chip wiring.

➔ How to prevent ?

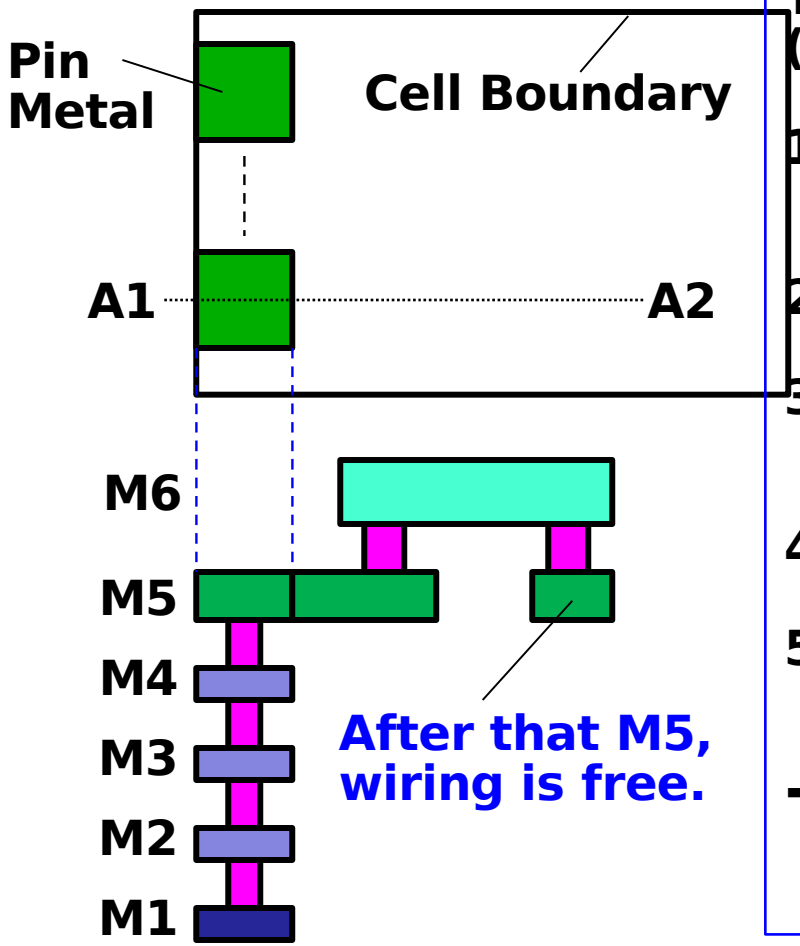


IP Layout TOP view



Solution for IP Layout

Fig-1. IP Layout TOP view



There is a solution around IP pins.
(* Mainly for signal pins)

1/ Provide as many layers as possible
(For flexible wiring at chip layout)

2/ But never use TOP metal at IP pin.

3/ Once pull in wiring with (TOP – 1) metal from pin.

4/ Then, lift up toward TOP metal

5/ Next, lower to (TOP – 1) metal soon.
After that, we can freely make routing.

➔With this construction, antenna error can be prevented, so far as IP verification is completed.

* Here is an example of M6 process.

Fig-2. Cross section at A1-A2 of Fig-1

Reference

[1] John Liobe , “The antenna effect: Problems and Solutions”

[2] Devendra Singh Kushwaha and Bhumika Bisht , “A review of antenna effect in VLSI design”

[3] T.Matsukawa , “Comprehensive analysis of Variability Sources of FinFET characteristics” , Nanoelectronics research Inst., AIST

[4] Johe F. Chen, Carol Gelatos, Philip Tobin, Rob Shimer, Chenming Hu, “Reverse Antenna Effect due to process-induced quasi-breakdown of gate oxide”

[5] Gagal Kansal, Ajay Sharma, “Mitigating antenna effect in IC design”

Thank you for listening!!!