**1/ What is IO cell?**

IO cell (Input Output cell) is interface of LSI. They are placed at the periphery of a chip and provide an interface between the chip and the external world.

The role of IO in LSI chip:

+ Signal transmission from/to other LSI or other devices.

+ Power supply to internal circuit

+ Protection of internal circuit from ESD event.

**1.2 Where is IO design in LSI step?**

+ IO need be available before starting floorplan of P&R so we need estimate the size to P&R estimate size for whole chip.

**2/ How many are there IO cell types?**

There are five IO cell types: signal cell, power cell, filler cell, corner cell and bridge cell.

Main Purpose:

+ Signal cell: Power-grid maintenance, Signal transmission and ESD protection (diodes).

+ Power cell: Power-grid maintenance, Power transmission (pad - IO cells / pad - core) and ESD protection (diodes+GCNMOS)

+ Filler cell: Power-grid maintenance, placed empty area to connect other cells.

+ Corner cell: Power-grid maintenance and placed at the corner

+ Bridge cell: Power-domain separation, use to connect the different height IO cells.

**2.2 Why we need a lot of power cells?**

We classify Power supply cells into 3 main types base on their function:

+ Supply power for Core

+ Supply power for IO

+ Supply power for PSW, PSWC, LS, LSC

**3/ What is LEF?**

LEF (Library Exchange Format) is a specification for representing the physical layout of an integrated circuit in a ASCII format.

Library data includes layer, via, locations of ports, cell size, wiring prohibition area, placement site type, macro cell definitions and antenna information.

LEF is used in conjunction with Design Exchange Format (DEF) to represent the complete physical layout of an integrated circuit while it is being designed.

Purpose:

+ To serve for Place-and-Route of the concerned CAD tool (often used for Cadence P&R tool) with the basic information requested.

+ Consuming less memory compared with DFII

**Note:** CLASS BUMP needed for fcroute tool to when Routing could connect auto with PAD pin.

**4/ What is OBS?**

OBS layer (obstacle layer) is the geometry of the blockage layer where P&R can’t be done wiring connection on chip top level.

It includes metal and via layers with purpose boundary.

Purpose:

+ To certain the physical limits (spacing rule, overlap rule) of manufacturing process when CHIP TOP designer make Placement and Routing.

+ To keep secrets for valuable resources on layout by covering OBS layer.

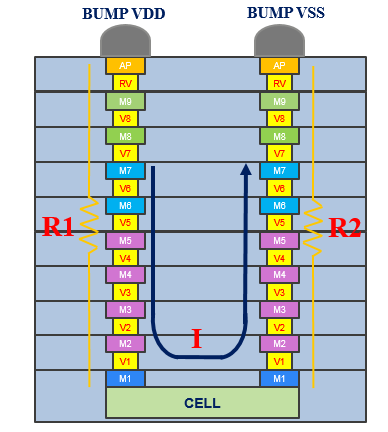
**5/ What is a liberty?**

Liberty is a kind of IO library, related with Electrical view and timing. It is a text file. The Content include some information of:

* + Timing delay for all timing arc
  + Transition time for each timing arc
  + Max capacitance of output pin
  + Capacitance of input pin

**6/ What is IR drop?**

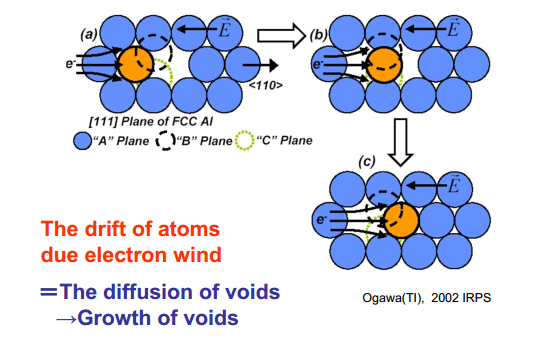
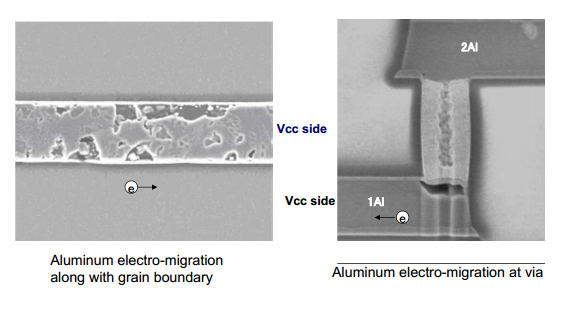
IR drop is an unwanted drop in voltage caused by current through a metal wire. It is named so because voltage (V) = current (I) \* resistance (R). An unexpected voltage drop on an instance or a device can cause a functional failure because the lowered voltage supply may not be strong enough to switch the instance, or may switch it too slowly. An IR analysis solution calculates the IR drop and shows real voltage values on devices.



VDrop = V supply – I\*(R1+R2)

**Fig1:** Drop calculation method in design

**7/ What is EM?**

* EM is the unwanted transport of material due to movement of ions in a conductor, caused by a transfer of momentum from electrons to these ions. One result is that high-density current in a narrow metal wire may destroy the wire. EM is thus a reliability problem that could occur after years of deployment in the field. An EM analysis solution calculates the current on each wire and compares it to foundry EM rules.

**Fig2:** Schematic of Electro-Migration mechanism **Fig3:** Electro-Migration mechanism in real

**8/ How to fix EM?**

**+** Widen width means increase metal width, upper metal layer.

+ Drop via at corner to reduce current flow at the congested area.

+ Move instance to near power stripe

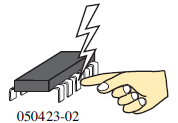
**What is ESD?**

* ESD stands for “Electrostatic Discharge”
* ESD is a physical phenomenon, the sudden flow of electrostatic charge between two objects, usually happening when two objects at different potentials come into direct contact with each other. ESD can also occur when a high electrostatic field develops between two objects in close proximity. ESD is one of the major causes of device failures in the semiconductor industry.

*Fig.: Electrostatic discharge from charged human body to door handle.*

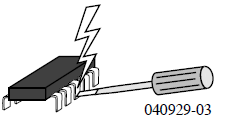
* ESD damage can occur at any point in the IC assembly and packaging, the packaged part handling or the system assembly process.
* Note that power is normally not ON during an ESD event.

**ESD damages in Integrated Circuits:**

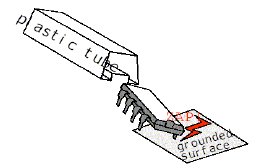
* Silicon melting
* Junction breakdown
* Gate breakdown

**ESD Models:** three different ESD stress models

* Human Body Model (HBM): representative of an ESD event between a human and an electronic component.

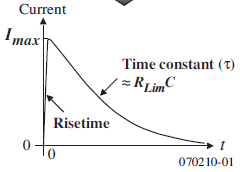
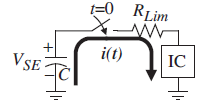


* Machine model (MM): simulates the ESD event when a charged “machine” discharges through a component.



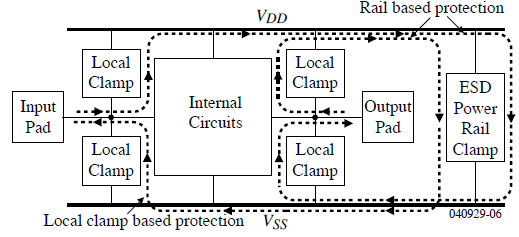
* Charge device model (CDM): simulates the ESD event when the component is charged and then discharges through a pin. The substrate of the chip becomes charged and discharges through a pin.

**Key parameters of an ESD event:**



* Maximum current flow
* Time constant or how fast the ESD event discharges.
* Rise-time of the pulse.

**ESD protection:**



The principal of ESD protection is that conducting ESD current flowing from charged pin(s) to ground pin(s) of chip through ESD devices, steered it away from internal circuits. ESD devices are Local clamp (diodes, snapback NMOS), and ESD power rail clamp (GCNMOS, RC time circuit).

Designers have to care in 3 phases: cell level design, chip integration, and verification.

* Cell level design: place ESD devices inside cell level (mainly in I/O cells), ESD device size and wire resistance are based on spec and know-how implementation.
* Chip integration: mainly in I/O arrangement, distribute positions of IO cells (w/ & w/o ESD power rail clamp) based on spec of power rail clamp size and wire resistance.
* Verification: uses EPOD tool, and check points in ESD checklist.

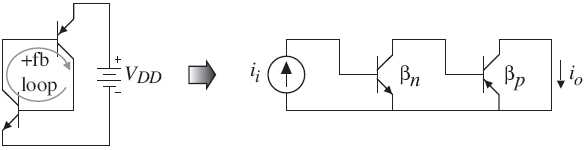
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | VIA | Metal |  |  |  |  |  |  |  |
| Cross Section (um2) | =n\*R2\*3.14 | = Thickness\*n | | when IESD passed | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  | R2=(X/2)\*(Y/2) |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| EM(mA) | =n\*Imax\*(relax\_rule) | =Imax\*(width\*Imax2-Imax3)\*n\*relax\_rule\*temp\_para | | | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

**What is latchup?**

Latchup refers to short circuit formed between power and ground rails in an IC leading to high current and damage to the IC. Speaking about CMOS transistors, latch up is the phenomenon of low impedance path between power rail and ground rail due to interaction between parasitic pnp and npn transistors. The structure formed by these resembles a Silicon Controlled rectifier (SCR, usually known as a thyristor, a PNPN device used in power electronics). These form a positive feedback loop, short circuit the power rail and ground rail, which eventually causes excessive current, and can even permanently damage the device.

**Latch-up prevention techniques**:

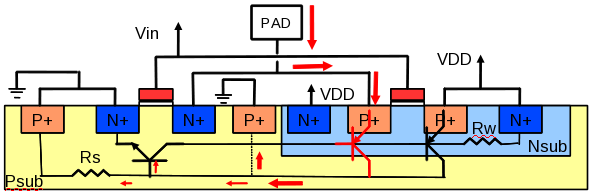
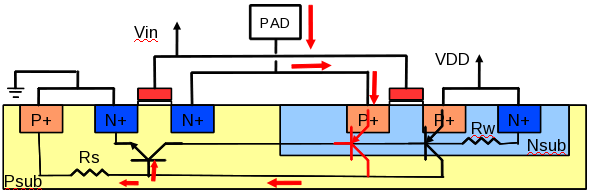
1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.



Loop gain:

2.) Reduce the values of Rw and Rs. This requires more current before latch-up can occur.

3.) Surround the transistors with guard rings. Guard rings reduce transistor betas and divert collector current from the base of SCR transistors.

****

Add guardring

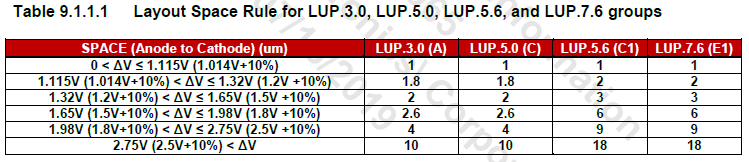
**Layout rule relating to Latch-up preventing**

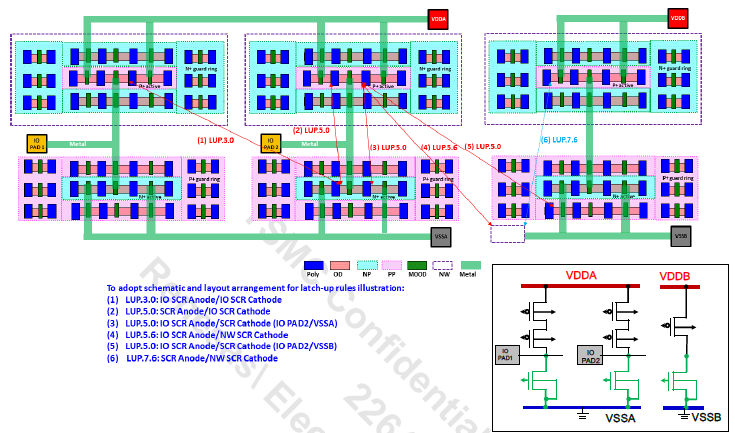
LUP.2 is the rule concern to latch-up error between IO MOS and internal MOS

LUP.2 area checking is extended area 15um from OD of IO MOS

1.) Within 15 um space from the MOS connected to an I/O pad, do not place any internal MOS (which is not have full guard-ring – p+ guard-ring or n+ guardring) inside this area

2.)Cover all internal MOS with full guardring (p+ guardring or n+ guardring)





**What is multi-patterning? (double-patterning in T16)**

* At the 20-nm process node and below, printing the required geometries is extremely difficult with the existing photolithography tools. The quality is lost due to diffraction of light around the corners and edges of the mask since the features are too small compared to the wavelength of light. => Multiple patterning, is used to partition the layout mask into two or more separate masks, each of which has an increased manufacturing pitch to enable higher resolution and better printability.

T7nm process, double patterning (DP) is used to partition the layout mask into two separate masks. The decomposition of the geometries of a metal layer into two sets, a process called “coloring” to the metals (red and green as shown in the image).

* In trade-off for the advantages in manufacturing process, there are certain additional design rules for DP to be successfully implemented. Besides Cost can be expensive, as it doubles the process steps in the lithography flow litho-etch-litho-etch (LELE)

**What is the shielding?**

* In practical layout, between 2 neighboring metal patterns have parasitic capacitance, crosstalk noise may affect from this signal to other signals.

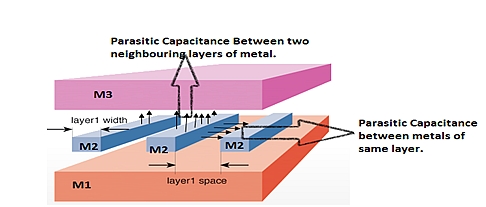


Fig 1 : Parasitic capacitance

* Shielding is the technique to reduce the interference between signal nets and other adjacent nets. In practical design, GND metal patterns surrounding signal nets are used as shield.

Parallel

Mx-1

Mx

Mx+1

Tandem

Signal

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

signal

Mx-1

Mx

Mx+1

Coaxial

VSS

signal

VSS

VSS

VSS

Fig 2: Some types of shielding

**What is shield ring and its application?**

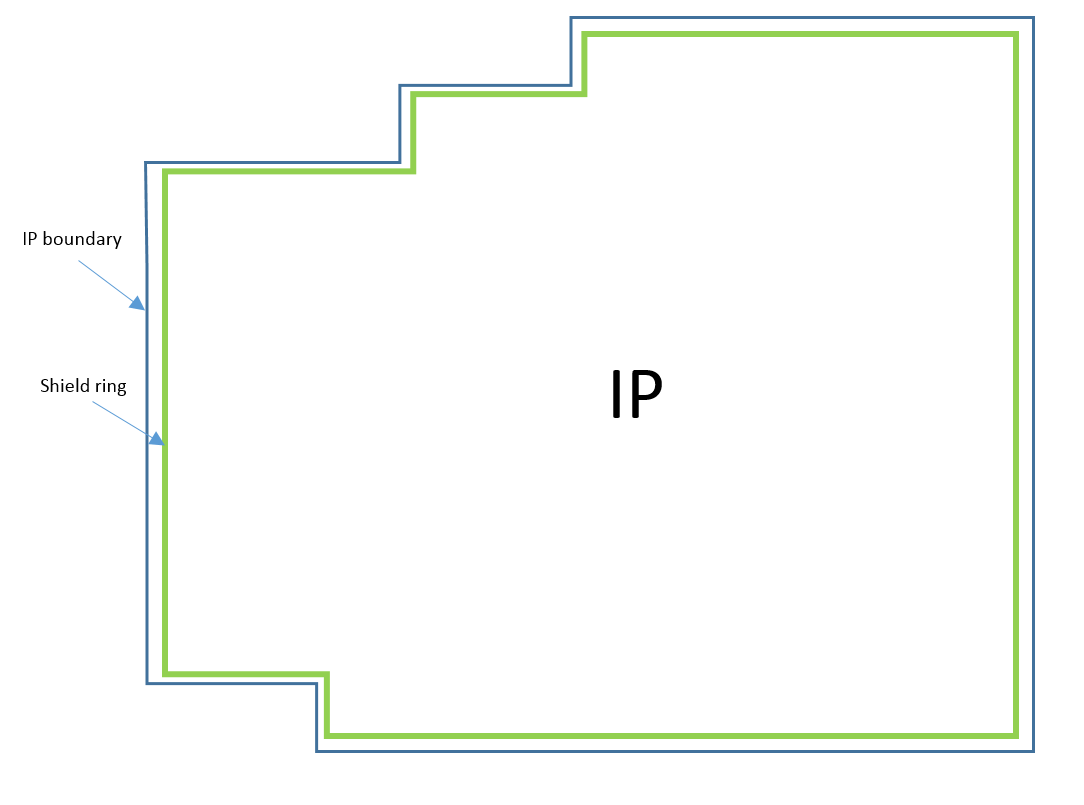
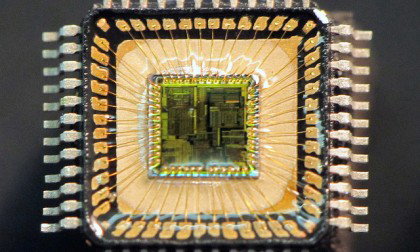
****

Fig: shield ring implementation in a real design

* Shield ring is the ring of patterns surrounding domain to prevent noise from this domain affect to other domains. The width of shield ring and the distance between shield ring and IP boundary base on spec.

**What is BUMP, PAD?**

BUMP, PAD are special physical patterns which are constructed from some materials. They are used for connection from I/Os of silicon die to their package. BUMP is used in Flip-Chip technology. PAD is used in Wire Bonding technology.

In Wire Bonding Technology, IOs and PADs are only placed in Chip peripheral. PADs are connected to IO’s Pad pins by Top metal. PADs are connected to the package by Bonding Wire.

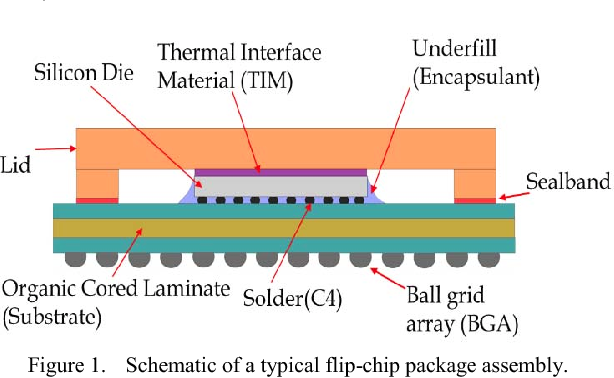
**Chip Top design in Wire Bonding technology**

**Source from** : <https://cse.buffalo.edu/~sheenara/Pad%20Frame%20Introduction.html>

**Wire Bonding Chip**

**Source from** : <http://www.armge.com/en/solutions/production-and-design/>

In Flip-Chip technology, IOs and BUMPs are placed in flexible positions of Chip area such as Chip peripheral area, Chip core area. BUMPs are connected to IO’s Pad pins by Redistribution Layer. BUMPs directly connect to the package by soldering them to package’s connectors.



IO buff

Redistribution

layer

bump

Chip surface

**Source from**: : https://www.semanticscholar.org

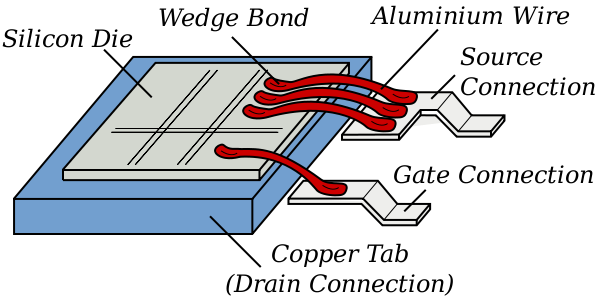
**Chip top design in Flip-Chip technology**

**What are wire bonding, flip-chip?**

**Flip-chip** and **Wire bonding** are two different methods to interconnect semiconductor devices to external circuitry in **integrated circuit packaging** steps.

**How to distinguish between wire bonding and flip-chip:**

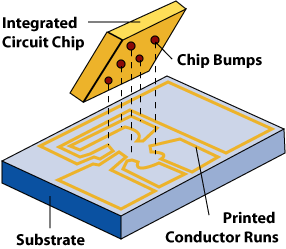
* Flip chip assembly is the direct electrical connection of face-down (“flipped” – This is how they called flip-chip) electronic components onto substrates, circuit boards, or other components by conductive bumps. In contrast, wire bonding, the older technology that flip chip replaces, uses face-up chips with an individual wire connected to each bond pad. Figures below show the difference between wire bonding and flip-chip.



*Face-up*

*(BEOL on top & FEOL on bottom of IC)*

*Face-down  
(FEOL on top & BEOL on bottom of IC)*



*Flip-chip*

*Wire bonding*

**Advantages and disadvantages of flip-chip comparing to wire bonding:**

* **Advantages of flip-chip:**

+ Small package size.

+ Short wire leads to reduce inductance.

+ Allowing higher – speed signals.

+ Conduct heat better.

* **Disadvantages of flip-chip:**

+ Not easy for replacement and manual installation.

+ Require very flat surfaces.

+ Thermal expansion leads to connections break.

**What is RDL?**

* RDL stands for “Redistribution Layer”.
* RDL, an essential term in flip-chip design, is an extra metal layer used to redistribute IO PADs to BUMPs without changing the IO cell placement.

IO

Redistribution

layer

bump

Chip surface

*After routing*

**RDL routing**

**PG core mesh**

**IO Cells**

**Bump**

**Net assignment**

*Before routing*

*Figure: RDL routing implementation.*

**What is power spec?**

* Power spec specify power domain for design, defines which (group) cell will belong to each power domain, as well as PG connections for each domain, …
* Power spec is used to create UPF file for PnR and used during verification phase (PP\_check, LVS, ...).
* Example power\_spec\_file (file \*.ps) used for PP check:

# 2018/05/14 10:03:52 PEX V01.07.00

# NOCHECK with verilog netlist

if\_block

ir.ir\_c4 C4

top.top\_nonfb.cpgmc.I\_zckbuf.I\_outbuf C4\_DVFS\_CA57

ca57ss.u\_dvfs.u\_CA57INTEG\_ucpu1 A1B1

…

\* DEFAULT

end

if\_area

DEFAULT VDD(1.25, H, VDD, P, ) VSS(0,0, L VSS, P )

PD\_VDD\_VSS VDD(1.25, H, VDD, P, ) VSS(0,0 L, VSS, P, )

…

end

Explaination: date, time creation, version

Define modules belong to which domain,

start with “if\_block”, end with “end” definition

Define voltage for each supply net supply (power/ground) inside domain,

start with “if\_area”, end with “end” definition

area\_activity

A2BS\_OFF A1B0(OFF) A1B1(OFF) A2BS(OFF) A1L0(ON) A1L1(ON) …

A2RGXB\_OFF A1B0(ON) A1B1(ON) A2BS(ON) …

…

end

Define activity status (ON/OFF) of domains

start with “area\_activity”, end with “end” definition

sysc\_info SYSC

ISOLATION\_A2VC1 A2VC1->C4 ( top.top\_nonfb.sys.isolation\_a2vc[1] H )

ISOLATION\_RGXA A3RGXA->C4\_DVFS\_RGX ( \

top.top\_nonfb.sys.isolation\_sgx[0] H \

top.top\_nonfb.sys.isolation\_sgx[1] H )

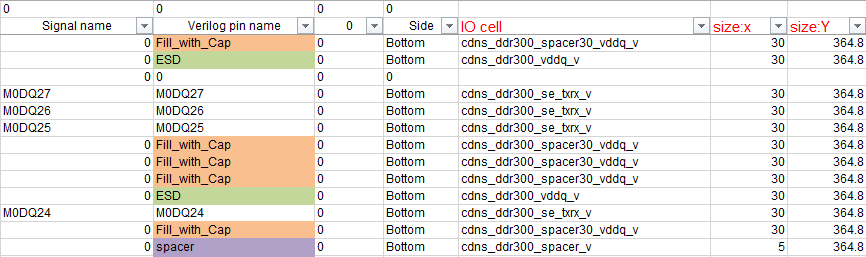
…

end

Define the pins to control the indeterminate propagation.

start with “if\_area”, end with “end” definition

**What is IO pin package assignment? IO pin assign (IOPA)? BUMP assignment?**

* IO pin package assignment: define information of I/O cells (cell name, instance name, pin, pad, size, orientation,…), and connections from I/O PADs 🡪 BUMPs, BUMPs 🡪 package pins. It is used for IO placement, BUMP assignment, and RDL routing. Below picture is example:
* IO pin assign (IOPA) file: in EPOD check, it is the file which describes the information of PAD number, PAD name, PAD position, IO cell name related to PAD etc.

(EPOD: ESD Protection Device Circuit Placement Check)

Define meaning of each collumn.

VERSION:######;

DESIGN:r7f5a009;

orderdef: WDPAD, PINNAME, IOBUF, PADNAME, INSTNAME;

LB001, AVSS0\_0, pf3v30tc, VSSPLL, AVSS0\_0\_PIO;

...

LR001, P20, pf3c3bo0o2godvql, pad, iotop.pamnvcc.AUTO\_IOBUF\_P20;

...

LT056, PC1, pf3c3bo0o2godvql, pad, iotop.pamnvcc.AUTO\_IOBUF\_PC1;

...

LL046, P82, pf3c3bo0o2godvql, pad, iotop.pamnvcc3.AUTO\_IOBUF\_P82;

...

Design name

Order and name of each IO,

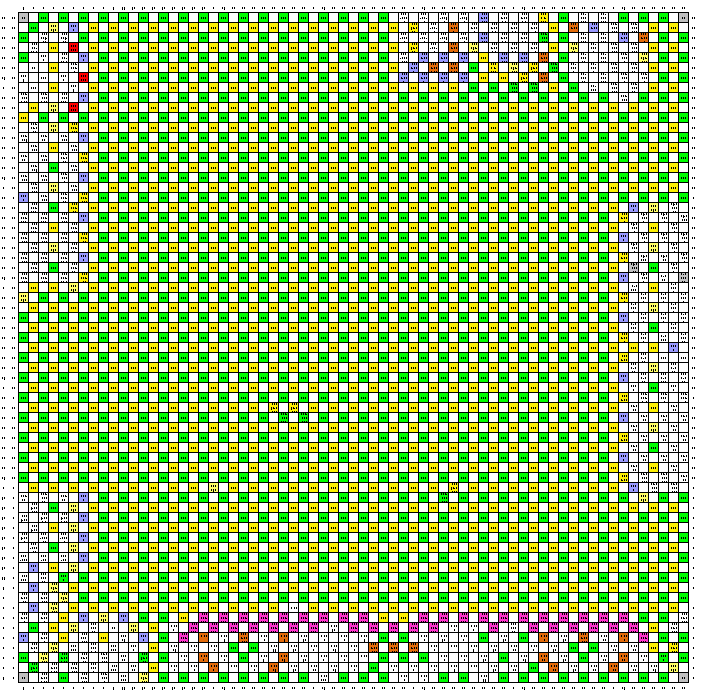
LB : bottom

LR : right

LT : top

LL : left

* BUMP assignment: define BUMP arrays, location and name of BUMPs. It is used to make BUMP def file and BUMP connections.



**What does Calibre, Hspice, PP check, EPOD, Custom Compiler, Virtuoso, HSSC, Quickview, Totem, PTPX, Voltus, EPS, Eagle, StarRC, QRC do?**

All of them are Applications which being used at Physical Layout phase for designing, checking and verifying.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| No | Tool name | Vendor | Main function | Description |
|  | Calibre | Mentor Graphics Corporation | Dummy generation, Physical Verification | Calibre tools package include: - Dummy generation (OD/PO, COD, Metal/Via, WM).  - Physical Verification: LVS, ERC, DRC, LVL, Antenna, … |
|  | HSPICE | Synopsys | Circuit simulation | To check the characteristics of circuit: timing, drivability, logic function, … |
|  | PP check | Renesas in-house | PG connection verification | Input is Verilog (with PG). This tool checks if PG connections abide by Power Specification or not. |
|  | EPOD | Renesas in-house | Check ESD protection circuits | E-POD : ESD PrOtection Device circuit placement check.  To verify the ESD protection circuit in accordance with the ESD Design Guidelines.  Input: CDL netlist, IO pin assign (IOPA), tech file, PKG connection. |
|  | Custom Compiler | Synopsys | Custom circuit and layout design | Custom Compiler™ is Synopsys' full-custom solution that features the pioneering visually-assisted automation flow that speeds up custom design tasks, reduces iterations and enables reuse. |
|  | Virtuoso | Cadence | Custom circuit and layout design | Virtuoso design tools support full custom analog, digital, RF, and mixed-signal designs at the device, cell, block, and chip levels. |
|  | HSSC | Synopsys | Resistance calculation and display | HSSC: Hercules+StarRC+SPRES+CustomDesigner.  HSSC is an analyzed system that, calculates, and displays routing resistance. |
|  | Quickview | Cadence | View GDS | This tool helps us view GDS/LEF/DEF data quickly. It just allows to view GDS but can not edit. |
|  | Totem PathFinder | ANSYS Apache | Post-Layout Static ESD Analysis, Resistance Analysis | Use to measure wiring resistance taking parasitic into consideration, and ESD/EM analysis. |
|  | PTPX | Synopsys | Analyzes power dissipation of a cell-based design | PrimeTime PX supports two types of power analysis modes: averaged and time-based. Averaged mode calculates average power based on toggle rates, while time-based mode provides both peak and average power using gate-level simulation activity. |
|  | Voltus | Cadence | EM/IRdrop analysis | The Voltus tool helps analyze EM/IRdrop of design, support designers debugging, verifying, and fixing IC chip power consumption, IR drop, and electro-migration (EM) constraints and violations (EMIR). |
|  | EPS | Cadence | EM/IRdrop analysis | EPS is same function as Voltus but old generation. Voltus is new generation. |
|  | Eagle | Mentor | Checking shielding for analog nets | EAGLE: Embedded IP Analog noise Guideline Layout chEcker  Eagle checks the Shielding for all Analog nets about some criteria: spacing, density, number of shields.  Eagle AIP (Analog), FIP (Flash) |
|  | StarRC | Synopsys | R/C extraction | Extract parasitic Resistance & Capacitance information using in Digital and Custom/Analog flow. |
|  | QRC | Cadence | R/C extraction | Extract parasitic Resistance & Capacitance information using in Digital and Custom/Analog flow. |

**What is DEF, LEF?**

**I. LEF**

**Library Exchange Format (LEF)** is data file, which contains the technology information of the design library. The LEF format defines the elements of an IC process technology and associated library of cell models, including layer, via, placement site type, and macro cell definitions. LEF file can be exported or imported by layout tools (ICC/ICC2, INNOVOUS, Virtuoso) so that we can use it as an input data for other tools (quickview , Voltus, StarRC ….).

In physical verification, we can use LEF to make a text.lis ( a text file that contain information of pins) using for DRC/LVS check.

**Example:**

**##**

**## LEF for PtnCells ;**

**## created by Innovus v16.25-s072\_1 on Wed Aug 1 20:39:58 2018**

**##**

**VERSION 5.8 ;**

**BUSBITCHARS "[]" ;**

**DIVIDERCHAR "/" ;**

**MACRO u7796hrcam30cc00**

**CLASS BLOCK ;**

**SIZE 1900.3200 BY 657.6000 ;**

**FOREIGN u7796hrcam30cc00 1212.1200 -1419.1200 ;**

**ORIGIN 0 0 ;**

**SYMMETRY X Y R90 ;**

**PIN x\_apreset\_armcm\_c4\_ack\_zs\_CCI500SS**

**DIRECTION OUTPUT ;**

**USE SIGNAL ;**

**ANTENNADIFFAREA 0.045792 LAYER M4 ;**

**ANTENNAPARTIALMETALAREA 0.0542 LAYER M4 ;**

**ANTENNAPARTIALMETALSIDEAREA 0.1897 LAYER M4 ;**

**PORT**

**LAYER M4 ;**

**RECT 0.0000 527.1800 0.3760 527.2200 ;**

**END**

**END x\_apreset\_armcm\_c4\_ack\_zs\_CCI500SS**

**PORT**

**LAYER M6 ;**

**RECT 0.0000 527.5800 0.3760 527.6200 ;**

**END**

**……..**

**ENDMACRO u7796hrcam30cc00**

**II. DEF**

**Design Exchange Format (DEF)** is data file, it defines the elements of a design that are related to the physical layout, including the placement and routing information, design netlist, and design constraints. It contains the design-specific information for a circuit and is a representation of the design at any point during the layout process. DEF file can be exported or imported from design data layout tools (ICC/ICC2 , INNOVOUS, Virtuoso so that we can use it as an input data for other tools (quickview , Voltus, StarRC ….).

**Example:**

**###############################################################**

**# Generated by: Cadence Innovus 16.25-s072\_1**

**# OS: Linux x86\_64(Host ID rvc-srv0343)**

**# Generated on: Wed Aug 1 20:40:01 2018**

**# Design: u7796hrcam30cc00**

**# Command: defOut -routing /shsv/Backend8/RCarM3ES3/4.DESIGN/CN/12.CC/2.PNR/21A.INNOVUS\_FLOW/OUTPUT\_DATA/PnR\_dataOut\_180801\_2035/def/u7796hrcam30cc00\_postlay\_180801\_2035.def.gz**

**###############################################################**

**VERSION 5.8 ;**

**DIVIDERCHAR "/" ;**

**BUSBITCHARS "[]" ;**

**DESIGN u7796hrcam30cc00 ;**

**UNITS DISTANCE MICRONS 2000 ;**

**DIEAREA ( 3939120 -2838240 ) ( 3939120 -2565600 )**

**( 2424240 -2565600 ) ( 2424240 -1523040 )**

**( 6224880 -1523040 ) ( 6224880 -2588640 )**

**( 5114160 -2588640 ) ( 5114160 -2838240 ) ;**

**ROW CORE\_ROW\_0\_b\_1 core7d5T 3939120 -2838240 N DO 4500 BY 1 STEP 192 0**

**;**

**……**

**- VIA23\_1cut\_HH\_E**

**+ RECT M2 ( -82 -32 ) ( 82 32 )**

**+ RECT M3 ( -96 -38 ) ( 128 38 )**

**+ RECT VIA2 ( -32 -32 ) ( 32 32 )**

**;**

**……**

**COMPONENT 20981**

**- u\_cci500ss/u\_cci\_integration/u\_cci500\_integration\_lockstep/psoI\_PDa3rc\_XX\_FSGA2SA0YSRGV10500N\_119\_136\_11 FSGA2SA0YSRGV10500N + SOURCE DIST + FIXED ( 2881800 -2565216 ) FS**

**;**

**…….**

**ENDCOMPONENT**

**Correlation between Layout design database (NDM, CEL, ENC) and LEF/DEF:**

**Because LEF/DEF are exchange data made from Layout design database. They must be consistent with database. There might mismatch about location of pin, port name for LEF; or mismatch of instance, nets for DEF during the iteration of design. The output LEF/DEF must be verified with layout design database.**

**Package design**

* What is IC package?

In electronics manufacturing, integrated circuit packaging is the final stage of semiconductor device fabrication, in which the tiny block of semiconducting material is encapsulated in a supporting case that prevents physical damage and corrosion. The case, known as a “package", supports the electrical contacts which connect the device to a circuit board.

* Why need IC package?

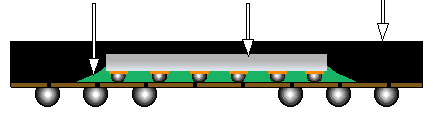
The package provides **protection** against impact and corrosion, holds the contact pins which are used to **connect from external** circuits to the device (die), and **dissipates heat** produced in the device.

* Basic processes of IC package:

There are various IC package process flows depend on package types. Below are some main steps for making an IC package after die manufacturing:

IC Mounding > IC Bonding (Wire Bonding/Flip Chip) > IC Encapsulation > Wafer bonding.

* Various methods in IC Bonding: Flip Chip vs Wire Bonding



Die

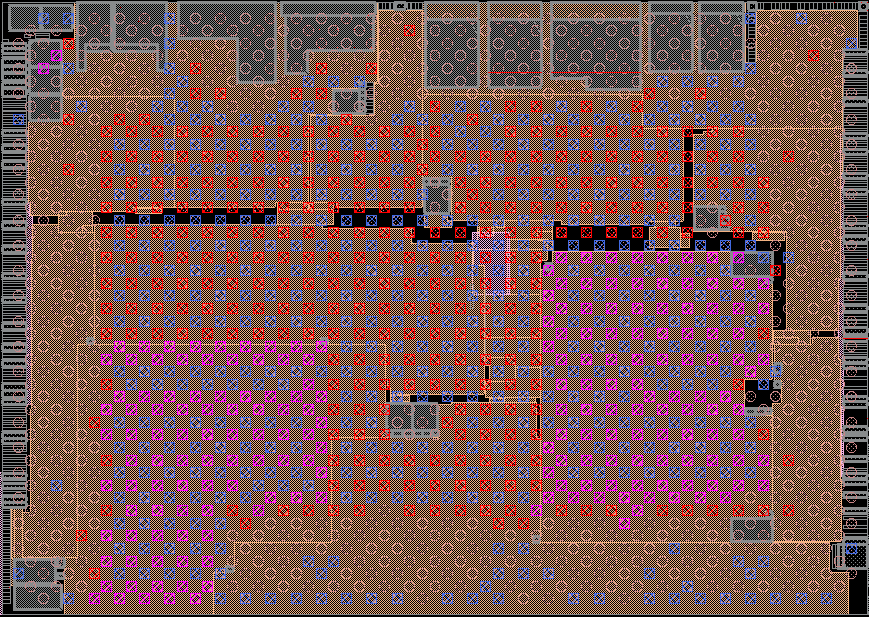
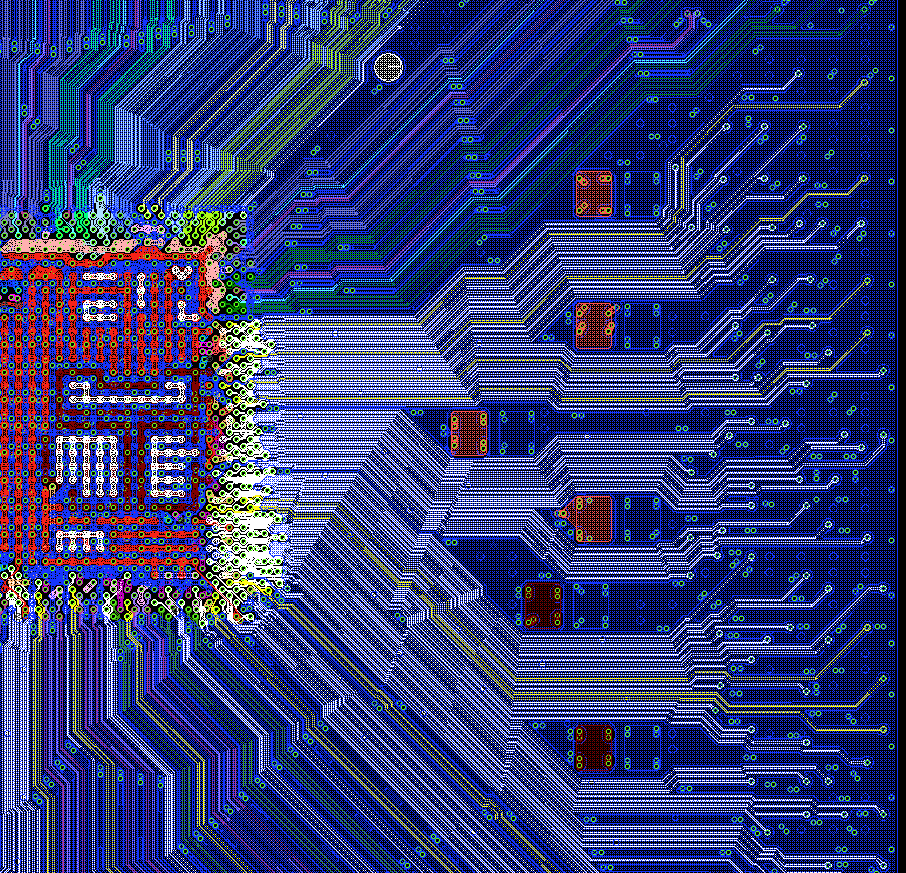
Epoxy under-fill

Mold Cap

Bump

Solder Ball

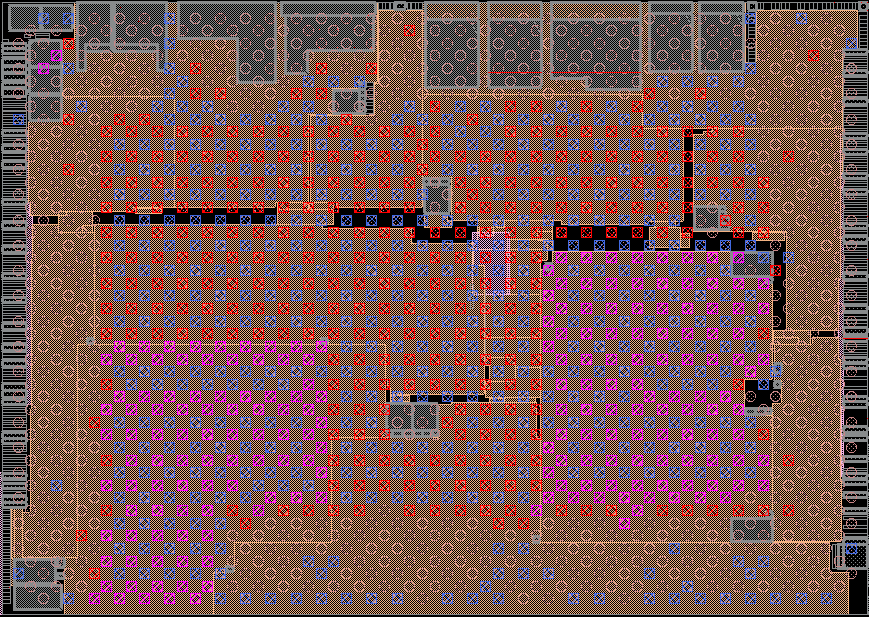
*Flip chip bonding style (cross section)*



Layout design

Die

Flipped



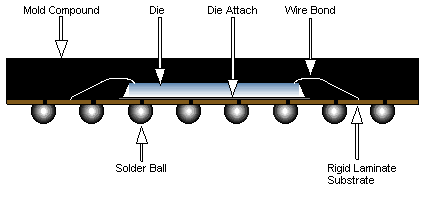
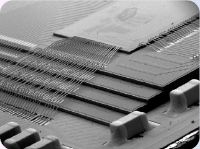
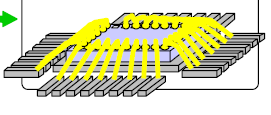
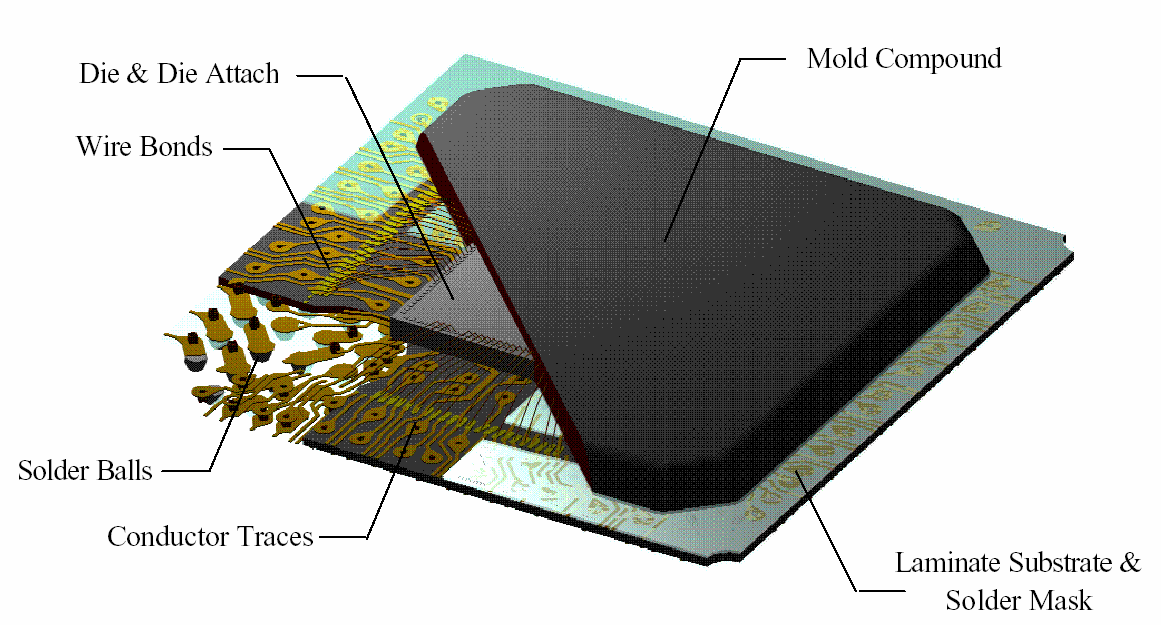
Die

Flip

Chip design with RDL

PKG routing design

*Flip chip bonding style including package layout design*



Cross section:

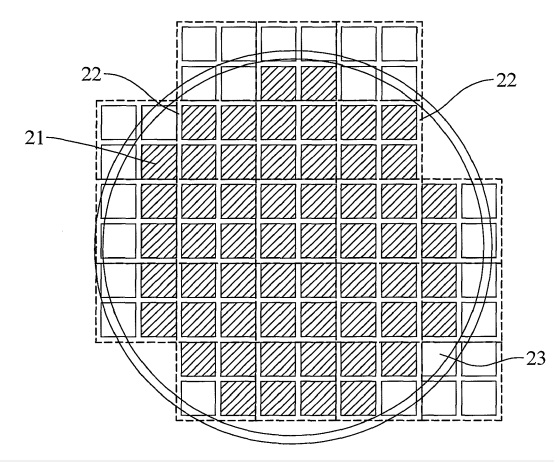
*Wire bonding bonding style (cross section and real chip picture)*

# Scribe line

* What is Scribe line?

During dicing process, a wafer with up to thousands of same circuits is cut into rectangular pieces, each called a die. In between those functional parts of the circuits, a thin non-functional spacing is foreseen where a saw can safely cut the wafer without damaging the circuits. This spacing is called the *scribe line* or *saw street*.

The width of the scribe is very small comparing to die size, typically around 100 [μm](https://en.wikipedia.org/wiki/Micrometre). A very thin and accurate saw is therefore needed to cut the wafer into pieces.



Scribe line Y

Incomplete exposure die

complete

exposure die

Wafer disc

Scribe line X

*Explanation for scribe line on wafer*

**Single scribe**

Combined from isolation, seal ring, dummy bar, space was placed symmetrically with one test line. At the center of it, the dicing line using as a cutting line to divide wafer into dies.

**Double scribe**

Combined from isolation, seal ring, dummy bar, was placed symmetrically with two space and two test lines. The dicing line was placed at 2nd test line.

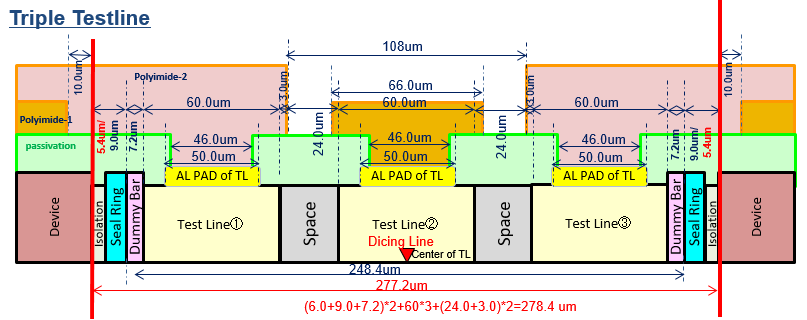
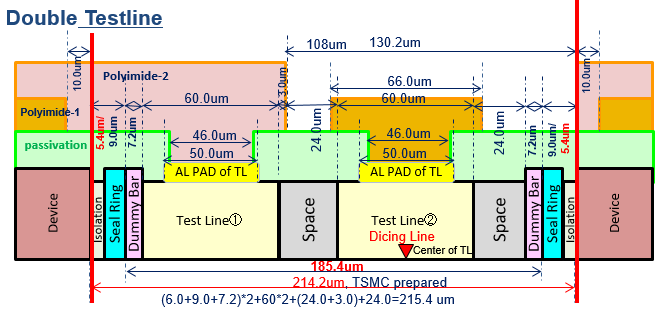
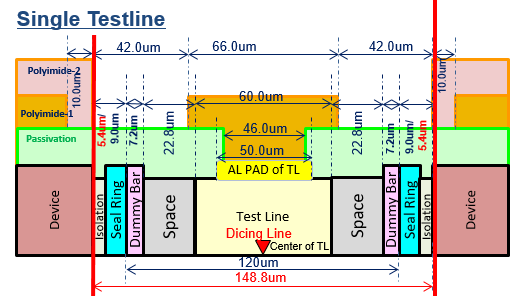
**Triple scribe line**

Combined from isolation, seal ring, dummy bar, was placed symmetrically with two space and three test lines. The dicing line was place at 2nd test line, also so center of the scribe line.

In design phase, we do assumption for the type of scribe line to calculate chip size and MFU as draft version.

After tapeout, TSMC will determine the actual scribe line width and seal ring needed for the design to calculate the final MFU number.

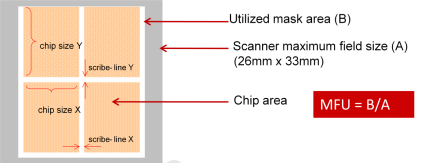
**Scribe line structure by TSMC**



**What is MFU? How to choose chip size for best MFU?**

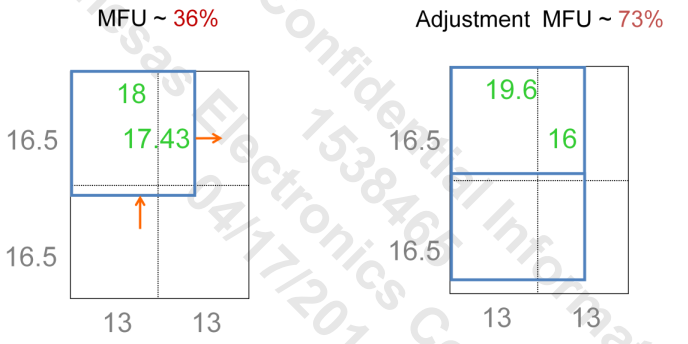
**MFU (Mask Field Utilization)**

Mask Field Utilization refers to the ratio of the mask area occupied by the die image compared to the maximum scanner field size, which is 26mm by 33mm (TSMC’s). MFU impacts how quickly the scanner can create die images of a single mask layer and also significanlty affects photolithography.



**How to choose chip size for best MFU?**

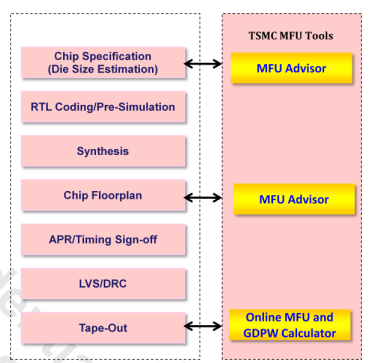
To have a best MFU, chip size must be considered deeply during the design phase. With a same area of die size can gives two different MFU percentages by changing the die aspect ratio.



*Same chip size for both cases: MFU per centage can be increased by changing die aspect ratio.*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **MFU number** | 80%-85% | 85%-90% | 90%-95% | 95%-100% |
| **Manufacturing cost discount** | 0% | 1% | 2% | 3% |

*Manufacturing cost discount proposed by TSMC.*



*Design flow with MFU consideration (TSMC’s)*