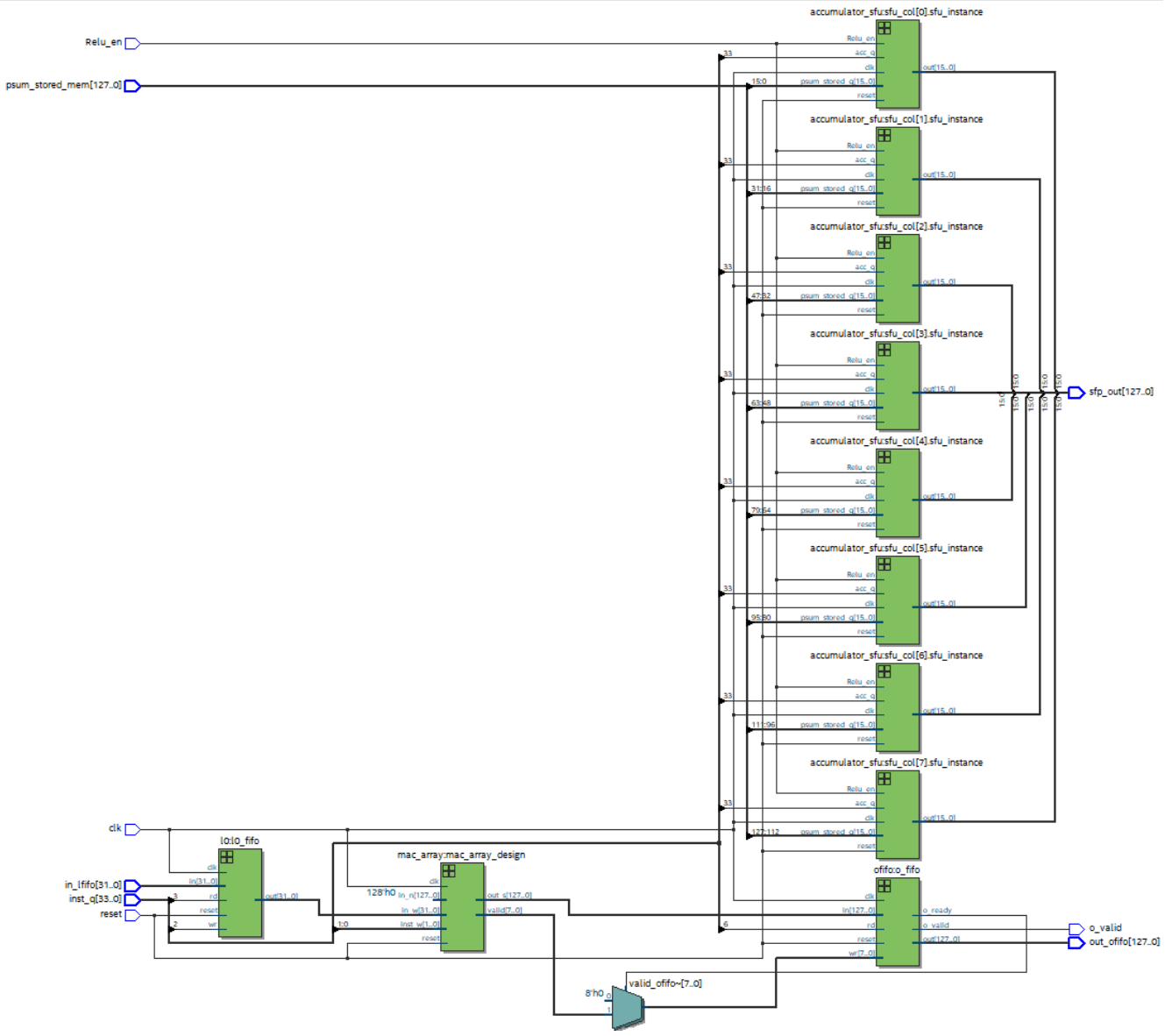
FPGA SYNTHESIS AND IMPLEMENTATIONS RESULTS

Vanilla Model



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	Vanilla Model (Cyclone IV GX)
Total Operations per cycle	128
Frequency	121.07MHz
Resource Utilization	Combinational Blocks without Register – 5142 Combinational Blocks with Register – 6931 Registers - 5167
Power Estimates	Total Thermal Power Dissipation – 339.46 mW

	Core Dynamic Thermal Power Dissipation – 35.96 mW Core Static Thermal Power Dissipation – 119.63 mW I/O Thermal Power Dissipation – 183.87 mW
TOPs	0.015496
TOPs/W	4.3 micro (TOPs/W)