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16-Bit, 8-Channel, Software Configurable Analog Input Module for Programmable Logic Controllers (PLCs)



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Design Resources

TIDA-00164	Input Module Design Files
TIDA-00123	I/O Controller Design Files
ADS8688	Product Folder
ISO1540	Product Folder
TCA6408A	Product Folder
LM5069	Product Folder
LM5017	Product Folder
ISO7141	Product Folder
TPS70950	Product Folder
TPS70933	Product Folder



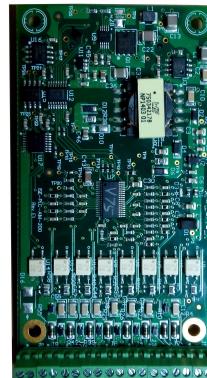
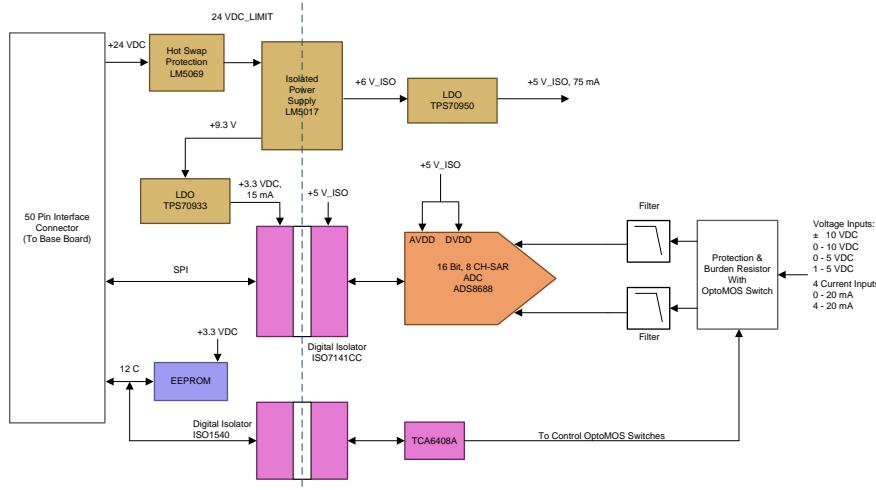
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Design Features

- Up to 8 Channels of User-Programmable Inputs
 - Voltage Inputs (with Typical Z_{IN} of $1 \text{ M}\Omega$): $\pm 10 \text{ V}$, $\pm 5 \text{ V}$, $\pm 2.5 \text{ V}$, 0 to 10 V and 0 to 5 V
 - Current Inputs (with Z_{IN} of $300 \text{ }\Omega$): 0 to 20 mA and 4 to 20 mA
- 16-Bit SAR ADC with SPI
- Accuracy Over Entire Input Range
 - Voltage: $<\pm 0.2\%$ Full Scale at 25°C
 - Current: $<\pm 0.2\%$ Full Scale at 25°C
- Onboard Isolated Fly-Buck™ Power Supply with Inrush Current Protection
- Slim Form Factor $96 \times 50.8 \times 10 \text{ mm}$ ($L \times W \times H$)
- Pluggable to I/O Controller for Easy Evaluation Platform ([TIDA-00123](#))
- LabView™-Based GUI for Signal-Chain Analysis and Functional Testing
- Designed to Comply with IEC61000-4 Standards for ESD, EFT, and Surge

Featured Applications

- PLC: Current and Voltage Input Module
- Remote PLCs and DCS
- Data Acquisition Systems
- Test and Measurement



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1 System Overview

This reference design provides a complete solution for a single-supply industrial control analog input module. The reference design is suitable for process control end equipment like programmable logic controllers (PLCs), distributed control systems (DCS), data acquisition systems (DAS) modules that must digitize standard industrial current inputs, and bipolar or unipolar input voltage ranges up to ± 10 V. In an industrial environment, the analog voltage and current ranges typically include ± 2.5 V, ± 5 V, ± 10 V, 0 to 5 V, 0 to 10 V, 0 to 20 mA, and 4 to 20 mA.

This reference design can measure all standard industrial voltage and current inputs. Eight channels are provided on the module, and each channel can be configured as a current or voltage input with software configuration.

The SAR-based architecture of ADS8688 leverages better sampling rates. ADS8688 also includes an on-chip PGA. The on-chip PGA uses the gain and ensure maximum of the ADC's input dynamic range. Depending on the range of the input signal, the PGA gain is adjusted by setting the Range_CHn in the program register. ISO7141 and ISO1541D provide digital signal isolation between the host microcontroller and the measurement side. The power isolation has been achieved using LM5017-based Fly-Buck transformer. The module has an onboard EEPROM to store calibration data and module configuration data. This reference design also demonstrates the TI products like the hot swap and inrush current-limit controller, isolated Fly-Buck controller, low noise LDO, and I²C-to-GPIO expander that can be used in the entire PLC signal processing chain.

The module has been designed to be pluggable to the I/O controller ([TIDA-00123](#)) for quick testing and evaluation. The module reference design also includes an external protection circuit and has been tested and verified to comply with IEC61000-4 standards for electrostatic discharge (ESD), electrical fast transient (EFT), and surge requirements with an I/O controller platform.

The schematics, BOM, PCB layout (Altium tool), Gerber, Tiva™ C Series MCU software, and the executable for an easy-to-use graphical user interface (GUI) are also provided.

2 Design Specification

Table 1 provides configuration information of the 16-bit resolution SAR ADC.

Table 1. Configuration of 16-Bit Resolution SAR ADC

PARAMETER	SPECIFICATIONS / FEATURES	
Number of channels	Eight channels	
Input range	Voltage: <ul style="list-style-type: none"> • ± 10 V • ± 5 V • ± 2.5 V • 0 to 10 V • 0 to 5 V 	Current: <ul style="list-style-type: none"> • 0 to 20 mA • 4 to 20 mA
Input impedance	Voltage >1 M Ω	Current <300 Ω
Overall accuracy	Voltage Input: $\pm 0.2\%$ full scale at 25°C	Current Input: $\pm 0.3\%$ full scale at 25°C
Power supply isolation	250-V DC (continuous) 1500-V AC for one minute (withstand)	
ESD immunity	IEC 61000-4-2: <ul style="list-style-type: none"> • 4 kV contact discharges • 8 kV air discharges 	
EFT immunity	IEC 61000-4-4: <ul style="list-style-type: none"> • ± 2 kV at 5 kHz on signal ports • ± 2 kV at 100 kHz on signal ports 	
Surge transient immunity	IEC 61000-4-5: ± 1 kV line-earth (CM) on signal ports	
Operating temperature range	0°C to 60°C	
Storage temperature	−40°C to 85°C	
Connectors	<ul style="list-style-type: none"> • 50-pin connector pluggable to PLC I/O module front-end controller using a Tiva C Series ARM® Cortex®-M4 MCU (TIDA-00123) • 8 × 2-pin screw terminal block for analog input connection • 2-pin for protective earth connection 	
Form factor (L × W)	90 × 50.8 mm (small industrial form factor)	

3 Block Diagram

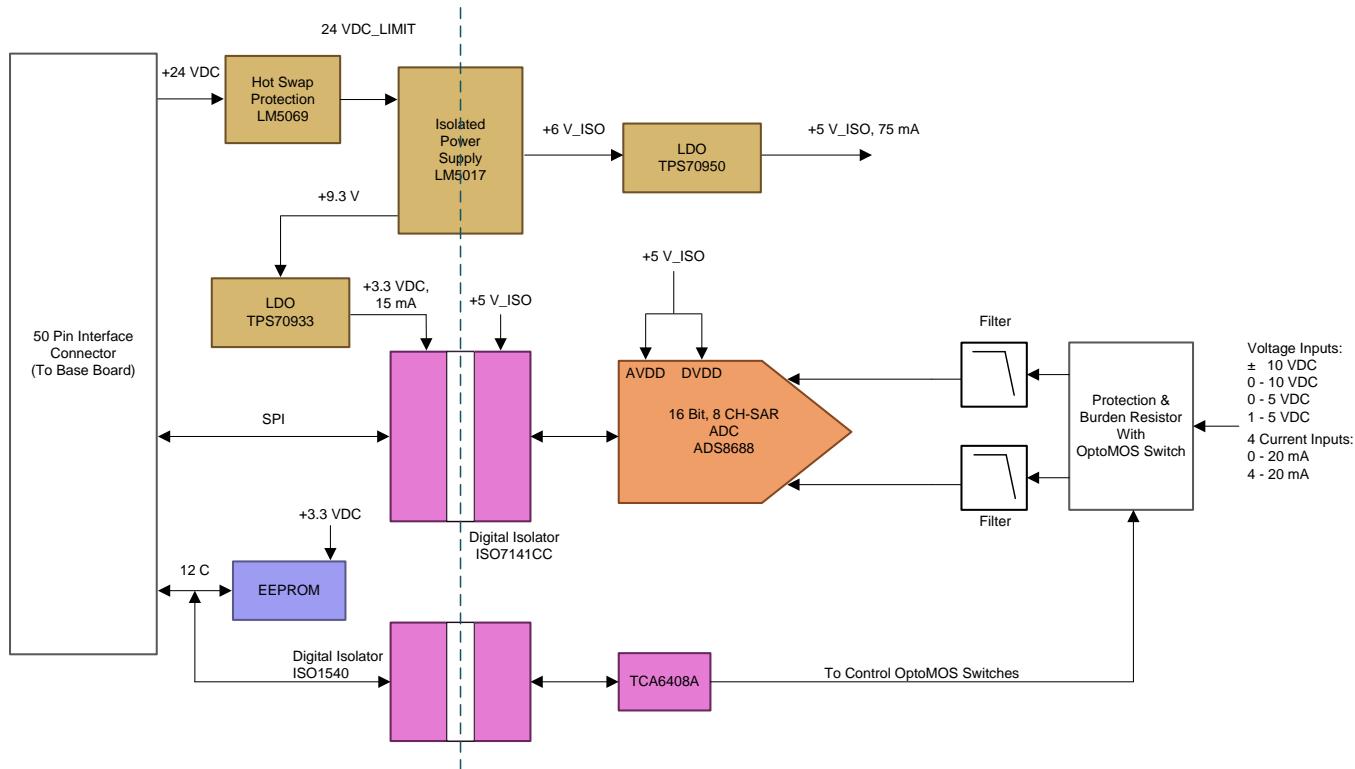


Figure 1. Block-Level Design

4 Highlighted Products

The module has eight analog input channels, and each channel can be configured as a current or voltage input with software configuration. The design uses ADS8688 (16-bit, 8-channel, single-supply SAR ADC) with an on-chip PGA and reference. The on-chip PGA provides a high-input impedance (typically 1 mΩ) and filters noise interference. The on-chip 4.096-V ultralow drift voltage reference is used as the reference for the ADC core.

The digital isolation is achieved using ISO7141 and ISO1541D. The host microcontroller communicates with TCA6408A, an 8-bit I²C I/O expander over an I²C bus. ISO1541D, or bidirectional I²C isolator, isolates the I²C lines for the TCA6408A. The TCA6408A controls the low RON optoswitch (TLP3123), which is used to switch between voltage to current input modes. The input channel configuration is done in microcontroller firmware.

A low-cost constant on-time synchronous buck regulator in Fly-Buck configuration with an external transformer (LM5017) generates the isolated power supply. The LM5017 has a wide input supply range, making it ideal for accepting a 24-V industrial supply. That transformer can accept up to 100 V, thereby making reliable transient protection of the input supply more easily achievable. The Fly-Buck power supply isolates and steps the input voltage down to 6 V. The supply then provides that voltage to TPS70950, the low dropout regulator, to generate 5 V to power the ADS8688 and other circuitry, such as the controller-side nonisolated circuitry. The LM5017 also features a number of other safety and reliability functions, such as undervoltage lockout (UVLO), thermal shutdown, and peak current limit protection.

Input analog signals are protected against high voltage, fast transient events often expected in an industrial environment. The protection circuitry makes use of the transient voltage suppressor (TVS) and ESD diodes. The RC low-pass mode filters have been used on each analog input before the input reaches the ADS8688, which eliminates any high frequency noise pickups and minimizes aliasing.

5 Circuit Design and Component Selection

5.1 ADC

The design uses the ADS8688, a 16-bit, 500-kSPS, 8-Channel, single-supply, SAR ADC. The ADS8688 can operate at a throughput rate of 500 kSPS with no missing code and ± 2.5 LSB. The ADS8688 can accept bipolar and unipolar analog input signals with a single 5-V supply. The single supply operation reduces design complexity and cost. The ADS8688 has five software-selectable input ranges: ± 10.24 V, ± 5.12 V, ± 2.56 V, 0 to 5.12 V, and 0 to 10.24 V. Each analog input channel can be independently programmed to one of the five input ranges. The device offers a $1\text{-M}\Omega$, constant resistive input impedance irrespective of the selected input range. The ADS8688 has an on-chip low-drift reference of 4.096 V, which enables accurate conversion.

The device also offers an integrated front-end signal processing including a multiplexer, second-order anti-aliasing filter, ADC driver amplifier, and an extended industrial temperature range, making the ADS8688 ideal for any standard industrial analog input measurements. The basic block diagram is shown in Figure 2.

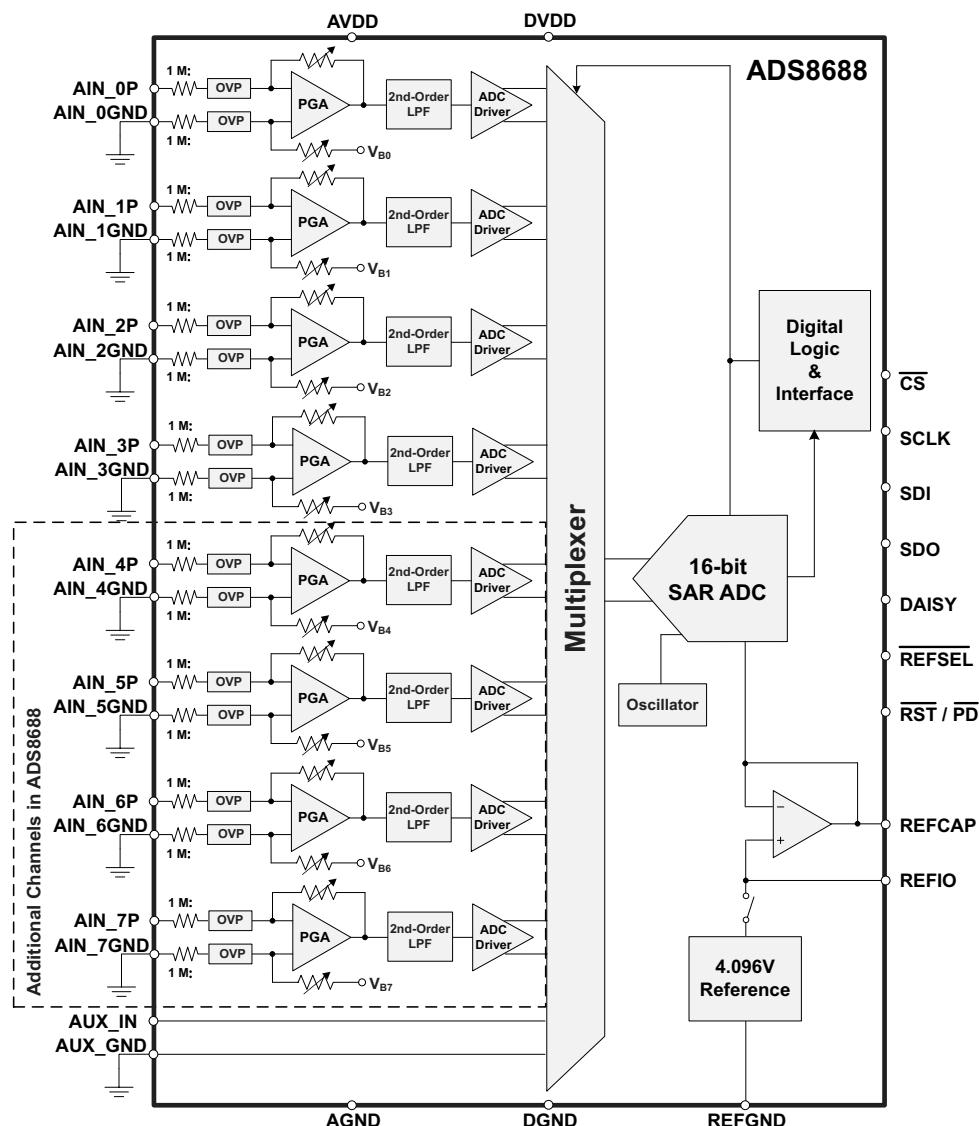


Figure 2. Internal Block Diagram of ADS8688

Table 2. Configuration With On-Chip 4.096-V Reference

ANALOG INPUT RANGE	RANGE_CHN [2:0]		
	BIT 2	BIT 1	BIT 0
$\pm 10.24\text{ V}$	0	0	0
$\pm 5.12\text{ V}$	0	0	1
$\pm 2.56\text{ V}$	0	1	0
0 to 10.24 V	1	0	1
0 to 5.12 V	1	1	0

5.1.1 ADC Reference

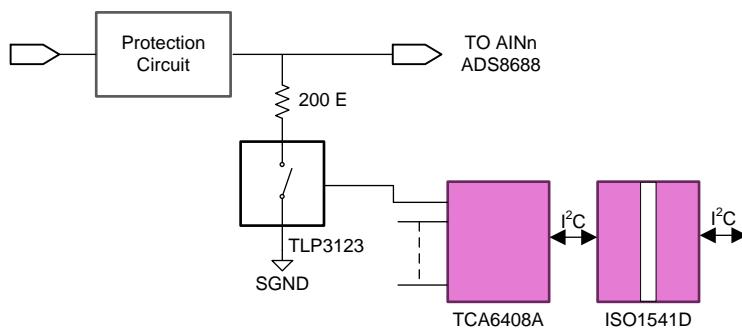
The ADS8688 can operate with on-chip 4.096-V reference or optional external reference. The type of reference used is set by an external /REFSEL pin of ADS8688. This reference design uses the on-chip reference. Also, the external reference is provided with the R80 and R85 resistor combination.

- If R80 is populated and R85 is not populated, ADS8688 operates on internal reference of 4.096 V.
- If R85 is populated and R80 is not populated, connect external reference between TP14 and TP18 (SGND).

The output of the internal reference buffer comes out at the REFCAP pin, which is decoupled with the REFGND pin using a 22- μF and 1- μF capacitor for better performance. The designer should place these decoupling capacitors close to the REFCAP pin of the ADS8688 to shunt the noise to ground and reduce the noise effect on the ADC. A variety of capacitor values in parallel gives a good response to a broad range of noise.

5.1.2 Analog Input and Filter

The ADS8688 contains a terminal block providing connection for eight analog input channels, which are specifically designed to interface with analog current and voltage input signals. For industrial control modules, analog input voltage and current ranges include $\pm 10\text{ V}$, $\pm 5\text{ V}$, $\pm 2.5\text{ V}$, 0 to 5 V, 0 to 10 V, 4 to 20 mA, and 0 to 20 mA. All eight channels provided on the ADS8688 are software configurable as a current or voltage input for the listed industrial voltage ranges. The host microcontroller commands TCA6408A to turn on or off the 200- Ω burden resistance. When the input is set to receive a 4 to 20-mA current, the switches are configured to provide a 200- Ω load resistor on the input, providing 0 to 4 V to the ADC with a full-scale voltage of 5 V.

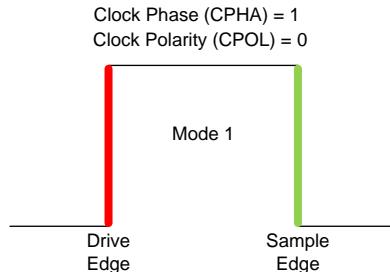
**Figure 3. Analog Input Section**

The ADS8688 on-chip input circuitry consists of eight single-ended analog inputs multiplexed into a single analog-to-digital converter (A/D) core. The A/D reads the selected input signal and converts it to a digital value. The multiplexer sequentially switches each input channel to the ADS8688's A/D. Multiplexing provides an economical means for a single A/D core to convert multiple analog signals. However, on-chip multiplexing also affects the speed at which an input signal can change and still be detected by the converter.

Table 3. SPI Communication with Isolation

ADC clock to DOUT output delay	25 nsec (Max)
Isolator propagation delay	23 nsec (Max) (round delay)
Microcontroller setup time required	17.15 nsec (Min)
Total delay	88.15 nsec

For proper data read, the microcontroller operated in SPI Mode 3. The data is driven on falling edge of the clock cycle and data is read on [Figure 4](#).

**Figure 4. Clock Cycle Data**

Therefore, the maximum SPI clock speed up to which the SPI works with the isolator is 10 MHz.

5.1.2.1 *Input Filter Design*

Table 4. Sampling Time and RC Filter Design

Maximum SPI clock frequency	= 10 MHz
One SPI clock period	= 100 nSec
Time required to read correct 16 bits for one channel (throughput)	= $(33 \times 266 \text{ nSec}) + t_{DV_CSDO}$ = $3.3 \mu\text{Sec} + 10 \text{ nSec}$ = $3.31 \mu\text{Sec}$
Hence sampling frequency	= $\frac{1}{3.31 \mu\text{Sec}}$ = 302ksps
RC low pass filter cut-off frequency \leq Sampling Frequency / 5	= $\frac{300 \text{ kps}}{5}$ = 60kHz
RC low pass filter cut-off frequency f_C	= $\frac{1}{2 \times \pi \times RC}$
R4 = 100 Ω, C12	= 27 nF (standard value)
The R4 and C12 forms RC filter 1, and R21 and C23 form the second RC filter. The dynamic impedance of each filter order affects its neighboring filter. To reduce the loading effect, the designer can make the impedance of each following stage $R \times 10$ and C/10 for the previous stage, so R21 = $10 \times R4$ and C23 = C12/10.	
Consider R21 = 1k, C23	= 2.7 nF (standard value)
The two RC filters forms second-order RC filter. The second-order filter has roll-off 40 dB/Decade for 60 kHz and higher frequencies.	
Setting for the RC low pass filter	= $5 \times R_{FLT}C_{FLT}$ (time constant) = $5 \times (1000 \Omega \times 2.7 \text{ nF})$ = 13 μSec
The external $R_{FLT}C_{FLT}$ low-pass filter network must settle within the next sample acquisition time.	
Sampling time	= $\frac{1}{60 \text{ kHz}}$ = 17 μSec
Settling for the RC low pass filter < Sampling time	

Table 5. Channel Scanning Time

With a moving average of four samples	= $4 \times 17 \mu\text{Sec}$ = $68 \mu\text{Sec}$
Time required to scan all eight channels in ADS8688	= $8 \times 68 \mu\text{Sec}$ = $544 \mu\text{Sec}$

The voltage input has an impedance of $1 \text{ M}\Omega$; when the current input is set to 300Ω , the burden resistor is switched on using Opto-MOS with low on-state resistance.

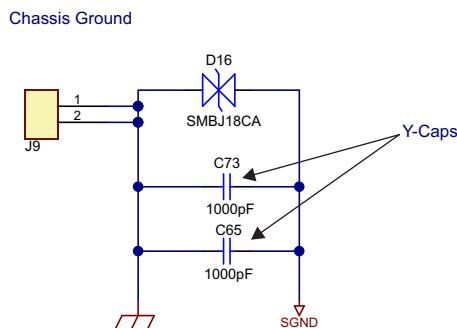
5.1.3 Protection for ESD, EFT, and Surge

The goal of EMC-protected circuitry is to shunt any sort of external transient to earth ground with low impedance and protect the analog input module from damage. The circuit includes standard external protections and has been tested and verified to fully comply with the specifications listed in [Table 6](#).

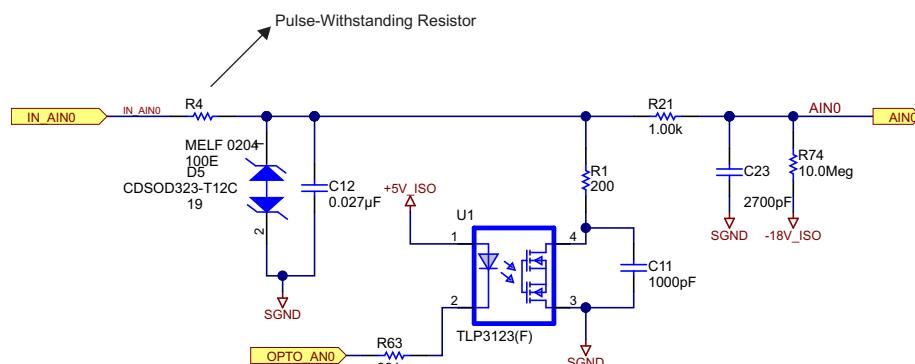
Table 6. IEC 61000 Specifications

TEST AND STANDARD	TEST LEVEL
IEC 61000-4-2: ESD	$\pm 4 \text{ kV}$ contact discharges $\pm 8 \text{ kV}$ air discharges
IEC 61000-4-4: Burst-EFT	$\pm 2 \text{ kV}$ at 5 kHz on signal ports
IEC 61000-4-5: Surge	$\pm 1 \text{ kV}$ CM on signal ports

The TVS diodes are used to clamp the surge voltage to safer limits with high-voltage capacitor Y-caps in parallel. In addition, two Y-caps have been placed at key locations to shunt transient energy quickly to earth ground. The Y-caps provide quick and low impedance to fast transients, and TVS diodes provide immunity against high voltage spikes.

**Figure 5. Y-Caps Placements**

The voltage surge has the highest energy. To demonstrate this, consider the case of 1 kV (CM) at $8/20 \mu\text{s}$ surge on input lines and calculate.

**Figure 6. Schematic of ADC Circuitry**

To find the impedance in path, see [Table 7](#).

Table 7. Z_{TOTAL} Value

Z_{TOTAL}	$= Z_{SURGE_GENERATOR} + Z_{CDN_NETWORK} + R_{SERIES_RESISTOR}$
	$= 2 \Omega + 40 \Omega + 100 \Omega$
	$= 142 \Omega$

The internal overvoltage protection circuit of ADS8688 can withstand up to ± 20 V on the analog input pins. Therefore, clamping voltage must be less than 20 V. The CDSOD323-T12SC rating provides the following values: $V_{BR} = 13.3$ V, $V_{CMAX} = 27.3$ V at 8/20 μ s with $I_{PP} = 14$ A, $PPP = 350$ W, and maximum leakage current = 1 μ A.

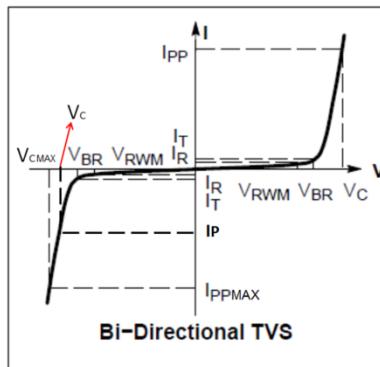


Figure 7. Bi-Directional TVS

Linear or straight line equation V_C :

$$= \frac{I_p}{I_{PP}} (V_C - V_{BR}) + V_{BR} \quad (1)$$

$$I_p = \frac{(1000 \text{ V} - V_C)}{Z_{TOTAL}} \quad (2)$$

$$= \frac{(1000 \text{ V} - V_C)}{142 \Omega} \quad (3)$$

Put I_P in the equation of V_C and solve the equation from [CDSOD323-T12SC data sheet](#) values.

Table 8. V_C and Pulse Power Dissipation Values

V_C	$= 20 \text{ V}$
Pulse Power Dissipation P_P	$= V_C \times I_p$
	$= 20 \times 6.9 \text{ A}$
	$= 138 \text{ W}$

5.2 Power Supply and Isolation Design

The LM5069 positive voltage hot swap controller provides intelligent control of the power supply connections during insertion and removal of a module from a live system or power source. The LM5069 provides inrush current limiting during activation and monitors the load current for faults during normal operation.

Additional LM5069 functions include undervoltage lockout (UVLO) and overvoltage lockout (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current of the module is limited to 2.75 A. The current limit and power dissipation in the external series pass N Channel MOSFET are programmable, ensuring operation within the safe operating area (SOA).

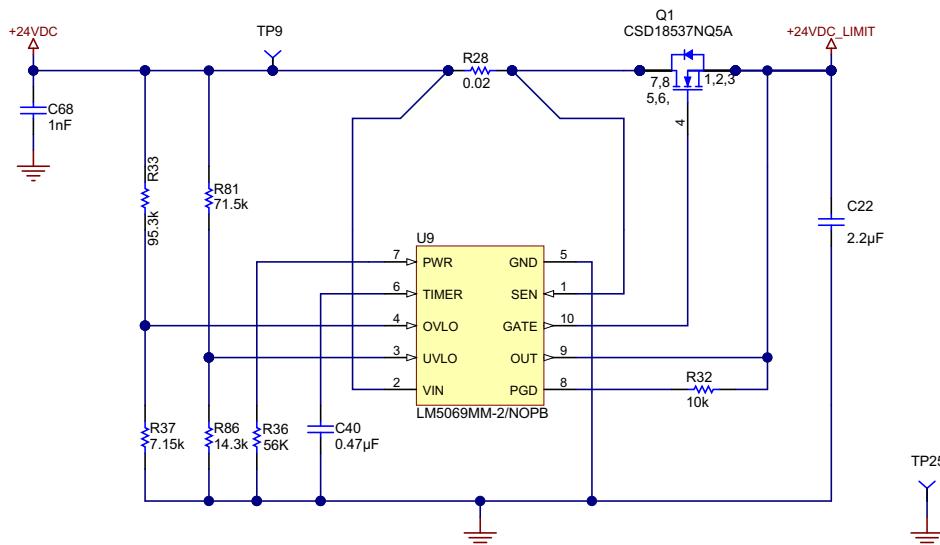


Figure 8. Current Limiter

The desired current limit threshold:

$$I_{LIM} = \frac{55 \text{ mV}}{R_{28}} = \frac{55 \text{ mV}}{20 \text{ m}\Omega} = 2.75 \text{ A} \quad (4)$$

For proper operation of the device, sense resistor R28 must be smaller than 100 mΩ.

NOTE: Current sense resistor (R28) must be placed close to LM5069. Connections from R28 to LM5069 should be made using Kelvin techniques (see [Figure 9](#)).

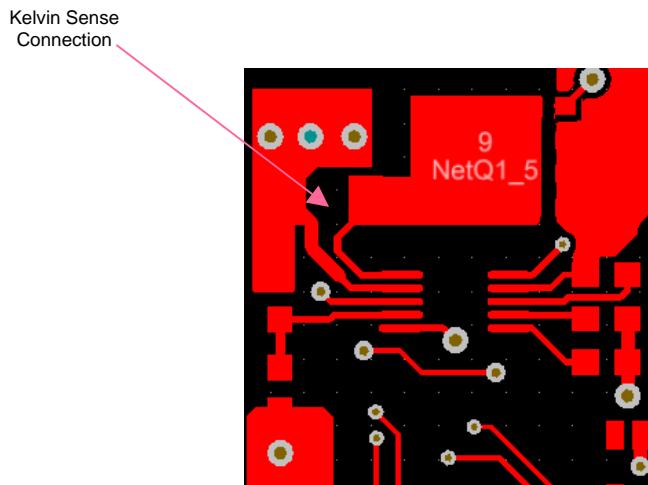


Figure 9. Kelvin Sense Connection for Sense Resistor

5.2.1 UVLO and OVLO

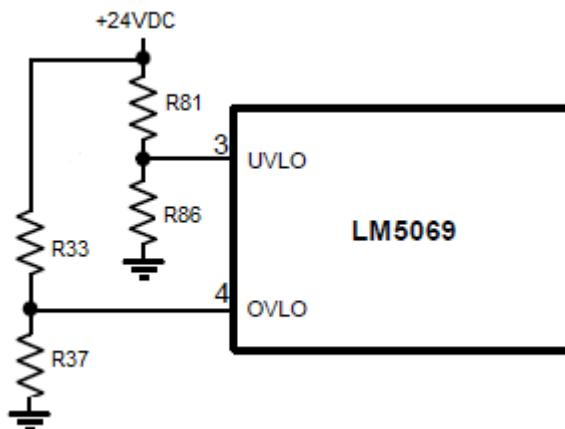


Figure 10. UVLO and OVLO Using External Resistors

To define all four thresholds accurately, this design uses four resistors for UVLO and OVLO.

Upper and lower UVLO thresholds:

$$R81 = \frac{V_{UVH} - V_{UVL}}{21 \mu\text{A}} = \frac{1.5 \text{ V}}{21 \mu\text{A}} = 71.42 \text{ K} \text{ (standard value)} \quad (5)$$

$$R86 = \frac{2.5 \text{ V} \times R81}{V_{UVL} - 2.5 \text{ V}} = \frac{2.5 \times 71.5 \text{ K}}{15 \text{ V} - 2.5 \text{ V}} = 14.3 \text{ K} \quad (6)$$

Therefore, $V_{UVH} = 16.50 \text{ V}$ and $V_{UVL} = 15 \text{ V}$, with a hysteresis of 1.5 V that keeps the device from responding to power-on glitches during start up.

Choose the upper and lower OVLO thresholds:

$$R33 = \frac{V_{OVH} - V_{OVL}}{21 \mu\text{A}} = \frac{2 \text{ V}}{21 \mu\text{A}} = 95.3 \text{ K} \quad (7)$$

$$R37 = \frac{2.5 \text{ V} \times R2}{V_{OVH} - 2.5 \text{ V}} = \frac{2.5 \text{ V} \times 95.3 \text{ K}}{36 \text{ V} - 2.5 \text{ V}} = 7.11 \text{ K} = 7.15 \text{ K} \text{ (standard value)} \quad (8)$$

Therefore, $V_{OVH} = 35.82 \text{ V}$ and $V_{OVL} = 33.82 \text{ V}$, with a hysteresis of 2 V.

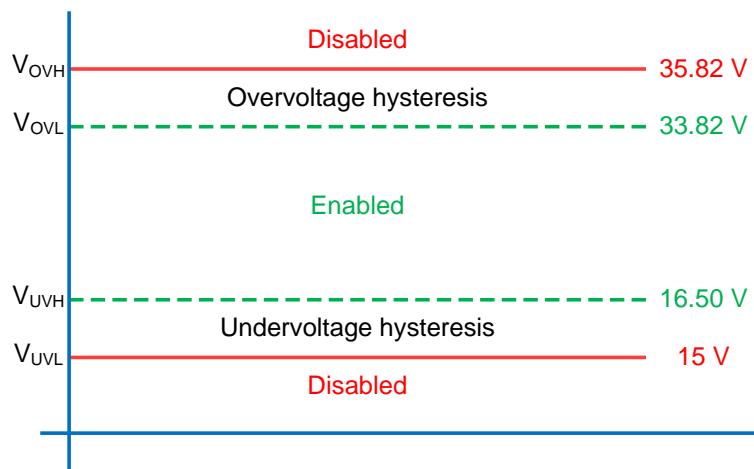


Figure 11. UVLO and OVLO Hysteresis

Refer to [LM5069 data sheet](#) and [LM5069EVAL evaluation board](#) for device operations, design procedures, and recommended PCB layout guidelines.

In industrial systems, signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. Isolation also avoids ground loop. The LM5017 is a synchronous buck regulator with integrated MOSFET.

The LM5017 is configured in Fly-Buck topology to generate nonisolated 3.3 V and isolated 5 V, 18 V from 24-V DC. An isolated Fly-Buck converter uses a coupled inductor windings to generate isolated outputs. In flyback topology there is no need for an Opto-coupler or auxiliary winding as the secondary output closely tracks the primary output voltage, resulting in cost effective and smaller size solution.

Table 9. Specifications for LM5017

SR. NO.	DESIGN SPECIFICATIONS	
1	Input Voltage Range (V_{IN})	16 to 35 V
2	Primary Output Voltage (V_{OUT1})	10 V (3.3 V after LDO)
3	Secondary Output Voltage (V_{OUT2})	5 V
4	Primary Load Current (I_{OUT1})	30 mA
5	Secondary Load Current (I_{OUT2})	120 mA
6	Switching Frequency (fsw)	1 MHz

The nonisolated output voltage ($V_{CC_NON_ISO}$) is set by two external resistors (R3, R70). The regulated output voltage is calculated as follows:

$$V_{CC_NON_ISO} = 1.225 \times \left(1 + \frac{R70}{R3}\right) = 1.225 \times \left(1 + \frac{196\text{ K}}{28\text{ K}}\right) = 10\text{ V} \quad (9)$$

The operating frequency can be calculated as follows:

$$f_{SW} = \frac{V_{OUT}}{10^{-10} \times R_{ON}} \quad (10)$$

$$R_{ON} = \frac{10\text{ V}}{10^{-10} \times 1\text{ MHz}} = 100\text{ K}\Omega \quad (11)$$

Minimum recommended on-time is 100 ns at maximum input voltage:

$$T_{ON_MAX} = \frac{10^{-10} \times R_{ON}}{V_{IN_MIN}} = 0.67\text{ }\mu\text{s} \quad (12)$$

Similarly,

$$T_{ON_MIN} = \frac{10^{-10} \times R_{ON}}{V_{IN_MAX}} = 0.29\text{ }\mu\text{s} \quad (13)$$

$V_{CC_NON_ISO}$ is given to TPS70933DBVT LDO that generates 3.3 V_NON_ISO and capable of delivering 30 mA of output current. The 3.3 V_NON_ISO is used to power-up an EEPROM and two digital isolators.

5.2.2 Selection of Rectifier Diode D2

The reverse bias voltage across D2 when the high side buck switch is calculated as follows:

$$V_{D2} = \frac{N_{sec}}{N_{pri}} \times V_{IN_MAX} = \frac{1}{1.55} \times 35 = 23 \text{ V} \quad (14)$$

Considering safety margins, the PIV of secondary diode should be greater than 35 V. Therefore, the 60-V Schottky diode PMEG6010CEH,115 is selected.

Rectified output (+VCC_ISO) on the secondary side is calculated as follows:

$$+VCC_ISO = \left(\frac{N_{sec}}{N_{pri}} \times V_{CC_NON_ISO} \right) - VFD2 = 6.45 - 0.4 \text{ V} = 6.05 \text{ V} \quad (15)$$

D4 is connected to generate -18V_ISO, which is used to detect sensor open condition. The load current of -18V_ISO rail is negligible as compared to 5V_ISO.

Refer to [LM5017 data sheet](#) for device operation and [AN-2292](#) for Fly-Buck converter design procedures and recommended PCB layout guidelines.

It is generally not recommended to power-up ADCs directly from switching regulator's output as the ADC contains ripple noise due to switching frequency. The ADC contains high frequency noise due to rapid transitions in the voltage or currents. Applying noise directly to ADC would kill the performance. Therefore, practice powering up ADCs from low noise LDO with high PSRR.

The LDO selected for the design is TPS70950DBVR. The LDO has a wide input voltage range up to 30 V and has 50-dB PSRR at 1 MHz (80 dB for lower frequencies). Therefore, the ripple noise from the switching regulator can adequately be attenuated by TPS70950DBVR. Typically, PSRR of LDOs is high at lower frequencies, tends to decrease at higher frequencies and becomes zero above few MHz. The TPS70950DBVR has better PSRR at higher frequencies. The TPS70950DBVR eliminates the need for a bulky LC filter.

Table 10. Design Considerations for TPS70950DBVT

SR. NO.	DESIGN SPECIFICATIONS AND KEY PARAMETERS	
1	Input Voltage Range (V_{IN})	6.2-V DC
2	Output Voltage (V_{OUT})	5 V (Fixed)
3	Output current (I_{OUT})	120 mA
4	V_{DO}	295 to 650 mV
5	Thermal shutdown at	158°C
6	T_{J_MAX}	125°C
7	θ_{JA} Junction-to-ambient thermal resistance	212.1°C / W

5.2.3 Input and Output Capacitors

TPS70950 is stable with minimum output capacitance of 1.5 μF . The 10- μF X5R ceramic capacitor is connected for better stability over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- μF to a 2.2- μF capacitor from V_{IN} to GND. The design uses a 1- μF capacitor connected at the input. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR.

5.2.4 Thermal Protection

Thermal protection in TPS70950 disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled.

5.2.5 Power Dissipation

Power Dissipation and Temperature Values

Pulse Power Dissipation P_P	= $(V_{IN} - V_{OUT}) \times I_{OUT}$ = $(6.2 - 5) \times 120 \text{ mA}$ = 144 mW
T_J	= $TA(\max) + (\theta_{JA} \times PD)$ = $70 + (212.1 \times 144 \text{ mW})$ = 100.54°C

Therefore, the TPS70950 does not need a heat sink.

See the [TPS70950 data sheet](#) for device operation and recommended PCB layout guidelines.

5.2.6 Digital Isolation

In industrial systems, signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. The high speed digital isolators ISO7141CC and ISO1541D connect the SPI host to the ADS8688 SPI. With these digital isolators, the host processor on the base board maintains 2.5 kVRMS of galvanic isolation for one minute for any high voltage condition appearing at the analog input module from the field side.

The ISO7141CC isolates SCLK, MISO, MOSI, and /CS signals of SPI. The ISO1541D isolates SDA and SCL signals of I²C. Both the products have achieved UL, CSA, and VDE safety approvals.

5.3 Interface

The analog input board has the following connectors:

1. J1 to J8: 2-pin screw terminal type 2.54-mm pitch connectors for interfacing external analog inputs
2. J9: 2-pin screw terminal type 2.54-mm pitch connectors for connecting protective earth
3. J10: 50-pin connector for connecting SPI, I²C, and power supply from the host controller

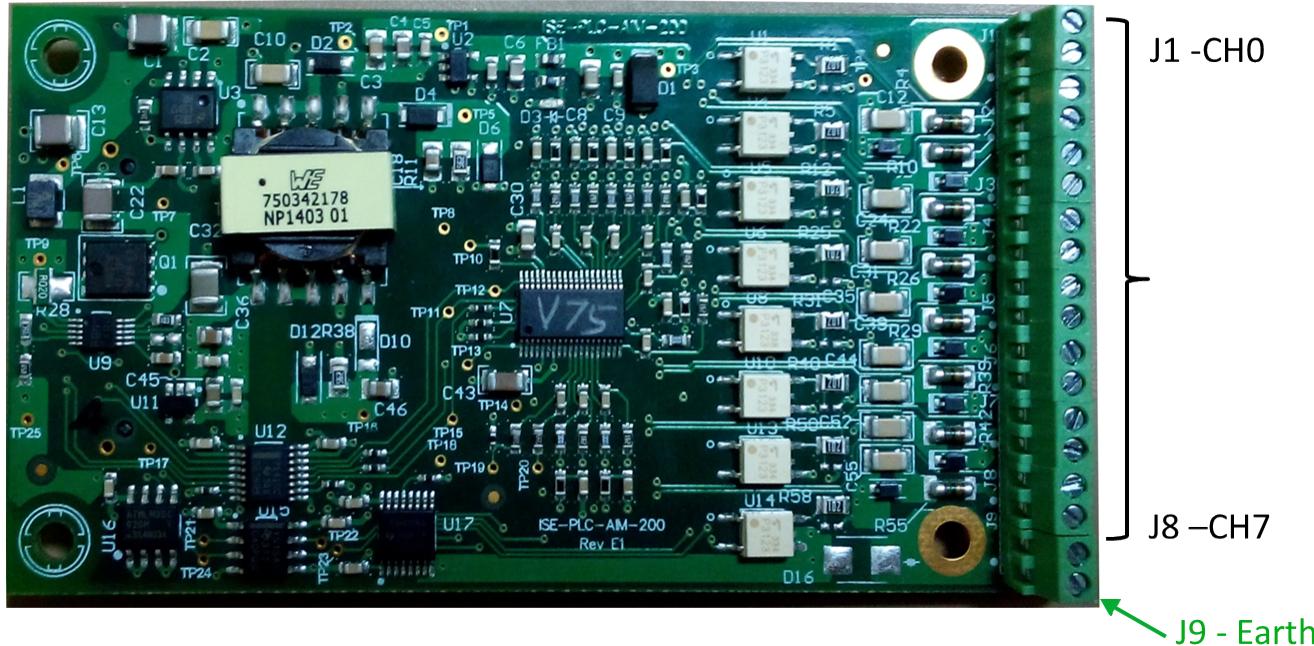


Figure 12. Top View

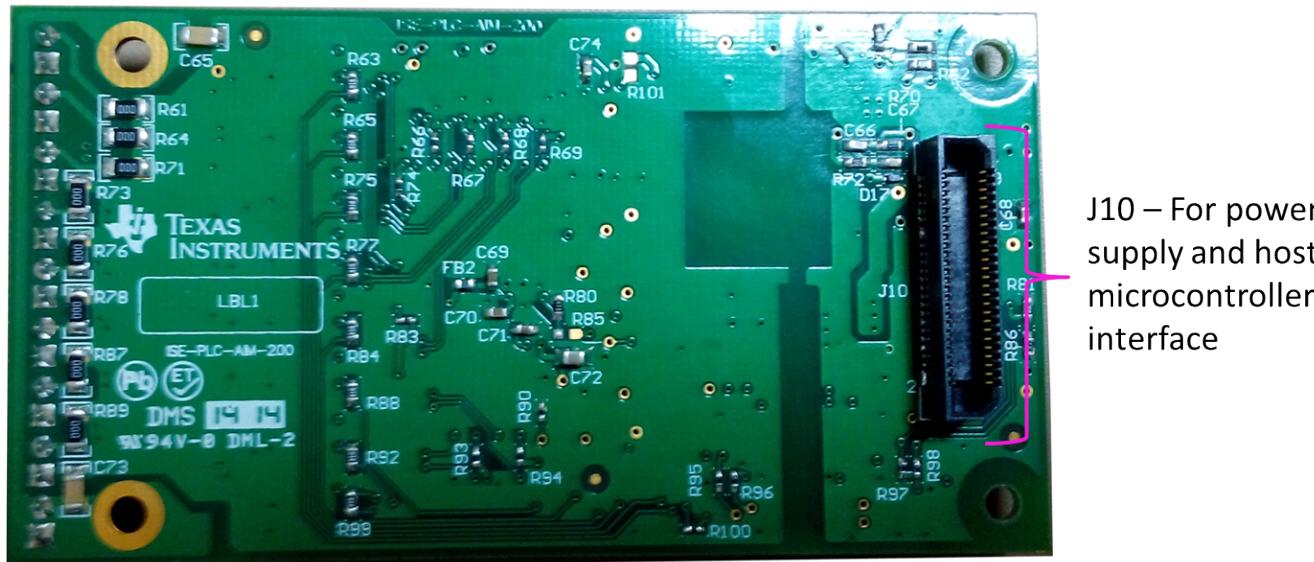


Figure 13. Bottom View

6 Test Setup

6.1 Hardware Test Setup

The Tiva C Series I/O Controller Platform has the required connectors and the MCU to interface with the analog input module. A 24-V power input to the analog input module is supplied by the Tiva C Series I/O Controller Platform.

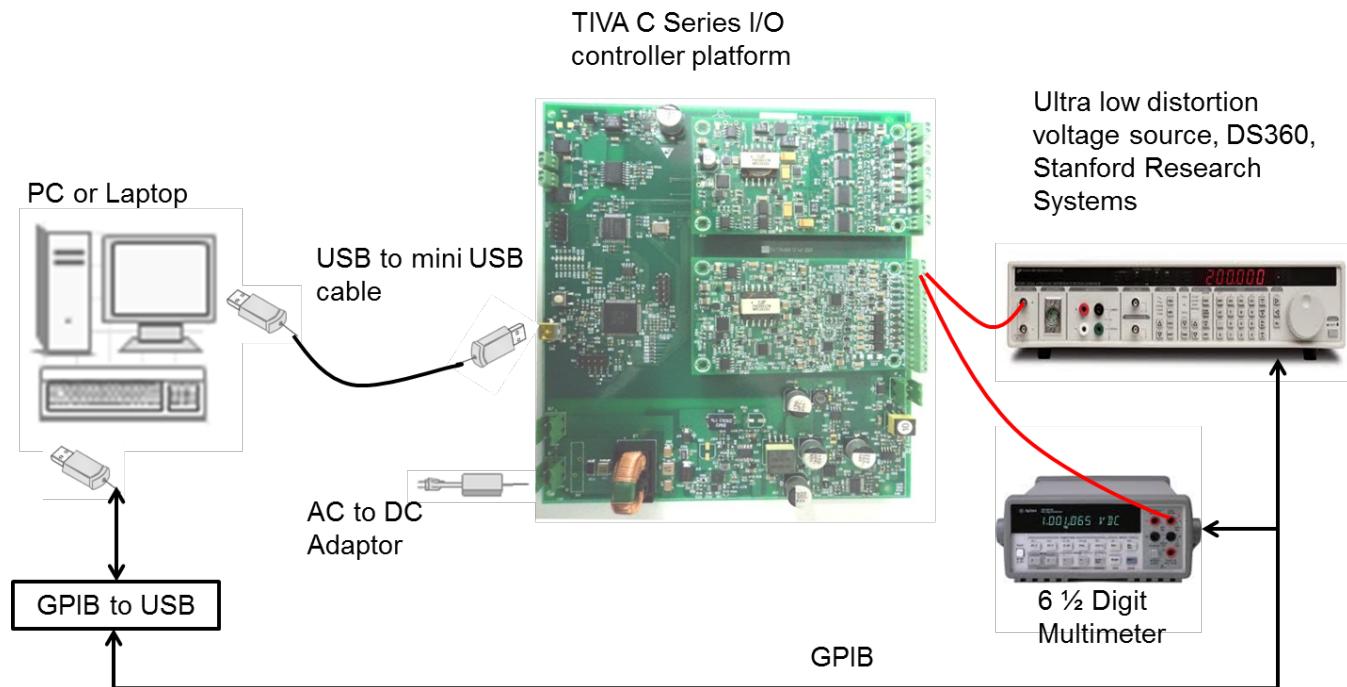


Figure 14. Test Configuration

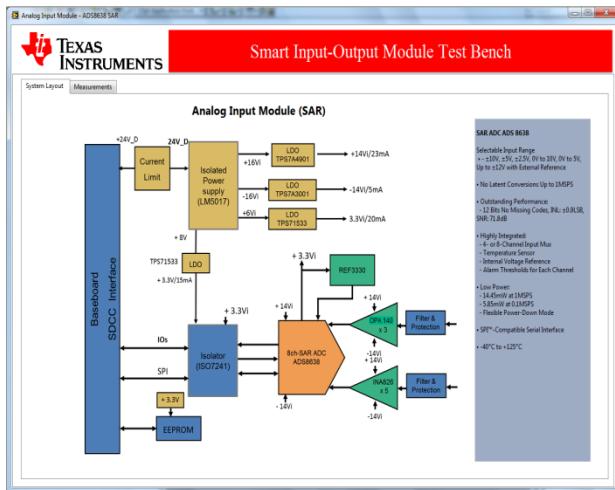


Figure 15. GUI to Demonstrate the Signal Chain Information

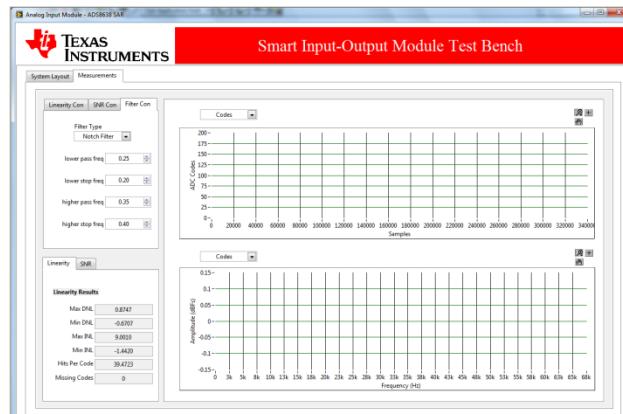


Figure 16. GUI to Demonstrate the Results

The complete signal chain performance can be evaluated using LabView-based GUI. The GUI on the PC connects to the Tiva C Series I/O Controller Platform through a USB interface. The Tiva C Series I/O Controller Platform then controls the analog input card via SPI. The setup has a precision signal generator (DS360, Stanford Research Systems), which feeds the analog input signal to the analog input module. The same signal is read by a 6 ½-digit multimeter. The digital output generated is measured by the Tiva C Series I/O Controller Platform. The GUI does the post processing and computation of results.

The GUI is LabView-based software. The GUI can set the following functions:

- Configures all the registers in the ADS8688
- Configures channel for voltage or current input
- Reads the digitized data from the module
- Posts processing of the data
- Creates result options: SNR, ENOB, DNL, and INL

7 Test Results

7.1 Typical Performance Characteristics

Figure 17 through Figure 25 show the results produced from the Smart I/O Module Test Bench, shown in Figure 16.

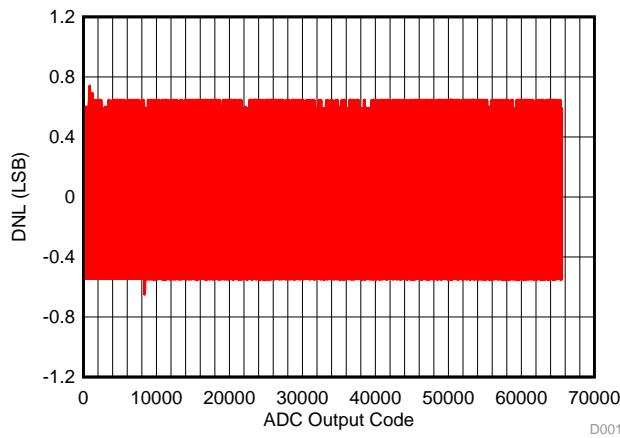


Figure 17. DNL Plot (Input Range: ± 10 V)

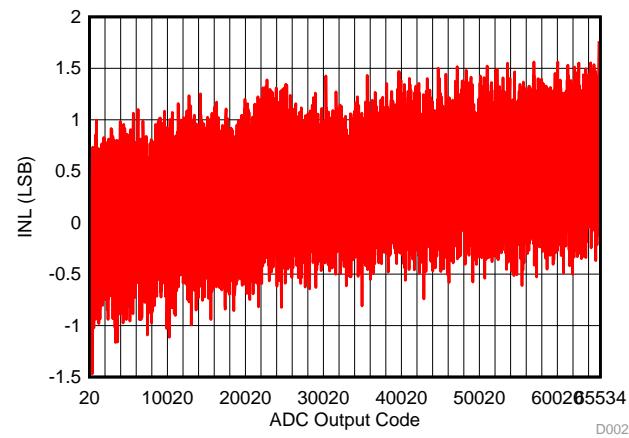


Figure 18. INL Plot (Input Range: ± 10 V)

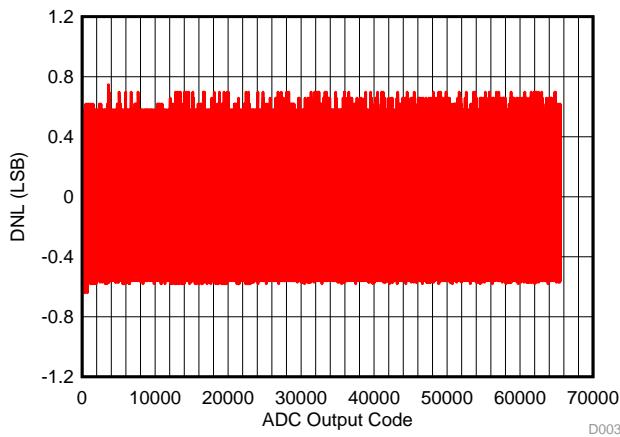


Figure 19. DNL Plot (Input Range: 10 V)

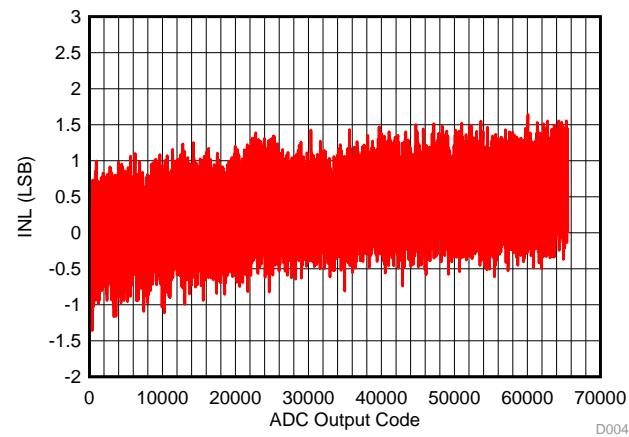


Figure 20. INL Plot (Input Range: 10 V)

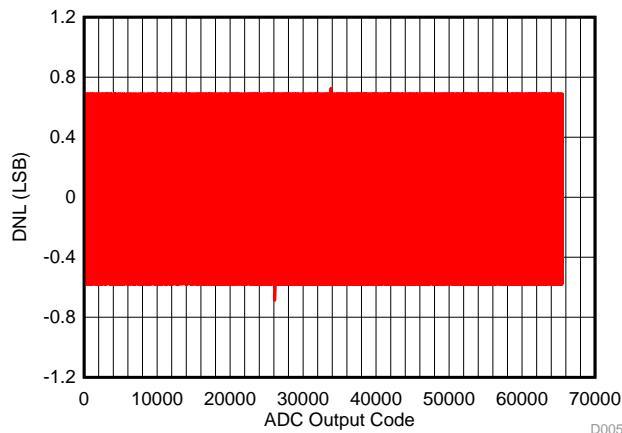


Figure 21. DNL Plot (Input Range: 5 V)

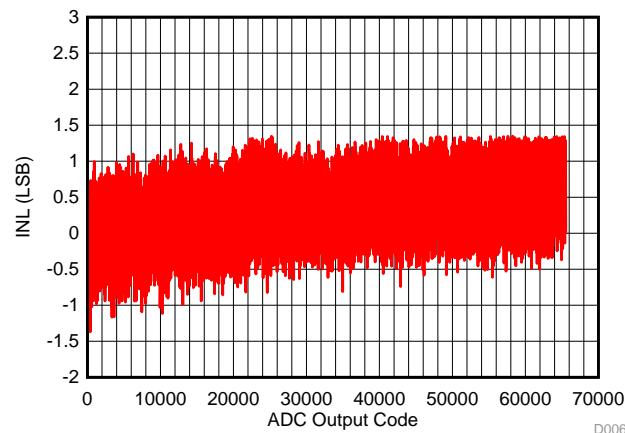


Figure 22. INL Plot (Input Range: 5 V)

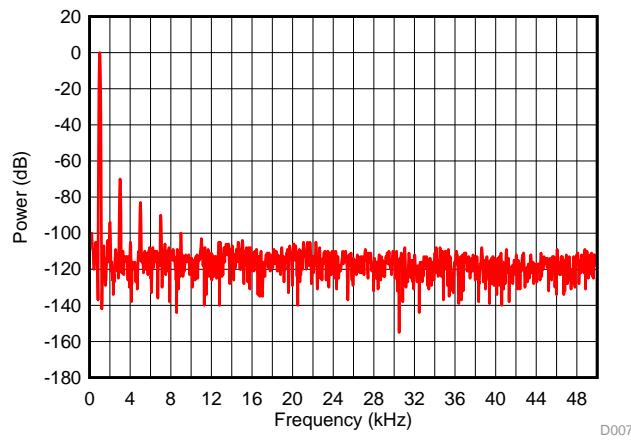


Figure 23. SNR (Input Range: ±10 V)

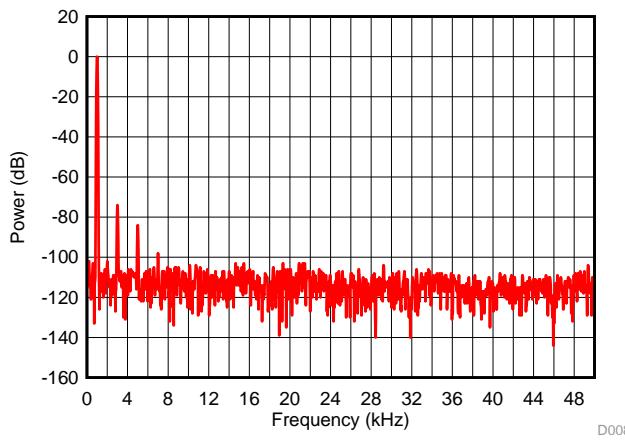


Figure 24. SNR (Input Range: 0 to 10 V)

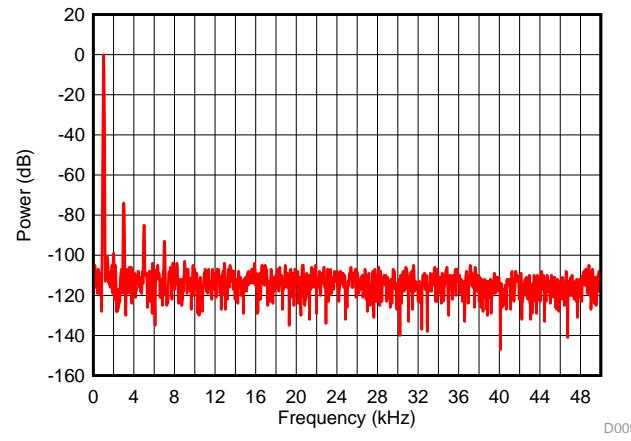


Figure 25. SNR (Input Range: 0 to 5 V)

7.2 Accuracy Test Results

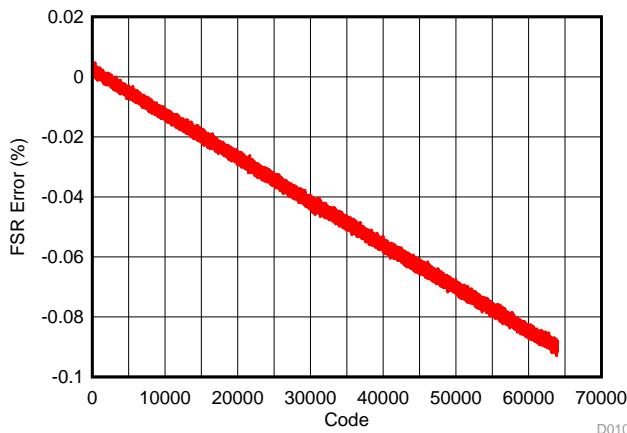


Figure 26. 0 to 5-V Range, Code versus FSR Error (%) Before Calibration

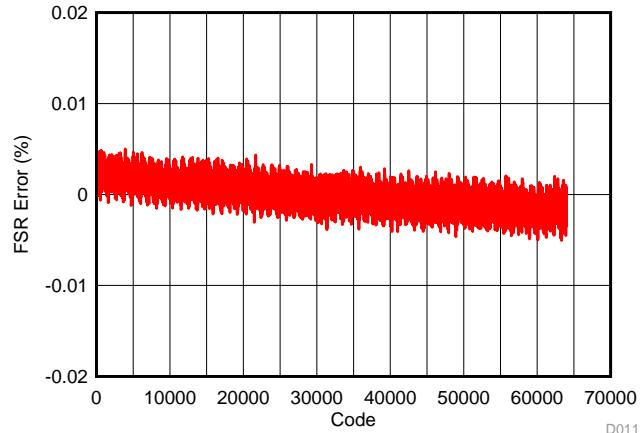


Figure 27. 0 to 5-V Range, Code versus FSR Error (%) After Calibration

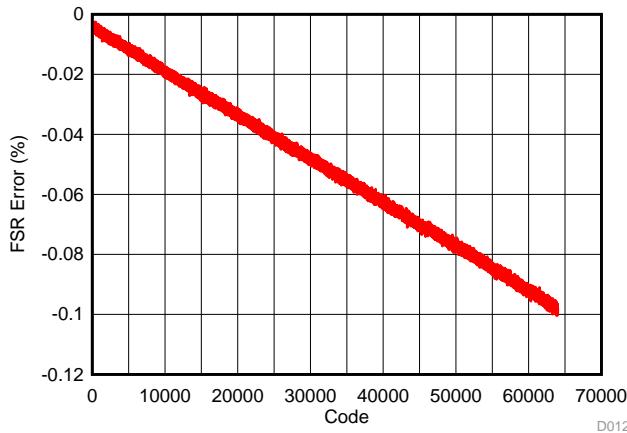


Figure 28. 0 to 10-V Range, Code versus FSR Error (%) Before Calibration

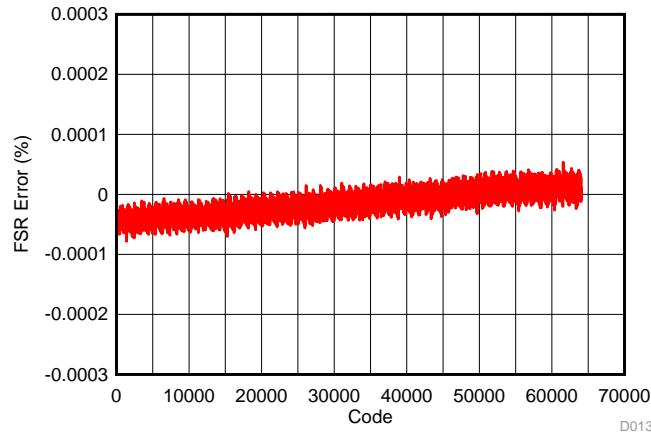


Figure 29. 0 to 10-V Range, Code versus FSR Error (%) After Calibration

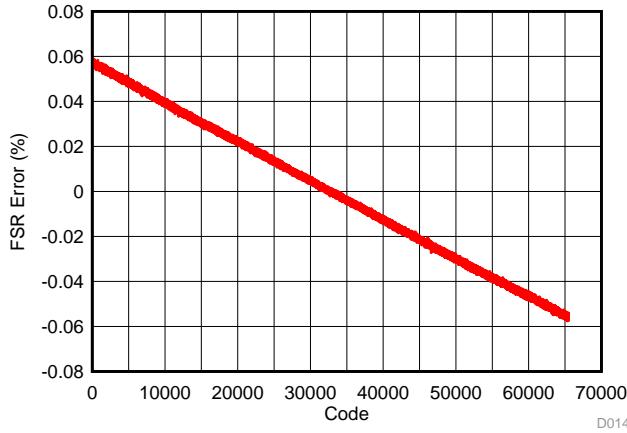


Figure 30. ±10-V Range, Code versus FSR Error (%) Before Calibration

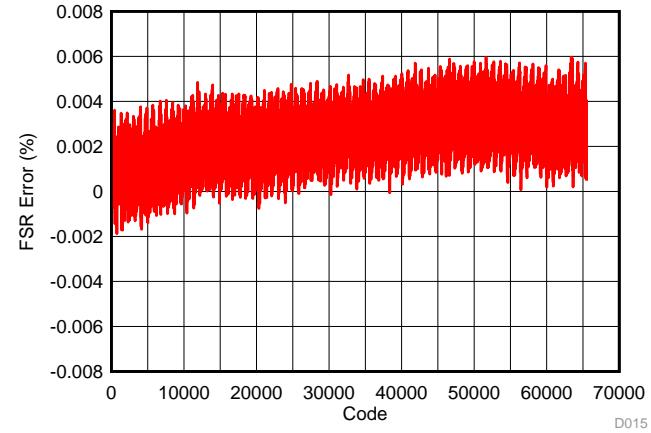


Figure 31. ±10-V Range, Code versus FSR Error (%) After Calibration

7.3 Results Summary

Table 11. Measurement Results Summary

SR. NO.	PARAMETER	±10-V RANGE	10-V RANGE	5-V RANGE	ADS 8688 Specifications
1	SNR	90.85	89.52	88.48	88 to 92(dB)
6	Max DNL	0.74	0.75	0.73	−0.6 to 0.7 (LSB)
7	Min DNL	−0.65	−0.64	−0.69	
8	Max INL	1.77	1.64	1.35	−1.4 to 1.7 (LSB)
9	Min INL	−1.47	−1.36	−1.37	

7.4 Precompliance Testing

The analog input module has been designed to meet standard EMC requirements for industrial PLC application.

The following EMC tests have been performed:

Table 12. EMC Tests and Standards

TESTS	STANDARDS
ESD	IEC61000-4-2
EFT	IEC61000-4-4
Surge	IEC61000-4-5

Table 13. Criteria and Performance as Per IEC61131-2

CRITERIA	PERFORMANCE (PASS) CRITERIA
A	The analog output module shall continue to operate as intended. The module has no loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the analog output module shall continue to operate as intended without manual intervention.
C	During the test, a loss of functions is accepted, but not the destruction of hardware or software. After the test, the analog output module shall continue to operate as intended automatically after a manual restart or power off/power on.

The targeted accuracy for criteria A is as follows:

- Voltage input: ±0.2% full scale at 25°C
- Current input: ±0.2% full scale at 25°C

The next sections explain the test setup, procedures, and observations.

7.4.1 Test Setup



Figure 32. Precompliance Test Setup

7.4.2 ESD: IEC61000-4-2

7.4.2.1 Test Level and Expected Performance

The ESD level at I/O connectors and the performance criteria expected are as follows:

Table 14. ESD Test Settings

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE (PASS) CRITERIA
ESDIEC 61000-4-2	4-kV contact discharges – Level 2 8-kV air discharges – Level 3	Criteria B

7.4.2.2 Setup Description

The ESD is injected to the EUT in two ways: contact discharge or air discharge.

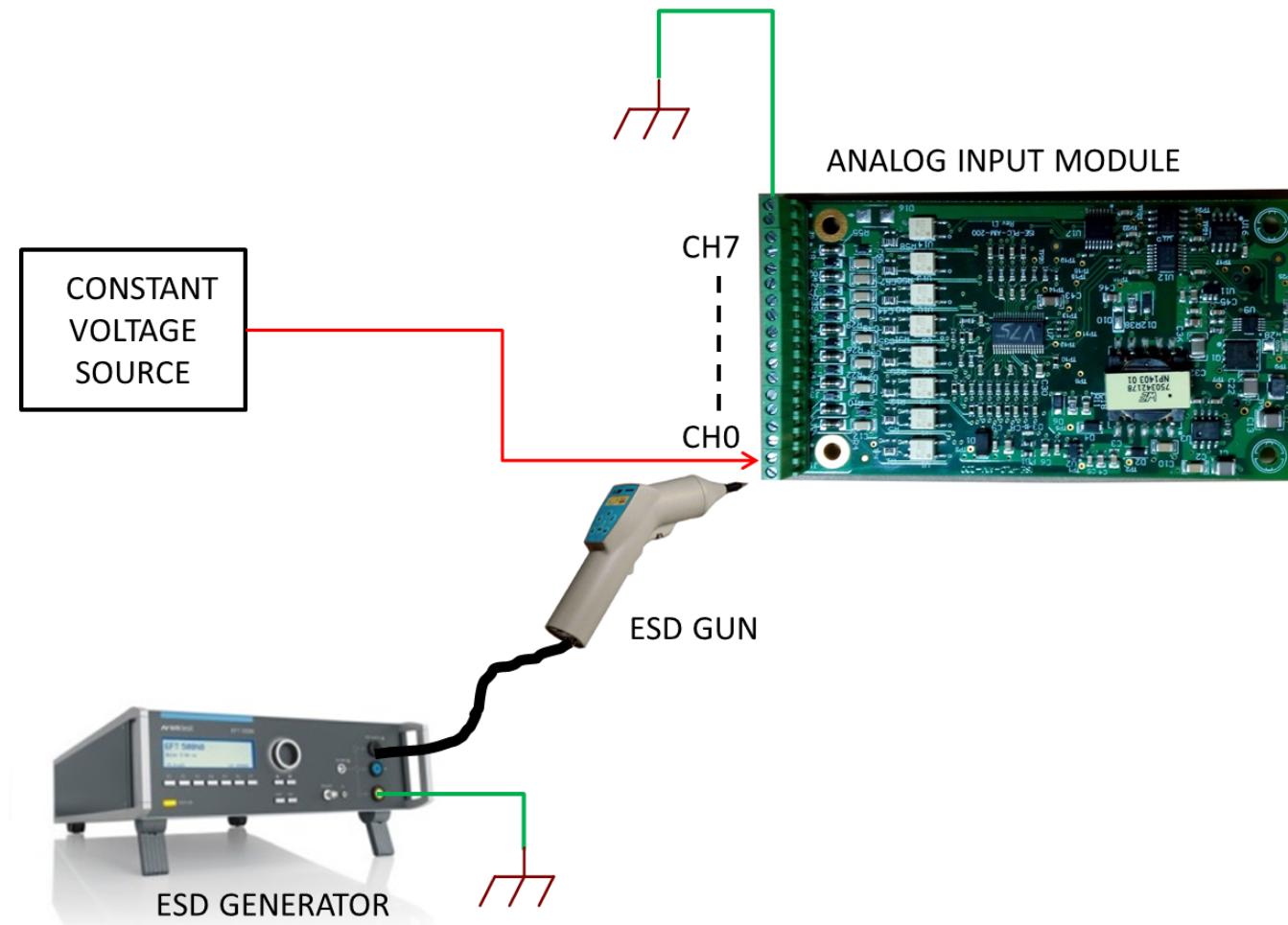


Figure 33. ESD Test Setup

The EUT is placed on a horizontal coupling plane (HCP) of 160 x 80-cm dimensions on top of a wooden table 80-cm high and located above the ground reference plane. The EUT and its attached cables were isolated from the HCP by a thin insulating support of 0.5-mm thickness. ESDs were applied using an ESD gun directly (via contact or air discharges) or indirectly (via an HCP). The EUT operation was monitored after the test. The EUT is tested in active mode using unshielded 3-m cables on I/O ports.

7.4.2.3 Monitoring Methods

- Connect the EUT as shown in [Section 7.4.2.2](#). The shield pin is connected to local earth, the same as the test generator
- Power on the EUT
 - The test software is configured to check the analog input for level with in a tolerance limit of 0.2%
 - If the input level exceeds the tolerance limit, the LED on the I/O controller toggles
- Set the voltage level to 3-V DC and current level
- The ESD test is performed as shown in [Table 15](#)
- After the test is performed, conduct a performance test to check the degradation
- Repeat the test by changing the input voltage level to 6-V DC

7.4.2.4 ESD Test Results
Table 15. ESD Test Results

TEST NO.	TEST MODE	OBSERVATION
1	Air 2 kV	Pass
2	Air -2 kV	Pass
3	Air 4 kV	Pass
4	Air -4 kV	Pass
5	Air 6 kV	Pass
6	Air -6 kV	Pass
7	Air 8 kV	Pass
8	Air 8 kV	Pass
9	Contact 1 kV	Pass
10	Contact -1 kV	Pass
11	Contact 2 kV	Pass
12	Contact -2 kV	Pass
13	Contact 4 kV	Pass
14	Contact -4 kV	Pass
15	HCP 2 kV	Pass
16	HCP -2 kV	Pass
17	HCP 4 kV	Pass
18	HCP -4 kV	Pass
22	HCP -4 kV	Pass

7.4.3 EFT: IEC61000-4-4

7.4.3.1 Test Level and Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are shown in [Table 16](#).

Table 16. EFT Test Settings

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE (PASS) CRITERIA
EFT/B IEC 61000-4-4	$\pm 2 \text{ kV}$ at 5 kHz, 100 kHz on signal ports	Criteria A

7.4.3.2 Setup Description

The burst signal is injected on all cables together using a capacitive coupling clamp. EUT is connected to auxiliary sources by unshielded cables. The lengths of the cables are set to 3 m and cables are placed 10 cm above the reference plane. The test is carried out with the EUT placed 10 cm above the reference plane on insulating material, and with the EUT placed on the reference plane.

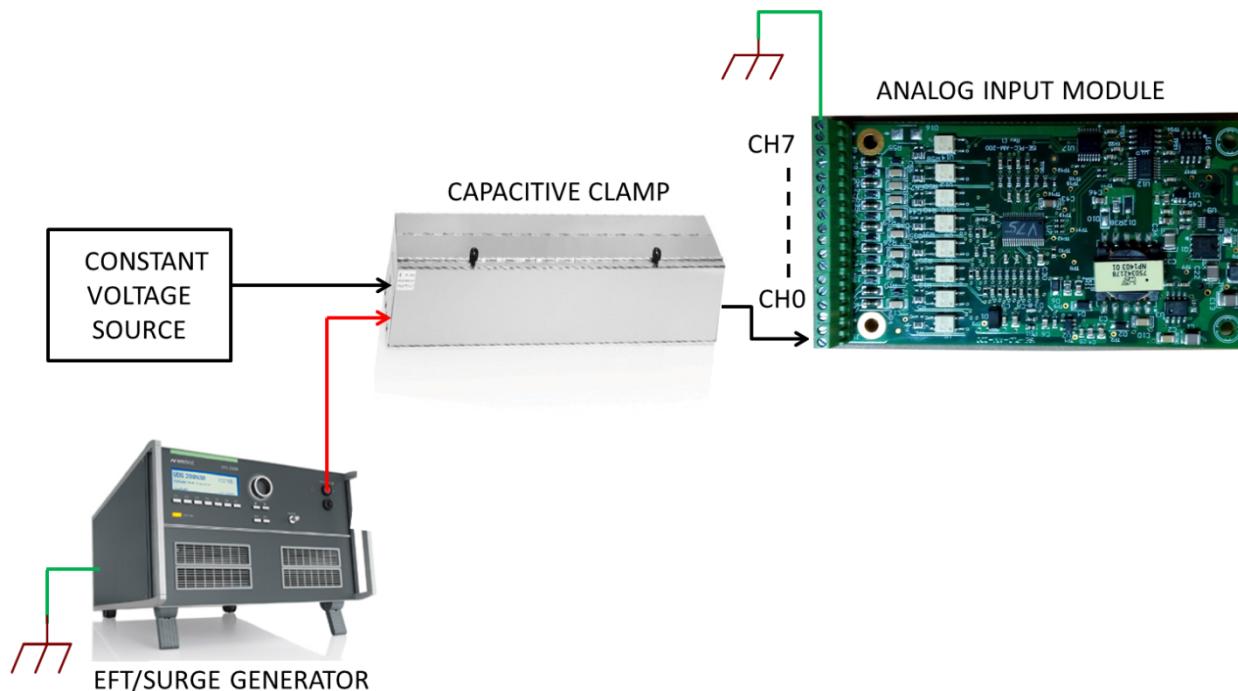


Figure 34. EFT Test Setup

7.4.3.3 Monitoring Methods

- Connect the EUT as shown in [Section 7.4.3.2](#). The shield pin is connected to local earth, the same as the test generator
- Power on the EUT
 - The test software is configured to check the analog input for level within a tolerance limit of 0.2%
 - If the input level exceeds the tolerance limit, the LED on the I/O controller toggles
- Set the voltage level to 3-V DC
- The EFT test is performed as per the test levels shown in [Table 17](#)
- After the test is performed, conduct a performance test to check the degradation
- Repeat the test by changing the input voltage level to 6-V DC

7.4.3.4 EFT Test Results
Table 17. EFT Test Results

TEST NO.	TEST MODE	OBSERVATION
1	0.5 kV, 5 kHz	Pass
2	-0.5 kV, 5 kHz	Pass
3	1 kV, 5 kHz	Pass
4	-1 kV, 5 kHz	Pass
5	1.5 kV, 5 kHz	Pass
6	-1.5 kV, 5 kHz	Pass
7	2 kV, 5 kHz	Pass
8	-2 kV, 5 kHz	Pass
9	0.5 kV, 100 kHz	Pass
10	-0.5 kV, 100 kHz	Pass
11	1 kV, 100 kHz	Pass
12	-1 kV, 100 kHz	Pass
13	1.5 kV, 100 kHz	Pass
14	-1.5 kV, 100 kHz	Pass
15	2 kV, 100 kHz	Pass
16	-2 kV, 100 kHz	Pass

7.4.4 Surge: IEC61000 -4-5

7.4.4.1 Test Level and Expected Performance

The common-mode surge at I/O connectors and the performance criteria expected are as follows:

Table 18. Surge Test Settings

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE (PASS) CRITERIA
Surge IEC 61000-4-5	± 1 kV CM on signal ports	Criteria B

7.4.4.2 Setup Description

The EUT and analog input cable were placed on nonconductive support 10 cm above a reference ground plane. Surge was injected into analog input cable (I/O cable) for testing via a coupling-decoupling network. The EUT operation was monitored before and after the test.

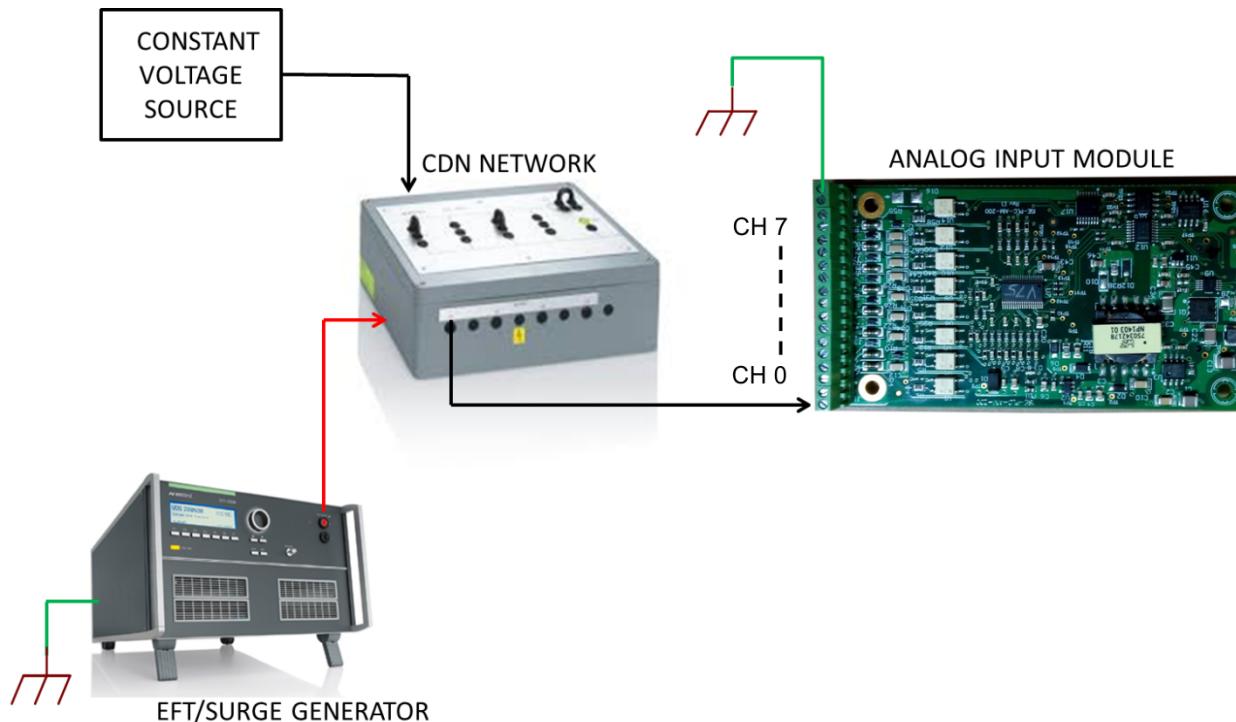


Figure 35. Surge Test Setup

The EUT operation was monitored after the test. All eight channels were monitored after the test by the MCU (on the I/O controller) and compared with a set value (equivalent to the external constant voltage or current source).

7.4.4.3 Monitoring Methods

- Connect the EUT as shown in the test setup. The shield pin is connected to local earth, the same as the test generator
- Power on the EUT
 - The test software is configured to check the analog input for level with in a tolerance limit of 0.2%
 - If the input level exceeds the tolerance limit, the LED on the I/O controller toggles
- Set the voltage level to 3-V DC
- The surge test is performed as per the test levels mentioned in [Table 19](#)
- After the test is performed, conduct a performance test to check the degradation
- Conduct the test by changing the input voltage level to 6-V DC

7.4.4.4 Results

Table 19. Surge Test Results

TEST NO.	TEST MODE	OBSERVATION
1	0.5 kV	Pass
2	-0.5 kV	Pass
3	1 kV	Pass
4	-1 kV	Pass

8 References

For more information, see the following references:

1. AN-2292 Application Report, *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter*, ([SNVA674](#)).
2. AN-2040 Application Report, *AN-2040 Output Voltage Clamping Using the LM5069 Hot Swap Controller*, ([SNVA430](#)).

9 Terminology

Signal-to-Noise Ratio (SNR)

SNR is a measure that compares the level of a desired signal to the level of background noise. SNR is defined as the ratio of signal power to the noise power. The SNR specification provides information regarding the noise energy, excluding the fundamental and harmonic energy present in the frequency spectrum for a particular input frequency. The SNR calculation usually integrates noise up to the Nyquist frequency.

$$\text{SNR} = \frac{P_{\text{SIGNAL}}}{P_{\text{NOISE}}} \quad (16)$$

$$\text{SNR} = 10\log_{10} \left[\frac{P_{\text{SIGNAL}}^2}{(\text{Sum of all harmonic amplitudes} - F_{\text{IN}} - \text{DC})} \times 2 \right] \quad (17)$$

Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)

DNL is the deviation between two analog values corresponding to adjacent input digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the DNL. DNL errors accumulate to produce a total INL.

DNL and INL values are usually specified using one of the following units: LSB or %FSV.

10 Design Files

10.1 Schematics

To download the Schematics, see the design files at [TIDA-00164](#).

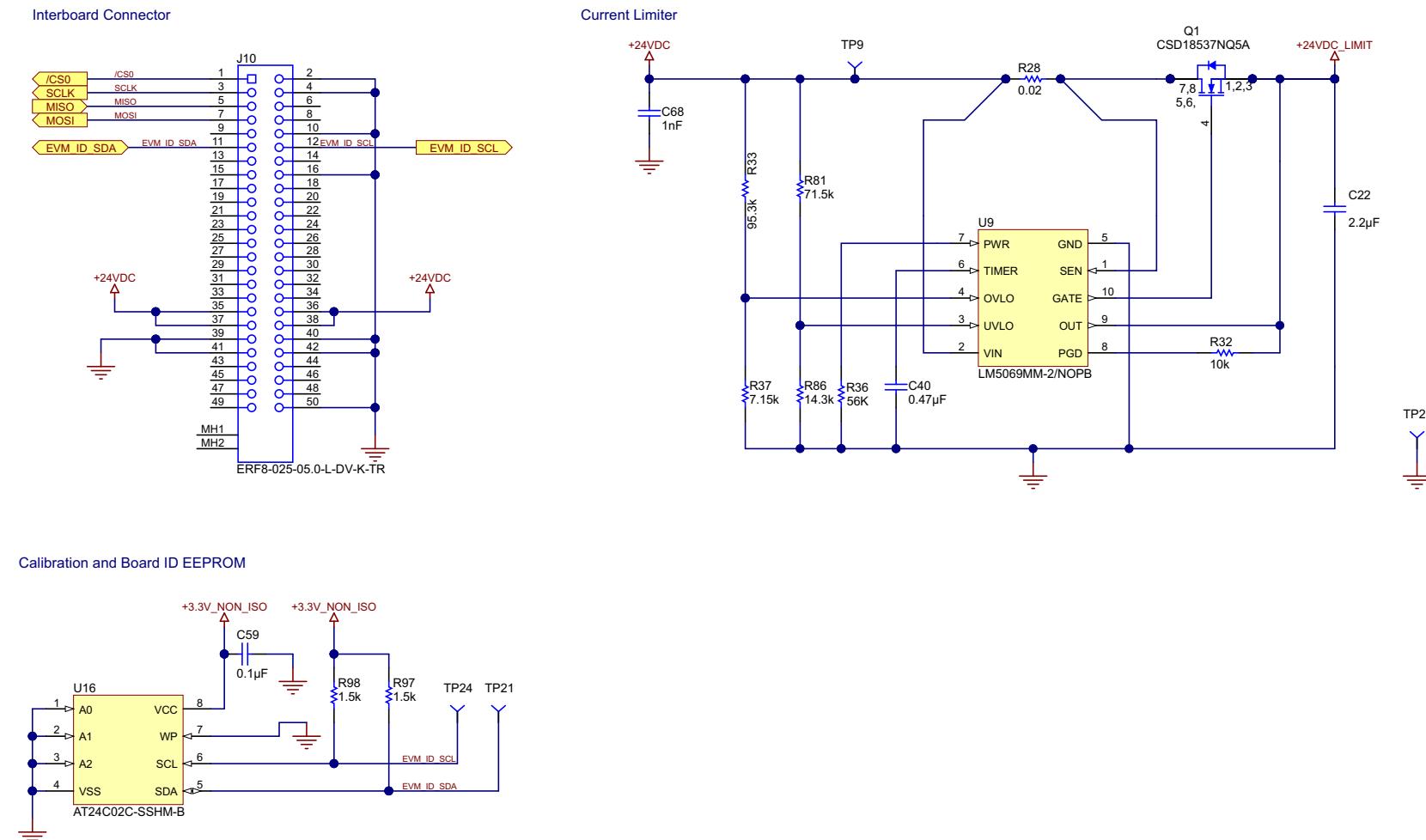


Figure 36. 50-Pin Connector to EVM Board, Hot Swap Controller, EEPROM

Isolated Power Supply and Signal Isolation

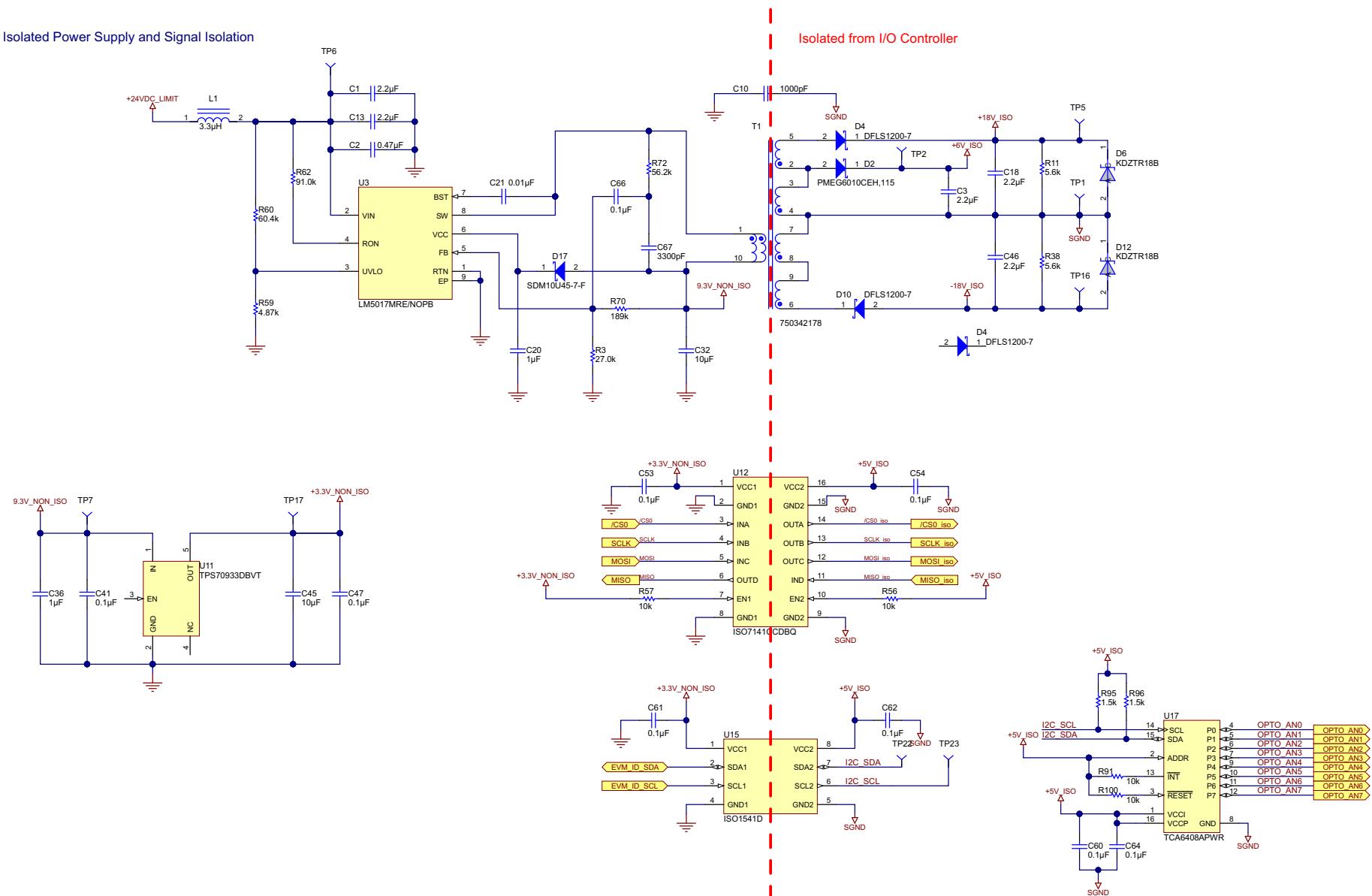


Figure 37. Isolated SPI and I²C, Isolated Fly-Buck Power Supply for 18V_ISO, -18V_ISO, 6V_ISO, and 3.3V_NON_ISO

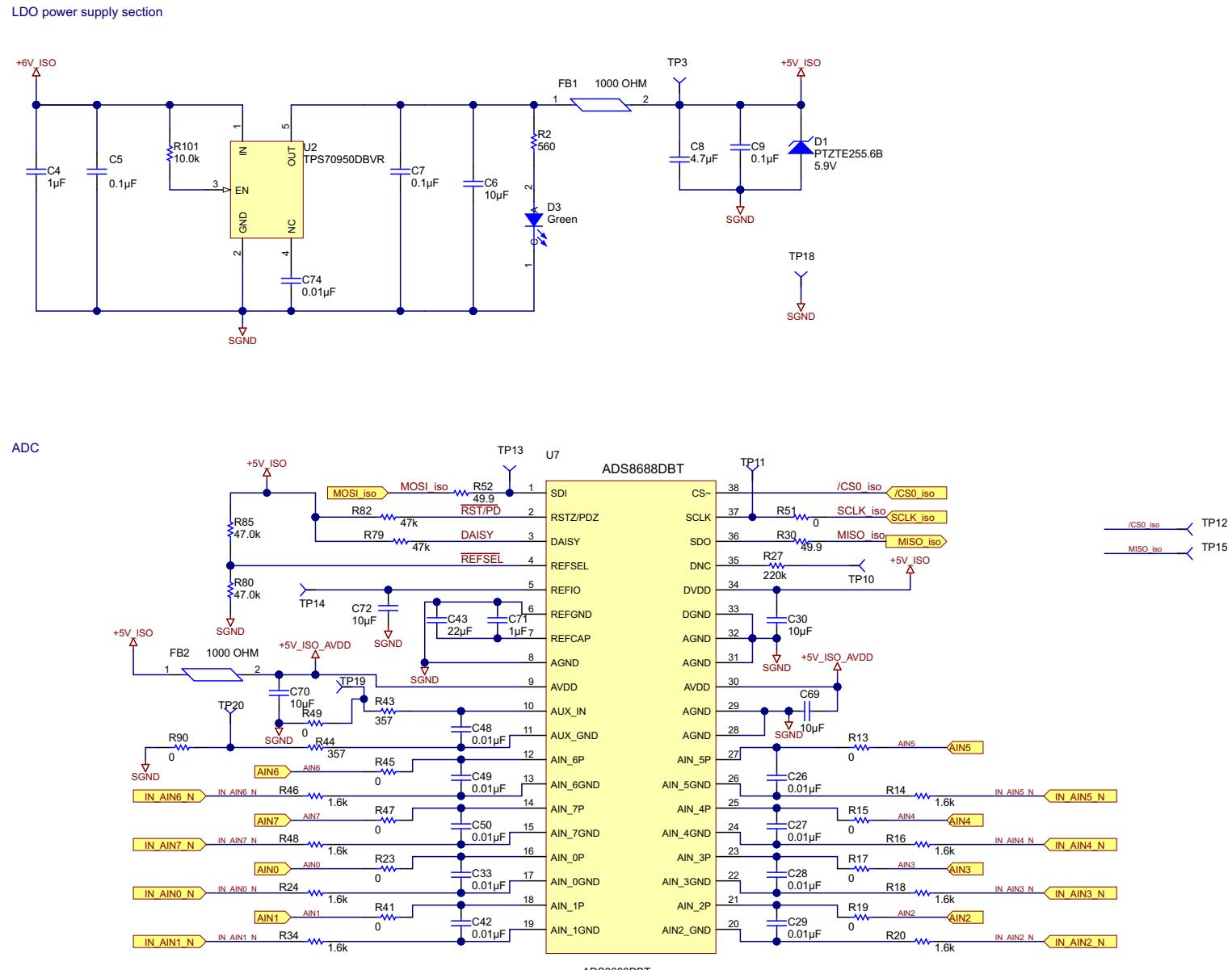


Figure 38. LDO to Generate 5V_ISO and V_{CC} and ADC

AN0 to AN3

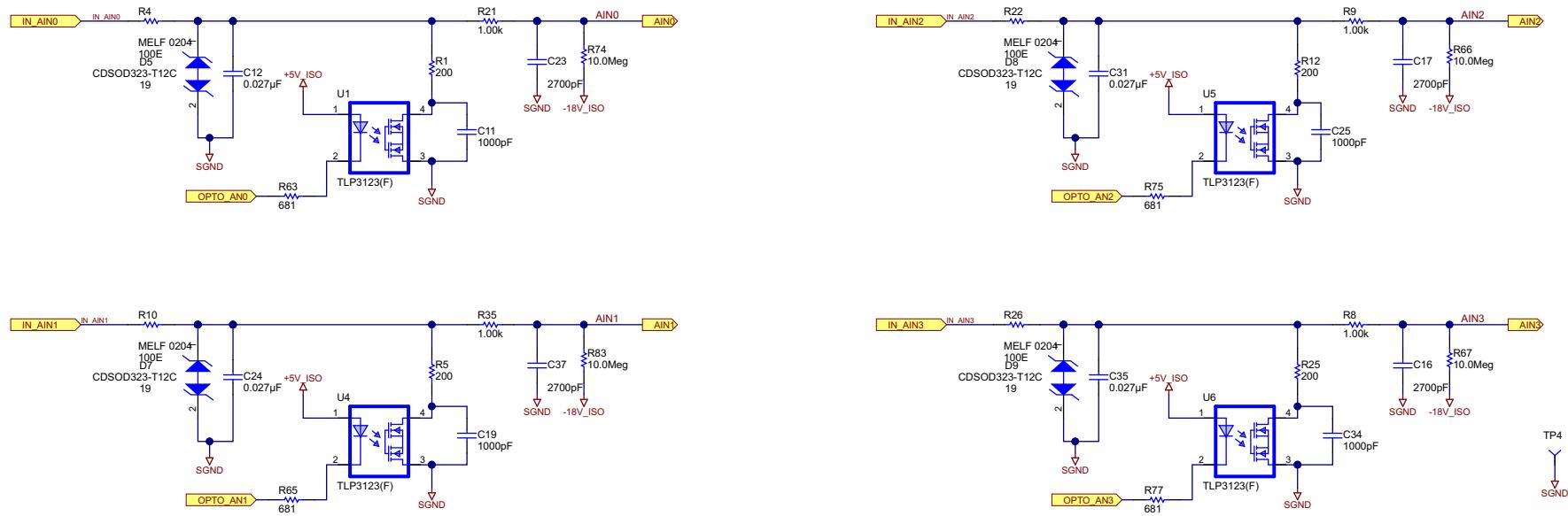
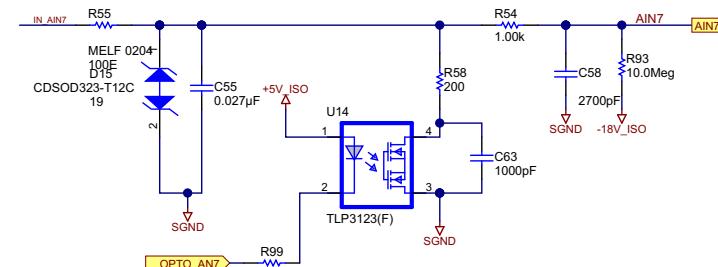
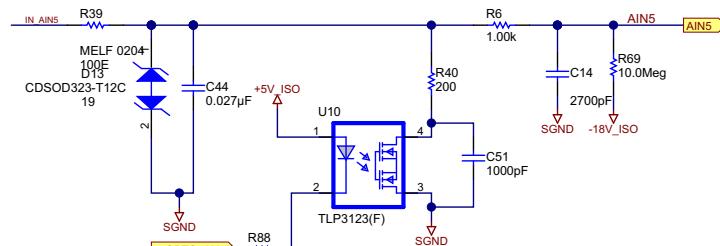
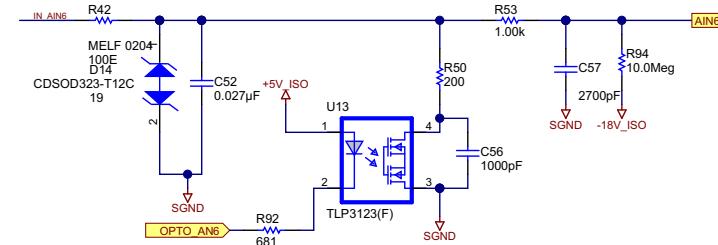
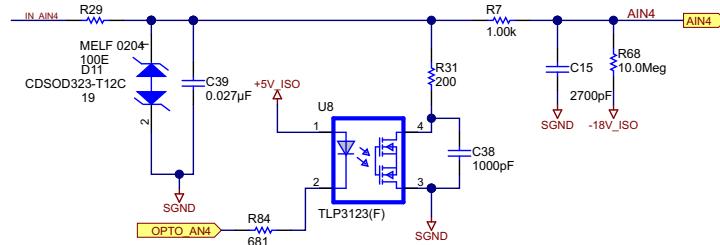
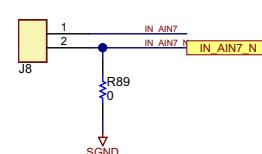
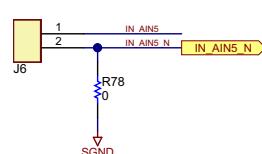
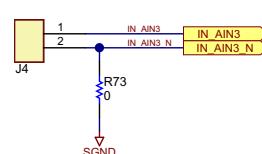
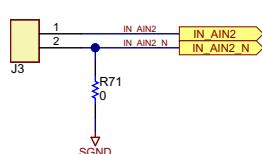
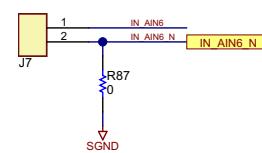
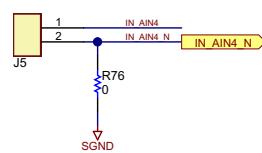
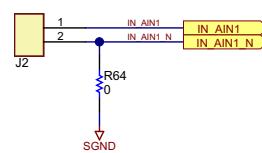
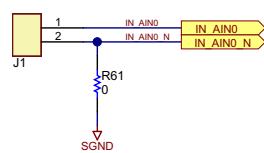
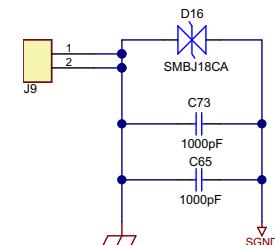


Figure 39. Analog Input 1

AN4 to AN7


Terminal Blocks Voltage Inputs

Chassis Ground

Figure 40. Analog Input 2

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00164](#).

Table 20. BOM

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
1	C1, C13, C22	CAP, CERM, 2.2 μ F, 100 V, \pm 10%, X7R, 1210	MuRata	GRM32ER72A225KA35L	3
2	C2	CAP, CERM, 0.47 μ F, 100 V, \pm 10%, X7R, 1206	MuRata	GRM31MR72A474KA35L	1
3	C3, C18, C46	CAP, CERM, 2.2 μ F, 25 V, \pm 10%, X7R, 0805	MuRata	GRM21BR71E225KA73L	3
4	C4, C36	CAP, CERM, 1 μ F, 50 V, \pm 10%, X7R, 0805	AVX	08055C105KAT2A	2
5	C5, C7, C9, C41, C47, C53, C54, C59, C60, C61, C62, C64	CAP, CERM, 0.1 μ F, 50 V, \pm 10%, X7R, 0603	Kemet	C0603C104K5RACTU	12
6	C6, C30, C45, C72	CAP, CERM, 10 μ F, 16 V, \pm 20%, X5R, 0805	AVX	0805YD106MAT2A	4
7	C8	CAP, CERM, 4.7 μ F, 50 V, \pm 10%, X5R, 0805	TDK	C2012X5R1H475K125AB	1
8	C10, C65, C73	CAP, CERM, 1000 pF, 2 KV 10% X7R 1206	Johanson Dielectrics Inc	202R18W102KV4E	3
9	C12, C24, C31, C35, C39, C44, C52, C55	CAP, CERM, 0.027 μ F, 50 V, \pm 5%, C0G/NP0, 1206	MuRata	GRM3195C1H273JA01D	8
10	C14, C15, C16, C17, C23, C37, C57, C58	CAP, CERM, 2700 pF, 100 V, \pm 5%, X7R, 0603	AVX	06031C272JAT2A	8
11	C20	CAP, CERM, 1 μ F, 50 V, \pm 10%, X5R, 0603	MuRata	GRM188R61H105KAALD	1
12	C21, C26, C27, C28, C29, C33, C42, C48, C49, C50	CAP, CERM, 0.01 μ F, 100 V, \pm 5%, X7R, 0603	AVX	06031C103JAT2A	10
13	C32	CAP, CERM, 10 μ F, 35 V, \pm 20%, X7R, 1210	Taiyo Yuden	GMK325AB7106MM-T	1
14	C40	CAP, CERM, 0.47 μ F, 50 V, 10%, X5R, 0603	Taiyo Yuden	UMK107ABJ474KA-T	1
15	C43	CAP, CERM, 22 μ F, 16 V, \pm 20%, X5R, 1206	AVX	1206YD226MAT2A	1
16	C66	CAP, CERM, 0.1 μ F, 100 V, \pm 10%, X7R, 0603	MuRata	GRM188R72A104KA35D	1
17	C67	CAP, CERM, 3300 pF, 100 V, \pm 5%, X7R, 0603	AVX	06031C332JAT2A	1
18	C68	CAP, CERM, 1000 pF, 100 V, \pm 20%, X7R, 0603	AVX	06031C102MAT2A	1
19	C69, C70	CAP, CERM, 10 μ F, 16 V, \pm 20%, X5R, 0603	Taiyo Yuden	EMK107BBJ106MA-T	2
20	C71	CAP, CERM, 1 μ F, 16 V, \pm 10%, X7R, 0603	Taiyo Yuden	EMK107B7105KA-T	1
21	C74	CAP, CERM, 0.01 μ F, 50 V, \pm 5%, X7R, 0603	Kemet	C0603C103J5RACTU	1
22	D1	DIODE ZENER 5.9 V, 1 W PMDS	Rohm Semiconductor	PTZTE255.6B	1
23	D2	Diode, Schottky, 60 V, 1 A, SOD-123F	NXP Semiconductor	PMEG6010CEH,115	1
24	D3	LED SmartLED Green 570 NM	OSRAM	LG L29K-G2J1-24-Z	1
25	D4	Diode, Schottky, 200 V, 1 A, PowerDI123	Diodes Inc.	DFLS1200-7	2
26	D5, D7, D8, D9, D11, D13, D14, D15	Diode, TVS, ARRAY, 19 V, SOD323	Bourns Inc.	CDSOD323-T12C	8
27	D6, D12	Diode Zener 19 V, 1 W PMDU	Rohm Semiconductor	KDZTR18B	2
28	D17	Diode, Schottky, 45 V, 0.1 A, SOD-523	Diodes Inc.	SDM10U45-7-F	1

Table 20. BOM (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
29	FB1, FB2	Ferrite Chip 1000 Ω , 300 MA 0603	TDK Corporation	MMZ1608B102C	2
30	J1, J2, J3, J4, J5, J6, J7, J8, J9	Terminal Block, 4x1, 2.54 mm, TH	On Shore Technology Inc	OSTVN02A150	9
31	J10	Receptacle, 0.8 mm, 25x2, SMT	Samtec	ERF8-025-05.0-L-DV-K-TR	1
32	L1	Inductor, Chip, $\pm 10\%$	EPCOS INC.	B82422H1332K	1
33	Q1	MOSFET, N-CH, 60 V, 50 A, SON 5x6 mm	Texas Instruments	CSD18537NQ5A	1
34	R1, R5, R12, R25, R31, R40, R50, R58	RES, 200 Ω , 0.1%, 0.125 W, 0805	Susumu Co Ltd	RG2012P-201-B-T5	8
35	R2	RES, 560 Ω , 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603560RJNEA	1
36	R3	RES, 27.0 k Ω , 1%, 0.1 W, 0603	Yageo America	RC0603FR-0727KL	1
37	R4, R10, R22, R26, R29, R39, R42, R55	RES 100 Ω , .4 W, 1% 0204 MELF	Vishay Beyschlag	MMA02040C1000FB300	8
38	R6, R7, R8, R9, R21, R35, R53, R54	RES, 1.00 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	8
39	R11, R38	RES, 5.6 k Ω , 5%, 0.125 W, 0805	Vishay-Dale	CRCW08055K60JNEA	2
40	R13, R15, R17, R19, R23, R41, R45, R47	RES, 0 Ω , 5%, 0.1 W, 0603	Rohm	MCR03EZPJ000	8
41	R14, R16, R18, R20, R24, R34, R46, R48	RES, 1.6 k Ω , 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K60JNEA	8
42	R28	RES, 0.02 Ω , 1%, 1 W, 1206	Susumu Co Ltd	PRL1632-R020-F-T1	1
43	R30, R52	RES, 49.9 Ω , 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	2
44	R32	RES, 10 k Ω , 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	1
45	R33	RES, 95.3 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060395K3FKEA	1
46	R36	RES 56 k Ω 1/20 W 1% 0201	Yageo America	RC0603FR-0756KL	1
47	R37	RES, 7.15 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW06037K15FKEA	1
48	R43, R44	RES, 357 Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603357RFKEA	2
49	R49, R51, R90	RES, 0 Ω , 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	3
50	R56, R57, R91, R100	RES, 10 k Ω , 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0JNED	4
51	R59	RES, 4.87 k Ω , 1%, 0.1 W, 0603	Yageo America	RC0603FR-074K87L	1
52	R60	RES, 60.4 k Ω , 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0760K4L	1
53	R61, R64, R71, R73, R76, R78, R87, R89	RES 0.0 Ω .5 W JUMP 1206 SMD	Vishay Dale	CRCW12060000Z0EAHP	8
54	R62	RES, 91.0 k Ω , 1%, 0.1 W, 0603	Yageo America	RC0603FR-0791KL	1
55	R63, R65, R75, R77, R84, R88, R92, R99	RES, 681 Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603681RFKEA	8
56	R66, R67, R68, R69, R74, R83, R93, R94	RES, 10.0 M Ω , 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210M0FKED	8
57	R70	RES, 189 k Ω , 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD07189KL	1
58	R72	RES, 56.2 k Ω , 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0756K2L	1

Table 20. BOM (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
59	R79, R82	RES, 47 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040247K0JNED	2
60	R80	RES, 47.0 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0747KL	1
61	R81	RES, 71.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060371K5FKEA	1
62	R86	RES, 14.3 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060314K3FKEA	1
63	R95, R96, R97, R98	RES, 1.5 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED	4
64	T1	Transformer, 50 uH, SMT	Wurth Elektronik eiSos	750342178	1
65	U1, U4, U5, U6, U8, U10, U13, U14	Photorelay Mosfet 1A 4-SOP	Toshiba Semiconductor and Storage	TLP3123(F)	8
66	U2	IC REG LDO 5 V, 0.15 A SOT23-5	Texas Instruments	TPS70950DBVR	1
67	U3	100 V, 600 mA Constant On-Time Synchronous Buck Regulator, DDA0008B	Texas Instruments	LM5017MRE/NOPB	1
68	U7	16-bit 400KSPS 8-Channel SAR ADC	Texas Instruments	ADS8688DBT	1
69	U9	Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	National Semiconductor	LM5069MM-2/NOPB	1
70	U11	IC REG LDO 3.3 V, 0.15 A SOT23-5	Texas Instruments	TPS70933DBVT	1
71	U12	4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	Texas Instruments	ISO7141CCDBQ	1
72	U15	Low-Power Bidirectional I2C Isolators, D0008A	Texas Instruments	ISO1541D	1
73	U16	IC, EEPROM, 2K-BIT, 1 MHZ, SOIC-8	Atmel	AT24C02C-SSHM-B	1
74	U17	Low-Voltage 8-Bit I2C and SMBus I/O Expander, 1.65 to 5.5 V, -40°C to 85°C, 16-pin TSSOP (PW), Green (RoHS and no Sb/Br)	Texas Instruments	TCA6408APWR	1
75	C11, C19, C25, C34, C38, C51, C56, C63	CAP, CERM, 1000 pF, 50 V, ±20%, X7R, 0402	TDK	C1005X7R1H102M	DNP
76	D10	Diode, Schottky, 200 V, 1 A, PowerDI123	Diodes Inc.	DFLS1200-7	DNP
77	D16	TVS 18 V, 600 W BI-DIR SMB	Littelfuse Inc	SMBJ18CA	DNP
78	R27	RES, 221 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD07221KL	DNP
79	R85	RES, 47.0 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0747KL	DNP
80	R101	RES, 10.0 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	DNP

10.3 PCB Layout

The analog input module is implemented in four PCB layers. For optimal performance of this design, follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC and EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low impedance, low-inductance traces should be used along the output signal path and protection elements. When possible, copper pours are used in place of traces. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

To achieve a high performance, follow these layout guidelines:

1. Use a common ground plane for both analog and digital.
2. Route all signals, assuming there is a split ground plane for analog and digital. Furthermore, split the ground initially during layout for better results. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then, short both grounds to form a common ground plane.
3. Return the ADC ground pins to the ground plane through multiple vias (PTH).
4. Ensure that protection elements, such as TVS diodes and capacitors, are placed as close to the connectors as possible to ensure the return current from high-energy transients does not cause damage to sensitive devices. Afterwards, use large and wide traces to ensure a low-impedance path for high-energy transients.
5. Place the decoupling capacitors close to supply pin of IC.
6. Use multiple vias for power and ground for decoupling caps.
7. Route the current sense resistor as a Kelvin sense connection.
8. SPI lines: for signal integrity, place the termination resistances near the source.
9. Place decoupling capacitors closely to each respective AVDD and AVSS pin.
10. Place the reference capacitor close to the voltage reference input pin.

10.3.1 PCB Layout Prints

To download the layout prints, see the design files at [TIDA-00164](#).

NOTE: All artwork is viewed from the top side.

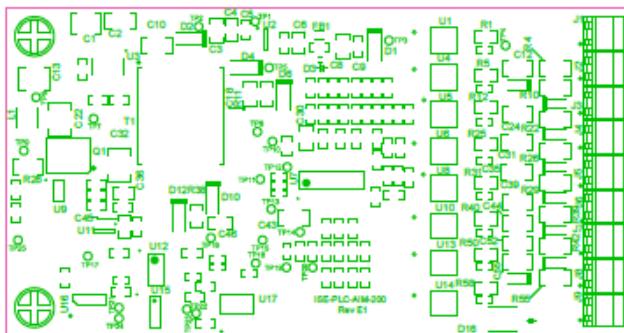


Figure 41. Top Silkscreen

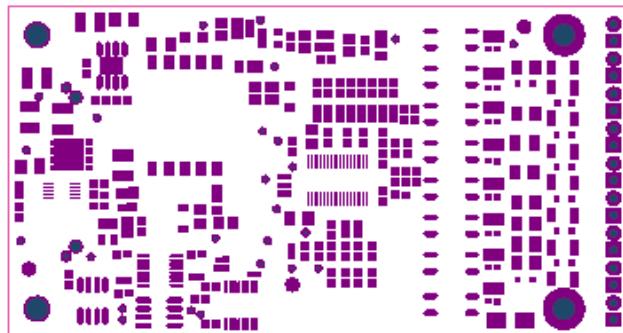


Figure 42. Top Solder Mask

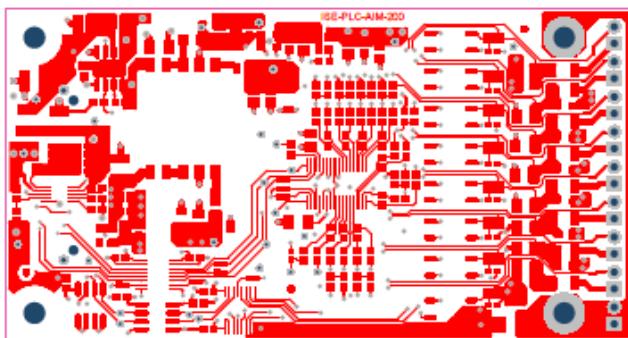


Figure 43. Top Layer

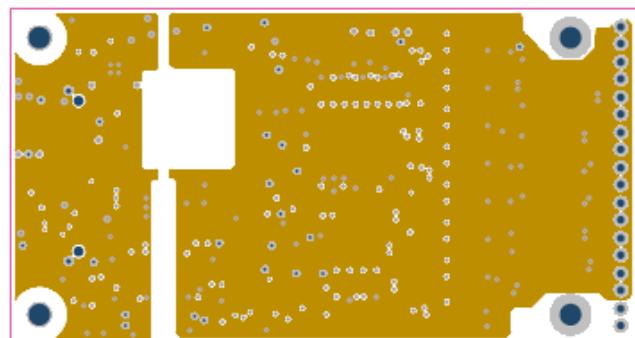


Figure 44. Ground Plane Layer 2



Figure 45. Power Plane Layer 3

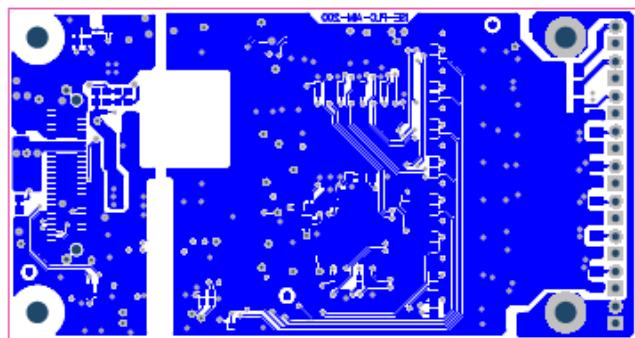


Figure 46. Bottom Layer

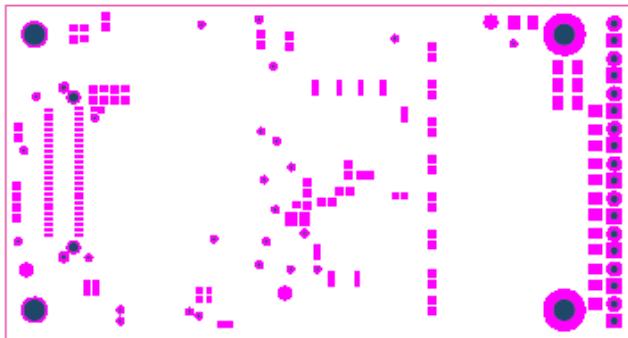


Figure 47. Bottom Solder Mask

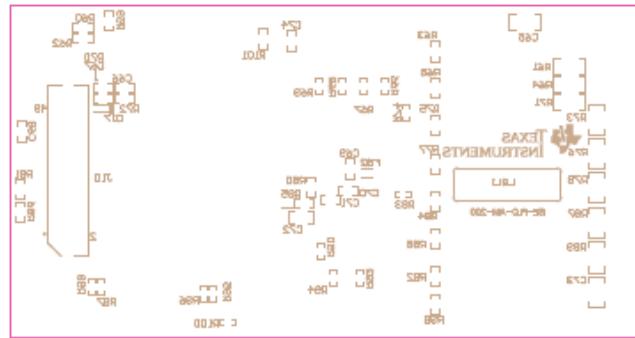


Figure 48. Bottom Silkscreen

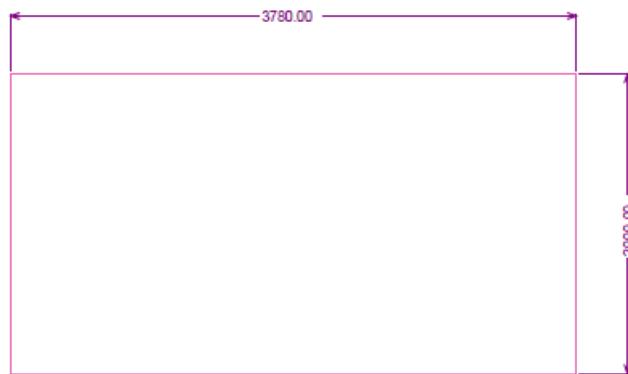


Figure 49. Mechanical Dimensions

10.4 Layout Guidelines

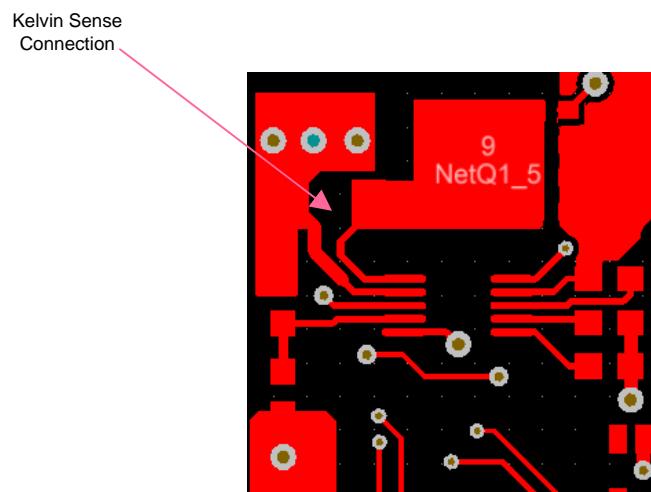


Figure 50. Kelvin Sense Connection

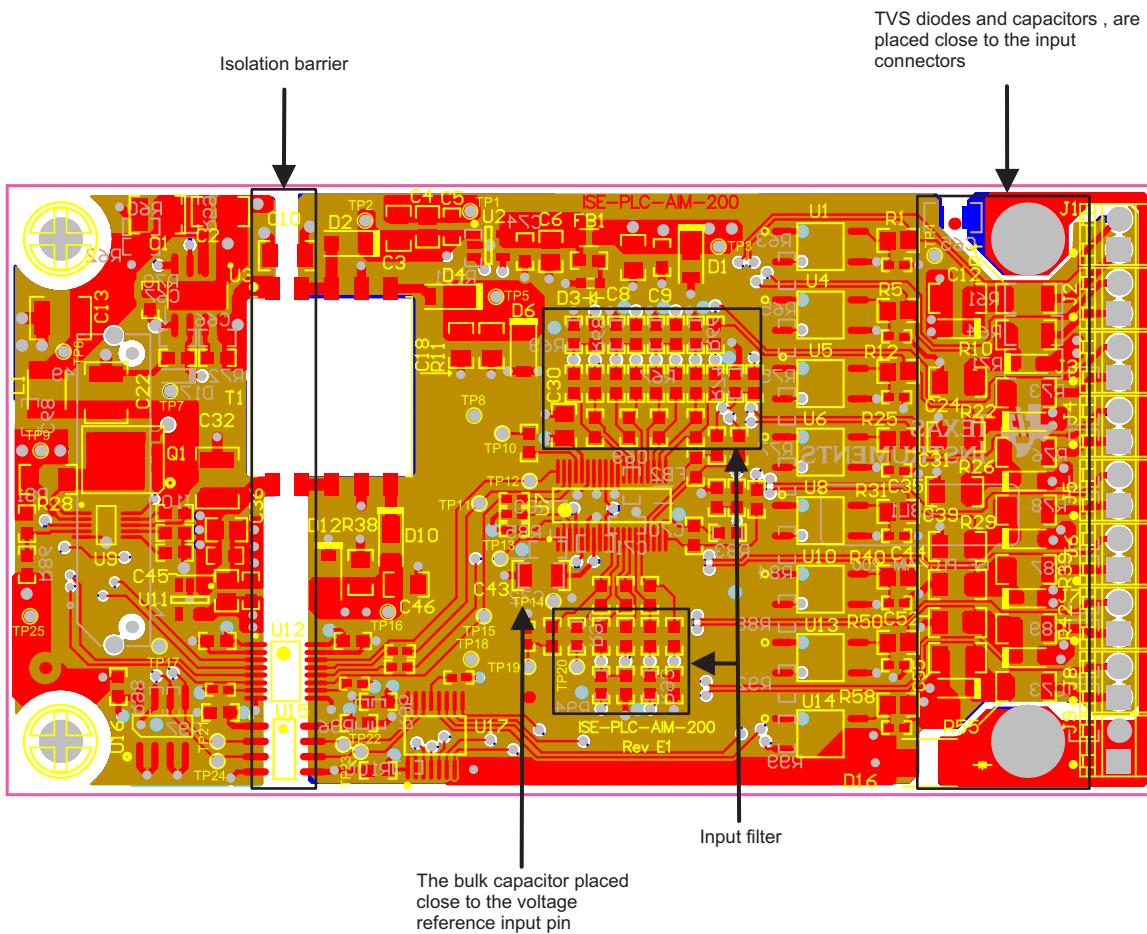


Figure 51. Highlighted Parts

10.5 Altium Project

To download the Altium project files, see the design files at [TIDA-00164](#).

10.6 Gerber Files

To download the Gerber files, see the design files at [TIDA-00164](#).

11 Software Files

To download the software files, see the design files at [TIDA-00164](#).

12 About the Authors

AMOL GADKARI is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Amol has eight years of experience in mixed signal board design, analog circuit designs, and EMC-protection circuit design. He can be reached at a-gadkari@ti.com.

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TIDA-00164 First Revision History

Changes from Original (June 2014) to A Revision	Page
• Changed Typical Characteristics graphs	18

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

TIDA-00164 Second Revision History

Changes from A Revision (July 2014) to B Revision	Page
• Deleted the $\pm 20\text{-mA}$ range	1
• Deleted sentence mentioning the ALARM feature	5
• Changed image to one without the ALARM pin	5
• Changed μSec value from 8.79	7
• Added Section 7.2: Accuracy Test Results.....	20
• Changed pin 35 to Do Not Connect to reflect the removal of the ALARM feature.....	31
• Changed the placement of various designators	34
• Changed the placement of various designators	35
• Changed the placement of various designators	36

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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