Section 7. Resets

HIGHLIGHTS

This section of the manual contains the following topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the **"Resets"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

7.1 INTRODUCTION

The Resets module combines all reset sources and controls the system reset signal SYSRST. The following is a list of device Reset sources:

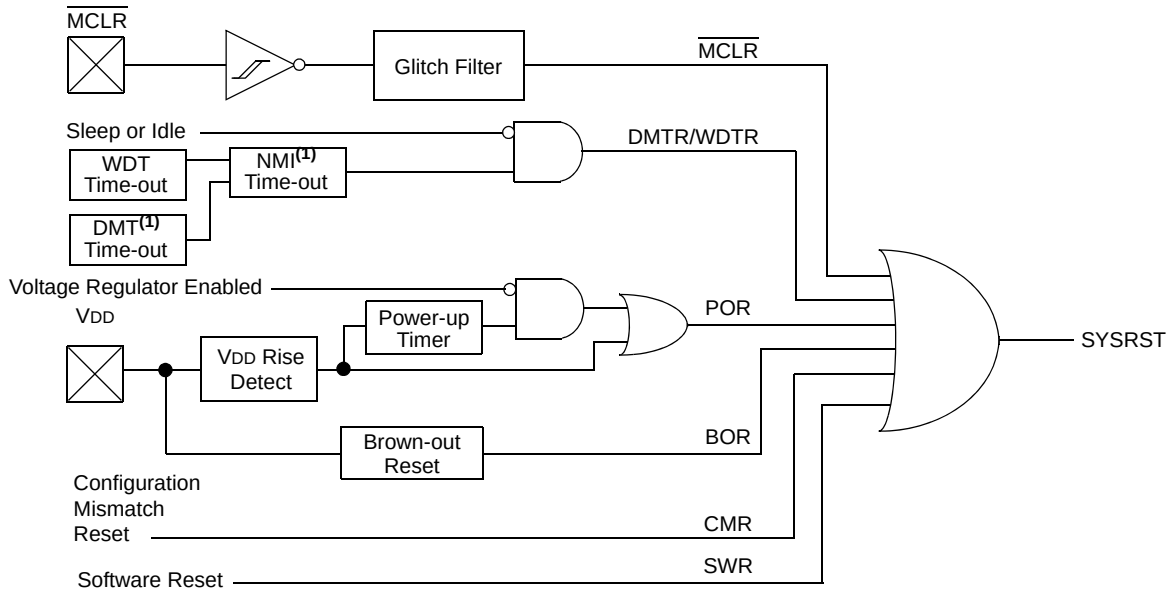
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Master Clear Reset ($\overline{\text{MCLR}}$)
- Watchdog Time-out Reset (WDTR)
- Software Reset (SWR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

Note: Not all reset sources exist on all devices. Refer to the **"Resets"** chapter in the specific device data sheet to determine availability.

A simplified block diagram of the Reset module is shown in Figure 7-1. Any active source of reset will make the system reset signal active. Many registers associated with the CPU and peripherals are forced to a known "reset state". Most registers are unaffected by a reset; their status is unknown on POR and unchanged by all other resets.

Note: For register reset states, refer to the specific peripheral or **Section 2. "CPU"** (DS60001113) of the "*PIC32 Family Reference Manual*".

Figure 7-1: System Reset Block Diagram



Note 1: This feature is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet for availability.

7.2 CONTROL REGISTERS

Most types of device resets will set corresponding Status bits in the RCON register to indicate the type of Reset (see Register 7-1). The one exception is the Non-maskable Interrupt (NMI) time-out Reset, which is only available on certain devices (refer to the **"Resets"** chapter of the specific device data sheet for availability). A Power-on Reset (POR) will clear all bits, except for the BOR and POR bits (RCON<1:0>), which are set. The user software may set or clear any of the bits at any time during code execution. The RCON bits serve only as Status bits. Setting a particular Reset status bit in software will not cause a system Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. For more information on the function of these bits, refer to **7.4.3 "Using the RCON Status Bits"**.

The RSWRST control register has only one bit, SWRST. This bit is used to force a software Reset condition.

For those devices that have the NMI Reset, it becomes possible to delay either the WDT or DMT Reset events by vectoring to a NMI instead of immediately forcing a reset. A delay equal to the duration of the number of NMICNT system clocks begins as it is decremented to zero. During this interval, the program can clear the WDT or DMT flag bits, if desired, to avoid a Reset. If the active flag is not cleared, the device will be reset at the end of the interval. The NMICNT value can be set to zero for no delay and up to 255 SYSCLK cycles.

The NMI interrupt can also be triggered by setting the SWNMI bit in software, or if the CF bit is set by the FSCM, but these do not begin the countdown and do not automatically lead to a reset.

The PWRCON register, available on some PIC32 devices, provides an alternate location of the VREGS bit, if it is not available in the RCON register.

The Resets module consists of the following Special Function Registers (SFRs):

- **RCON: Reset Control Register**
- **RSWRST: Software Reset Register**
- **RNMICON: Non-Maskable Interrupt (NMI) Control Register**
- **PWRCON: Power Control Register**

Table 7-1 summarizes all Resets-related registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 7-1: Reset SFR Summary

Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
RCON(1)	31:24	—	—	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR
RSWRST(1)	31:24	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
RNMICON(1)	31:24	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	—	—	CF	WDTS
	23:16	—	—	—	—	—	—	—	—	—	NMICNT<7:0>						
PWRCON(1)	31:24	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS

Legend: — = unimplemented, read as '0'. Address offset values are shown in hexadecimal.

Note 1: This register has an associated Clear, Set, and Invert register at an offset of 0x4, 0x8, and 0xC bytes, respectively. The Clear, Set, and Invert registers have the same name with CLR, SET, or INV appended to the register name (e.g., RCONCLR). Writing a '1' to any bit position in these registers will clear, set, or invert valid bits in the associated register. Reads from these registers should be ignored.

Register 7-1: RCON: Reset Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	RW-0, HC	R/W-0, HC	U-0	U-0
	—	—	—	—	BCFGERR(4)	BCFGFAIL(4)	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
	—	—	—	—	—	—	CMR(1,3)	VREGS(4)
7:0	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
	EXTR(1,3)	SWR(1,3)	DMTO(4)	WDTO(1,3)	SLEEP(1,3)	IDLE(1,3)	BOR(1,2,3)	POR(1,2,3)

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HC = Cleared by hardware	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit(4)
1 = An error occurred during a read of the primary configuration from registers
0 = No error occurred during a read of the primary configuration from registers

bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit(4)
1 = An error occurred during a read of the primary and alternate configuration registers
0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Flag bit(1,3)
1 = A configuration mismatch reset has occurred
0 = A configuration mismatch reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = The voltage regulator is enabled and is on during Sleep mode
0 = The voltage regulator is disabled and is off during Sleep mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit(1,3)
1 = A master clear (pin) reset has occurred
0 = A master clear (pin) reset has not occurred

bit 6 **SWR:** Software Reset Flag bit(1,3)
1 = A software reset was executed
0 = A software reset was not executed

bit 5 **DMTO:** Deadman Timer Time-out Flag bit(4)
1 = A Deadman Timer time-out has occurred
0 = A Deadman Timer time-out has not occurred

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit(1,3)
1 = A Watchdog Timer time-out has occurred
0 = A Watchdog Timer time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit(1,3)
1 = The device was in Sleep mode
0 = The device was not in Sleep mode

Note 1: The RCON flag bits only serve as status bits. Setting a particular reset status bit in software will not cause a device Reset to occur.

2: The BOR bit is also set after a Power-on Reset (POR).

3: This bit is set in hardware; it can only be cleared (= 0) in software.

4: This bit is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet for availability.

Register 7-1: RCON: Reset Control Register (Continued)

bit 2 **IDLE:** Wake From Idle Flag bit(1,3)
- 1 = The device was in Idle mode
- 0 = The device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1,2,3)

User software must clear this bit to view next detection.
- 1 = A Brown-out Reset has occurred
- 0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1,2,3)

User software must clear this bit to view next detection.
- 1 = A Power-on Reset has occurred
- 0 = A Power-on Reset has not occurred

Note 1: The RCON flag bits only serve as status bits. Setting a particular reset status bit in software will not cause a device Reset to occur.

2: The BOR bit is also set after a Power-on Reset (POR).

3: This bit is set in hardware; it can only be cleared (= 0) in software.

4: This bit is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet for availability.

Register 7-2: RSWRST: Software Reset Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0
	—	—	—	—	—	—	—	SWRST(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1)

1 = Enable software Reset event

0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. A read must follow the write of this bit to generate a Reset. See **7.3.4 "Software Reset (SWR)"** for more information.

Register 7-3: RNMICON: Non-Maskable Interrupt (NMI) Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	—	—	CF	WDTS
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	NMICNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMTO:** Deadman Timer Time-out Flag bit
1 = DMT time-out has occurred and caused a NMI
0 = DMT time-out has not occurred
Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit
1 = WDT time-out has occurred and caused a NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event, and MNICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger
1 = An NMI will be generated
0 = An NMI will not be generated

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure

Setting this bit will cause a a CF NMI event, but will not cause a clock switch to the Back-up FRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NMICNT<7:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
11111111-00000001 = Number of SYSCLK cycles before a device Reset occurs(1)
00000000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches '0', no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: This register is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet for availability.

Register 7-4: PWRCON: Power Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W
	—	—	—	—	—	—	—	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **VERGS:** Voltage Regulator Stand-by Enable bit
1 = Voltage regulator will remain active during Sleep
0 = Voltage regulator will go to Stand-by mode during Sleep

Note: This register is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet for availability.

7.3 MODES OF OPERATION

7.3.1 System Reset (SYSRST)

The PIC32 Internal System Reset (SYSRST) can be generated from multiple Reset sources, such as:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Master Clear Reset ($\overline{\text{MCLR}}$)
- Watchdog Time-out Reset (WDTO)
- Software Reset (SWR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A system reset is active at the first POR and asserted until device configuration settings are loaded and the oscillator clock sources become stable. The system reset is then deasserted allowing the CPU to start fetching code after eight system clock cycles (SYSCLK).

BOR, $\overline{\text{MCLR}}$ and WDTO resets are asynchronous events, and to avoid SFR and RAM corruptions, the system reset is synchronized with the system clock. All other reset events are synchronous.

7.3.2 Power-on Reset (POR)

A power-on event generates an internal POR pulse when a VDD rise is detected above VPOR. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise-rate specifications, refer to the **"Electrical Characteristics"** chapter of the specific device data sheet.

For those PIC32 devices that have the on-chip voltage regulator enabled, the Power-up Timer (PWRT) is automatically disabled. For those PIC32 devices that have the on-chip voltage regulator disabled, the core is supplied from an external power supply and the Power-up Timer is automatically enabled and is used to extend the duration of a power-up sequence. The PWRT adds a fixed 64 ms nominal delay at device start-up. Therefore, the Power-on delay can either be the on-chip voltage regulator output delay, designated as TPU, or the power-up timer delay, designated as TPWRT.

At this point the POR event has expired, but the device Reset is still asserted while device configuration settings are loaded and the clock oscillator sources are configured. The clock monitoring circuitry waits for the oscillator source to become stable. The clock source used by PIC32 devices when exiting from Reset, is always selected from the FNOSC<2:0> bits (DEVCFG1<2:0>). This additional delay depends on the clock and can include delays for TOSC, TLOCK and TFSCM. For details on the oscillator, PLL and Fail-Safe Clock Monitoring (FSCM). Depending on your device, refer to either **6.3.5 "Fail-Safe Clock Monitor Operation"** in **Section 6. "Oscillator"** (DS60001112) or **42.3.6 "Fail-Safe Clock Monitor Operation"** in **Section 42. "Oscillators with Enhanced PLL"**.

After these delays expire, the system reset, SYSRST, is deasserted. Before allowing the CPU to start code execution, eight system clock cycles are required before the synchronized reset to the CPU core is deasserted.

The power-on event sets the BOR and POR status bits (RCON<1:0>).

For more information on the values of the delay parameters, refer to the **"Electrical Characteristics"** chapter in the specific device data sheet.

Note:	When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user software must ensure that the delay between the time power is first applied and the time the system reset is released is adequate to get all operating parameters within the specification.

7.3.3 Master Clear Reset ($\overline{\text{MCLR}}$)

Whenever the master clear pin ($\overline{\text{MCLR}}$) is driven low, the reset event is synchronized with the system clock, SYSCLK, before asserting the system reset, SYSRST, provided the input pulse on $\overline{\text{MCLR}}$ is longer than a certain minimum width, as specified in the **"Electrical Characteristics"** chapter of the specific device data sheet.

The $\overline{\text{MCLR}}$ pin provides a filter to minimize the effects of noise and to avoid unwanted reset events. The Status bit, EXTR (RCON<7>), is set to indicate the $\overline{\text{MCLR}}$ Reset.

7.3.4 Software Reset (SWR)

The PIC32 CPU core does not provide a specific `RESET` instruction; however, a hardware reset can be performed in software (software reset) by executing a software reset command sequence. The software reset acts like a $\overline{\text{MCLR}}$ Reset. The software reset sequence requires the system unlock sequence to be executed before the SWRST bit (RSWRST<0>) can be written. For system unlock details, see either **6.3.6 "Clock Switching Operation"** in **Section 6. "Oscillator"** (DS60001112) or **42.3.7 "Clock Switching Operation"** in **Section 42. "Oscillators with Enhanced PLL"**.

A software Reset is performed as follows:

1. Write the system unlock sequence.
2. Set the SWRST bit (RSWRST<0>) = `1`.
3. Read the RSWRST register.

Follow with "`while(1);`" or four "`NOP`" instructions.

Writing a '`1`' to the RSWRST register sets the SWRST bit, arming the software reset. The subsequent read of the RSWRST register triggers the software reset, which should occur on the next clock cycle following the read operation. To ensure no other user code is executed before the reset event occurs, it is recommended that four "`NOP`" instructions or a "`while(1);`" statement is placed after the `READ` instruction.

The SWR Status bit (RCON<6>) is set to indicate the software reset.

Example 7-1: Software Reset Command Sequence

```
/* The following code illustrates a software Reset */
// assume interrupts are disabled
// assume the DMA controller is suspended
// assume the device is locked
/* perform a system unlock sequence */
// starting critical sequence
SYSKEY = 0x00000000; //write invalid key to force lock
SYSKEY = 0xAA996655;  //write key1 to SYSKEY
SYSKEY = 0x556699AA;  //write key2 to SYSKEY
// OSCCON is now unlocked
/* set SWRST bit to arm reset */
RSWRSTSET = 1;

/* read RSWRST register to trigger reset */
unsigned int dummy;
dummy = RSWRST;
/* prevent any unwanted code execution until reset occurs*/
while(1);
```

7.3.5 Watchdog Timer Reset (WDTR)

A Watchdog Timer (WDT) reset event is synchronized with the system clock, SYSCLK, before asserting the system reset.

Note:	A WDT time-out during Sleep or Idle mode will wake-up the processor and branch to the PIC32 reset vector, but does not Reset the processor.

The only bits affected are WDTO, and SLEEP or IDLE in the RCON register. For more information on the WDT reset, refer to **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114).

7.3.6 Brown-out Reset (BOR)

PIC32 family devices have a simple Brown-out Reset (BOR) capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a BOR event, which is synchronized with the system clock, SYSCLK, before asserting the system Reset. This event is captured by the BOR flag bit (RCON<1>). Refer to the **"Electrical Characteristics"** chapter of the specific device data sheet for further details.

7.3.7 Configuration Mismatch Reset (CMR)

To maintain the integrity of the stored configuration values, all device Configuration bits are loaded and implemented as a complementary set of bits. As the Configuration Words are being loaded, for each bit loaded as '1', a complementary value of '0' is stored into its corresponding background word location and vice versa. The bit pairs are compared every time the Configuration Words are loaded, including Sleep mode. During this comparison, if the Configuration bit values are not found opposite to each other, a configuration mismatch event is generated, which causes a device Reset.

If a device Reset occurs as a result of a configuration mismatch, the CMR Status bit (RCON<9>) is set.

7.3.8 Deadman Timer Reset (DMTR)

Note:	This feature is not available on all devices. Refer to the **"Resets"** chapter in the specific device data sheet to determine availability.

A Deadman Timer (DMT) reset is generated when the DMT count has expired.

The primary function of the DMT is to reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

A DMT is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected.

7.3.9 Non-maskable Interrupt (NMI) Timer

The NMI timer provides a delay between DMT or WDT events and a device Reset. Set the delay in System Clock counts from 0 to 255 in the NMICNT<7:0> (RNMICON<7:0>) bits. If these bits are set to zero, there will be no delay between the DMTO or WDTO flag and a device Reset. If set to a non-zero value, the NMI interrupt has that number of system clocks to clear flags or save data for debugging purposes.

The DMTO flag will be set if there is a DMT event. The DMTO flag can be cleared in software during the NMI counter interval. If the DMTO flag is not cleared, the device will be reset after the NMI counter expires.

The WDTO flag will be set if there is a WDT event. The WDTO flag can be cleared in software during the NMI counter interval. If the WDTO flag is not cleared, the device will be reset after the NMI counter expires.

The WDTS flag will be set if there is a WDT event during Sleep mode. The WDTS flag will trigger the NMI interrupt, but will not start the NMI counter, nor cause a reset.

The CF (RNMICON<17>) bit may be set by the Fail-Safe Clock Monitor (FSCM) if there a clock failure is detected. The CF flag will trigger the NMI interrupt, but will not start the timer, nor cause a reset.

The SWNMI (RNMICON<23>) bit can be set in software to cause a NMI interrupt, but will not start the NMI counter, nor cause a reset.

7.3.10 Determining the Source of Device Reset

After a device Reset, the RCON register can be examined by initialization code to confirm the source of the reset. In certain applications, this information can be used to take appropriate action to correct the problem that caused the reset to occur.

All reset status bits in the RCON register should be cleared after reading them to ensure the RCON value will provide meaningful results after the next device Reset.

Example 7-2 illustrates how to determine the source of device Reset using the RCON register.

Example 7-2: Determining the Source of Device Reset

```
int main(void)
{
    //... perform application specific startup tasks

    // next, check the cause of the Reset
    if(RCON & 0x0003)
    {
        // execute a Power-on Reset handler
        // ...
    }
    else if(RCON & 0x0002)
    {
        // execute a Brown-out Reset handler
        // ...
    }
    else if(RCON & 0x0080)
    {
        // execute a Master Clear Reset handler
        // ...
    }
    else if(RCON & 0x0040)
    {
         // execute a Software Reset handler
        // ...
    }
    else if (RCON & 0x0200)
    {
        // execute a Configuration Mismatch Reset handler
        // ...
    }
    else if (RCON & 0x0010)
    {
        // execute Watchdog Time-out Reset handler
        // ...
    }
    else if (RCON & 0x0020)
    {
        // execute Deadman Timer time-out Reset handler
        // ...
    }

    //... perform other application-specific tasks

    while(1);
}
```

7.4 EFFECTS OF VARIOUS RESETS

The Reset value for the Reset Control register, RCON, will depend on the type of device Reset, as indicated in Table 7-2.

Table 7-2: Status Bits, Their Significance and the Initialization Condition for RCON Register

Condition	Program Counter	EXTR	SWR	WDTO	DMTO	SLEEP	IDLE	CMR	BOR	POR
Power-on Reset	0xBFC0_0000	0	0	0	0	0	0	0	1	1
Brown-out Reset		0	0	0	0	0	0	0	1	u
$\overline{\text{MCLR}}$ Reset during Run Mode		1	u	u	u	u	u	u	u	u
$\overline{\text{MCLR}}$ Reset during Idle Mode		1	u	u	u	u	1(1)	u	u	u
$\overline{\text{MCLR}}$ Reset during Sleep Mode		1	u	u	u	1(1)	u	u	u	u
Software Reset Command		u	1	u	u	u	u	u	u	u
Configuration Word Mismatch Reset		u	u	u	u	u	u	1	u	u
WDT Time-out Reset during Run Mode		u	u	1	u	u	u	u	u	u
WDT Time-out Reset during Idle Mode		u	u	1	u	u	1(1)	u	u	u
WDT Time-out Reset during Sleep Mode		u	u	1	u	1(1)	u	u	u	u
DMT Time-out Reset		u	u	u	1	u	u	u	u	u
Interrupt Exit from Idle Mode	Vector	u	u	u	u	u	1(1)	u	u	u
Interrupt Exit from Sleep Mode		u	u	u	u	1(1)	u	u	u	u

Legend: u = unchanged

Note 1: SLEEP and IDLE bits states are defined by previously executed WAIT instructions.

7.4.1 Special Function Register (SFR) Reset States

Most of the SFRs associated with the PIC32 CPU and peripherals are reset to a particular value at a device Reset. Reset values are specified in Table 7-2.

The reset value for the Reset Control register, RCON, will depend on the type of device reset.

7.4.2 Configuration Word Register Reset States

All Reset conditions force the configuration settings to be reloaded. The POR sets all the Configuration Word register locations to a '1' before loading the configuration settings. For all other Reset conditions, the Configuration Word register locations are not reset prior to being reloaded. This difference in behavior accommodates $\overline{\text{MCLR}}$ assertions during Debug mode without affecting the state of the debug operations.

Independent of the source of a reset, the system clock is always reloaded and is specified by the FNOSC<2:0> bits (DEVCFG<2:0>). When the device is executing code, the user software may change the primary system clock source by using the OSCCON register. For more information, refer to **Section 6. "Oscillator"** (DS60001112) or **Section 42. "Oscillators with Enhanced PLL"**.

7.4.3 Using the RCON Status Bits

The user software can read the RCON register after any system Reset to determine the cause of the reset. Table 7-3 provides a summary of the reset flag bit operation.

Note:	The Status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 7-3: Reset Flag Bit Operation

Flag Bit(1)	Set by	Cleared by
POR (RCON<0>)	POR	User Software
BOR (RCON<1>)	POR, BOR	User Software
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	User Software, POR, BOR
SWR (RCON<6>)	Software Reset command	User Software, POR, BOR
CMR (RCON<9>)	Configuration mismatch	User Software, POR, BOR
WDTO (RCON<4>)	WDT time-out	User Software, POR, BOR
DMTO (RCON<5>	DMT time-out	User Software, POR, BOR
SLEEP (RCON<3>)	`WAIT` instruction	User Software, POR, BOR
IDLE (RCON<2>)	`WAIT` instruction	User Software, POR, BOR

Note 1: All reset flag bits may be set or cleared by the user software.

7.4.4 Device Reset to Code Execution Start Time

The delay between the end of a reset event and when the device actually begins to execute code is determined by two main factors: the type of reset, and the system clock source coming out of the reset. The code execution start time for various types of device resets are summarized in Table 7-4. Individual delays are characterized in the **"Electrical Characteristics"** chapter of the specific device data sheet.

Table 7-4: Code Execution Start Time for Various Device Resets

Reset Type	Clock Source	Power-Up Delay(1,2,3,4)	System Clock Delay(1,5,6)	FSCM Delay(1,7)
POR	EC, FRC, FRCDIV, LPRC	(TPU or TPWRT) + TSYSDLY	—	—
	ECPLL, FRCPLL	(TPU or TPWRT) + TSYSDLY	TLOCK	TFSCM
	XT, HS, SOSC	(TPU or TPWRT) + TSYSDLY	TOST	TFSCM
	XTPLL, HSPLL	(TPU or TPWRT) + TSYSDLY	TOST + TLOCK	TFSCM
BOR	EC, FRC, FRCDIV, LPRC	TSYSDLY	—	—
	ECPLL, FRCPLL	TSYSDLY	TLOCK	TFSCM
	XT, HS, SOSC	TSYSDLY	TOST	TFSCM
	XTPLL	TSYSDLY	TOST + TLOCK	TFSCM
$\overline{\text{MCLR}}$, CMR, SWR, WDTO, DMTO	Any Clock	TSYSDLY	—	—

Note 1: For parameter specifications, see the **"Electrical Characteristics"** chapter of the specific device data sheet.

2: TPU = Power-up Period with on-chip regulator enabled.

3: TPWRT = Power-up Period (Power-up Timer) with on-chip regulator disabled.

4: TSYSDLY = Time required to reload Device Configuration Fuses plus eight SYSCLK cycles.

5: TOST = Oscillator Start-up Timer.

6: TLOCK = PLL lock time.

7: TFSCM = Fail-Safe Clock Monitor delay.

7.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Resets are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

7.6 REVISION HISTORY

Revision A (September 2007)

- This is the initial released version of this document.

Revision B (October 2007)

- Updated document to remove Confidential status.

Revision C (April 2008)

- Revised status to Preliminary; Revised U-0 to r-x.

Revision D (June 2008)

- Revised Figure 7-2; Deleted Figure 7-3; Revised Sections 7.3.2, 7.3.3, 7.3.4; Revised Table 7-4; Delete Figure 7.2 and 7.3; Change Reserved bits from “Maintain as” to “Write”.

Revision E (July 2008)

- Revised Section 7.3.2, 7.3.3, 7.3.6, 7.4.4.

Revision F (October 2011)

This revision includes the following updates:

- Added a Note at the beginning of the section, which provides information on the complementary documentation
- Changed the document running header from PIC32MX Family Reference Manual to PIC32 Family Reference Manual
- Changed all occurrences of PIC32MX to PIC32
- Removed the following Clear, Set and Invert registers:
  - RCONCLR: Reset Control Clear Register
  - RCONSET: Reset Control Set Register
  - RONINV: Reset Control Invert Register
  - RSWRSTCLR: Software Reset Clear Register
  - RSWRSTSET: Software Reset Set Register
  - RSWRSTINV: Software Reset Invert Register
- Added Notes to Register 7-1 and Register 7-2 describing their corresponding Set, Clear and Invert registers
- Updated all r-x bits as U-0 bits in Register 7-1 and Register 7-2
- Updated Example 7-1
- Relocated and renamed 7.5 “Design Tips” to 7.3.8 “Determining the Source of Device Reset”
- Modifications to register formatting and minor text updates have been made throughout the document

Revision G (November 2013)

This revision includes the following updates:

- The document was updated to include Deadman Timer information
- Updated the system reset block diagram (see Figure 7-1)
- Updated the Reset SFR Summary (see Table 7-1)
- Added new paragraphs describing the Non-maskable Interrupt Reset (see **7.2 “Control Registers”**)
- Updated the Reset Control Register (see Register 7-1)
- Updated the Software Reset Register (see Register 7-2)
- Added the Non-Maskable Interrupt (NMI) register (see Register 7-3)
- Added the Power Control Register (see Register 7-4)
- Added the WDTO Status bit and Reset information toTable 7-2,Table 7-3, and Table 7-4
- Added **7.3.8 “Deadman Timer Reset (DMTR)”**
- Added **7.3.9 “Non-maskable Interrupt (NMI) Timer”**
- Updated Example 7-2: Determining the Source of Device Reset
- Minor updates to text and formatting were incorporated throughout the document

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