PIC32MX1XX/2XX Family
Silicon Errata and Data Sheet Clarification

The PIC32MX1XX/2XX family devices that you have received conform functionally to the current Device Data Sheet (DS61168**E**), except for the anomalies described in this document.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX silicon.

Note: The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 and Table 2. The last column of each table represents the latest silicon revision for the devices listed. The silicon issues are summarized in Table 3.

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various silicon revisions are provided in Table 1 and Table 2.

TABLE 1: SILICON DEVREV VALUES FOR DEVICES WITH 16/32 KB FLASH

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	A1
PIC32MX110F016B	0x04A07053	0x0	0x1
PIC32MX110F016C	0x04A09053		
PIC32MX110F016D	0x04A0B053		
PIC32MX210F016B	0x04A01053		
PIC32MX210F016C	0x04A03053		
PIC32MX210F016D	0x04A05053		
PIC32MX120F032B	0x04A06053		
PIC32MX120F032C	0x04A08053		
PIC32MX120F032D	0x04A0A053		
PIC32MX220F032B	0x04A00053		
PIC32MX220F032C	0x04A02053		
PIC32MX220F032D	0x04A04053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS61168**E**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON DEVREV VALUES FOR DEVICES WITH 64/128 KB FLASH

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	A1
PIC32MX130F064B	0x04D07053	0x0	0x1
PIC32MX130F064C	0x04D09053		
PIC32MX130F064D	0x04D0B053		
PIC32MX230F064B	0x04D01053		
PIC32MX230F064C	0x04D03053		
PIC32MX230F064D	0x04D05053		
PIC32MX150F128B	0x04D06053		
PIC32MX150F128C	0x04D08053		
PIC32MX150F128D	0x04D0A053		
PIC32MX250F128B	0x04D00053		
PIC32MX250F128C	0x04D02053		
PIC32MX250F128D	0x04D04053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS61168**E**) for detailed information on Device and Revision IDs for your specific device.

TABLE 3: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Device		
				Flash Memory (KB)	Silicon Revision	
					A0	A1
Voltage Regulator	BOR	1.	Device may not exit Brown-out Reset (BOR) state if a BOR event occurs.	16/32	X	
				64/128	X	
Oscillator	Clock Switch	2.	If a Fail-Safe Clock Monitor (FSCM) event occurs when Primary Oscillator (POSC) mode is used, firmware clock switch requests to switch from FRC mode will fail.	16/32	X	X
				64/128	X	X
I^2C™	Slave Mode	3.	The I^2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	16/32	X	X
				64/128	X	X
USB	UIDLE Interrupt	4.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	16/32	X	X
				64/128	X	X
ADC	—	5	The DNL parameter of the ADC module is not within the published data sheet specifications when the ADC module is operating at maximum conversion rate.	16/32	X	X
				64/128	X	X
ADC	CTMU Calibration	6.	Open selection for Channel 0 positive input is not functional.	16/32	X	X
				64/128		
ADC	Conversion Trigger from INT0 Interrupt	7.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	16/32	X	X
				64/128	X	X
Parallel Master Port (PMP)	Address Pins	8.	When the Parallel Master Port (PMP) module is enabled, address pins cannot be used as GPIO output pins.	16/32	X	X
				64/128	X	X
I/O Ports	RA0 and RA1 Pins	9.	Output High Voltage (VOH) and internal capacitance on pins RA0 and RA1 is not within the published data sheet specification.	16/32	X	X
				64/128	X	X
CPU	Data Write to a Peripheral	10.	A data write operation by the CPU to a peripheral may be repeated if an interrupt occurs during initial write operation.	16/32	X	X
				64/128	X	X
Oscillator	Clock Out	11.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	16/32	X	X
				64/128	X	X
Input Capture	Idle Mode and Sleep Mode	12.	All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle mode or Sleep mode.	16/32	X	X
				64/128	X	X
Watchdog Timer (WDT)	Windowed Mode	13.	The Watchdog Timer may issue a reset even if the user tries to clear the module within the allowed window.	16/32	X	X
				64/128	X	X
Non-5V Tolerant Pins	Pull-ups	14.	Internal pull-up resistors may not guarantee a logical ‘1’ on non-5V tolerant pins when they are configured as digital inputs.	16/32	X	X
				64/128	X	X
5V Tolerant Pins	Pull-ups	15.	Internal pull-up resistors may not guarantee a logical ‘1’ on 5V tolerant pins when they are configured as digital inputs.	16/32	X	X
				64/128	X	X

Legend: An ‘X’ indicates the issue is present in this revision of silicon;
Shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue;
Blank cells indicate an issue has been corrected in this revision of silicon.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon based on memory size.

1. Module: Voltage Regulator

Device may not exit the Brown-out Reset (BOR) state if a BOR event occurs.

Work arounds

Work around 1:

VDD must remain within the published specification (see parameter DC10 of the device data sheet).

Work around 2:

Reset the device by providing the Power-on Reset (POR) condition.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X					
64/128	X					

2. Module: Oscillator

If the Primary Oscillator (POSC) mode is implemented and a Fail-Safe Clock Monitor (FSCM) event occurs (failure of the external primary clock), the internal clock source will switch to the FRC oscillator. Subsequent firmware clock switch requests from the FRC oscillator to other clock sources will fail and the device will continue to execute on the FRC oscillator. On repair of the external clock source and a power-on state, the device will resume operation with the primary oscillator clock source.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

3. Module: I²C™

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I²C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but it does not.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

4. Module: USB

If the bus has been idle for more than 3 ms, the UIDLE interrupt flag is set. If software clears the interrupt flag and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption (i.e., Resume, Reset, SOF, or Error).

Note:	Resume and Reset are the only interrupts that should be following UIDLE assertion. If the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

5. Module: ADC

If the ADC module is configured to operate at a maximum conversion rate of 1.1 Msps, missing codes are possible every 2^5 codes and the DNL parameter will not be within the published specification.

Work around

Configure the ADC module to operate for a maximum conversion rate of 500 ksps.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

6. Module: ADC

If the ADC module is used in conjunction with the CTMU module in Absolute Capacitive/Time Measurement mode, Channel 0 positive input must remain open (CH0SA<3:0> = 1111 or CH0SB<3:0> = 1111) during the calibration step. However, open selection for Channel 0 positive input is not functional and connects this input to AVSS.

Work around

Connect the ADC module to any unused pin and perform the CTMU calibration step. This connection will add a small amount of additional capacitance, but will have minimal impact on overall measurements.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128						

7. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternately, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

8. Module: Parallel Master Port (PMP)

If the PMP module is enabled, any pin with a PMP addressing capability (PMAx) cannot be used as a general purpose output pin, even when the corresponding PTEN<10:0> bit in the PMAEN register is cleared. All other functionality on these pins, including GPIO input functionality is not affected.

Work around

To use a GPIO pin as an output when this pin is shared with PMP addressing functionality and PMP is enabled, do the following:

1. Enable PMP addressing by setting the corresponding PTEN<10:0> bit in the PMAEN register.
2. Instead of using corresponding LATx registers to output GPIO data, use the PMADDR register.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

9. Module: I/O Ports

Output High Voltage (V_{OH}) on the RA0 and RA1 pins is not within the published data sheet specification if the I2C1 module is enabled. In addition, internal capacitance on these pins is one and one-half (1.5) and two times higher, respectively, than other I/O ports.

Work around

Disable slew rate control of the I2C1 module by setting the DISSLW bit (I2C1CON<9>).

There is no workaround for higher capacitance.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

10. Module: CPU

During normal operation, if a CPU write operation is interrupted by an incoming interrupt, it should be aborted (not completed) and resumed after the interrupt is serviced. However, some of these write operations may not be aborted, resulting in a double write to peripherals by the CPU (the first write during the interrupt and the second write after the interrupt is serviced).

Work around

Most peripherals are not affected by this issue, as a double write will not have a negative impact. However, the following communication peripherals will double-send data if their respective transmit buffers are written twice: SPI, I^2C, UART and PMP. To avoid double transmission of data, utilize DMA to transfer data to these peripherals or disable interrupts while writing to these peripherals.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

11. Module: Oscillator

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

12. Module: Input Capture

All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle or Sleep mode.

Work around

Configure the Input Capture module for Interrupt-only mode (ICM<2:0> = 111) when the CPU is in Sleep or Idle mode.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

13. Module: Watchdog Timer (WDT)

When the Watchdog Timer module is used in Windowed mode, the module may issue a reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

14. Module: Non-5V Tolerant Pins

When internal pull-ups are enabled on non-5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

15. Module: 5V Tolerant Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1				
16/32	X	X				
64/128	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS61168**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: DC Characteristics: I/O Pin Input Specifications

Certain specifications in Table 29-8 were stated incorrectly in the data sheet. The correct values are shown in bold type in the following table.

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical(1)	Max.	Units	Conditions
	VIH	Input High Voltage					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	(Note 4,**6**)
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	(Note 4,**6**)
		I/O Pins 5V-tolerant(5)	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled (Note 4,**6**)
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,**6**)
DI30	ICNPU	Change Notification Pull-up Current	**—**	**—**	**-50**	µA	VDD = 3.3V, VPIN = VSS (Note 3, **6)**
DI31	ICNPD	Change Notification Pull-down Current(4)	—	50	—	µA	VDD = 3.3V, VPIN = VDD

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the "Pin Diagrams" section for the 5V-tolerant pins.

6: The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

APPENDIX A: REVISION HISTORY

Rev A Document (10/2011)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (Voltage Regulator), 2 (Oscillator), 3 (I^2C™), 4 (USB), 5 (ADC), 6 (ADC), 7 (ADC), 8 (Parallel Master Port (PMP)), and 9 (I/O Ports).

Rev B Document (2/2012)

Added silicon revision A1 for 16/32 KB Flash devices.

Added 64/128 KB Flash devices.

Added silicon issues 10 (CPU) and 11 (Oscillator).

Rev C Document (4/2012)

Updated silicon issue 10 (CPU).

Added silicon issue 12 (Input Capture).

Rev D Document (10/2012)

Updated silicon issue 6 (ADC).

Added silicon issue 13 (Watchdog Timer (WDT)).

Updated the note in the Silicon DEVREV Values tables (see Table 1 and Table 2).

Rev E Document (4/2013)

Updated the Device ID for the PIC32MX150F128B in Table 2.

Updated silicon issue 9 (I/O Ports).

Added silicon issues 14 (Non-5V Tolerant Pins) and 15 (5V Tolerant Pins).

Added data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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