NMAM INSTITUTE OF TECHNOLOGY, NITTE

Off-Campus Centre of Nitte (Deemed to be University)

I Sem B.Tech. (CBCS) Mid Semester Examinations - I, September 2022

Duration: 1 Hour — EC1002-1 – APPLIED DIGITAL LOGIC DESIGN — Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	Convert the hexadecimal number $A6.7_{16}$ to binary by using decimal representation of the number. Verify the result using direct conversion.	5	L*3	1	1
	b)	Given the simplified expression of a Boolean function, write the truth table, minterm list and obtain the given simplified function using K-map method. $Y = f(a, b, c) = c'$	5	L3	2	1
2.	a)	Design a combinational logic circuit to generate an output whenever a majority of four inputs is logic 1 and output function is not specified whenever the number of 0's and 1's is equal in the inputs. However, the output is logic zero for the remaining conditions.	5	L3	2	1
	b)	Prove the commutative law using truth table method for both the law of addition and law of multiplication.	5	L2	1	1
		Unit – II				
3.	a)	Design a combinational logic circuit to generate an output of logic 1 whenever the result of multiplication of two numbers of 2-bits each is non zero.	6	L3	2	1
	b)	Realize the given Boolean expression using NOR gates only. Also draw the logic diagram using NOR gates only. $R=f(A, B, C D) = ABC+BC'D+A'BC$	4	L3	1	1
4.	a)	Simplify the given Boolean expression using QM technique. $G = f(a, b, c d) = \sum(1, 3, 5, 7, 13, 15)$	6	L3	2	1
	b)	An exam consisted of three questions Q1, Q2 and Q3, where the marks allotted for Q1, Q2 and Q3 were four, two and one respectively. The minimum qualifying marks for the exam was three. Implement a combinational logic circuit which indicated whether the student has qualified in the exam or not.	4	L3	2	1

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

Off-Campus Centre of Nitte (Deemed to be University)

I Sem B.Tech. (CBCS) Mid Semester Examinations - II, November 2022

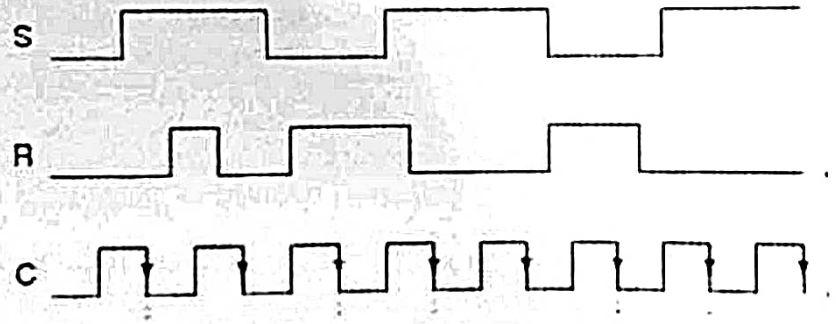
EC1002-1 – APPLIED DIGITAL LOGIC DESIGN

Duration: 1 Hour

Max. Marks: 20

Note: Answer any One full question from each Unit.

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	With a neat diagram illustrate the design of full adder using two half adders.	4	L*2	3	1
	b)	Implement the function F(A,B,C,D)=∑m(6,7,9,10,13) using 8:1 multiplexer.	6	L3	3	2
2.	a)	Implement u=a+bc' using 4:1 Mux.	5	L3	3	2
	b)	Design a circuit using 3:8 decoder and OR gates that realizes following functions - f1(A,B,C)=∑m(0,4,6), f2=A'+AC.	5	L3	3	2
		Unit – II				
3.	a)	Give the characteristic equation of T flip-flop and SR flip-flop.	5	L1	4	1
	b)	Explain the operation of master-slave JK flip-flop with truth table and timing diagram.	5	L2	4	1
4.	a)	Draw the output for the S, R and clock input as shown in below figure. Consider - ve edge of the clock.	4	L3	4	2



	b)	Write a note on i. Latch ii. Flip-flop iii. Characteristic equation of D flip-flop	6	L1	4	1

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