NAGADASTAGIRI CHALLAPALLE

Email-id: dastagiri.c@gmail.com,
Mobile No.: +14696058910

ACADEMIC DETAILS

Degree	Institute	Year	CPI / Percentage
Ph.D (Computer Science and Engineering)	The Pennsylvania State University, UP	2021*	3.91 (on 4pt scale)
M.Tech. (Electrical Engineering)	Indian Institute of Technology Kanpur, Kanpur	2016	10 (on 10pt scale)
B.Tech. (Electronics and Communications Engineering)	Amrita School of Engineering, Bangalore	2011	8.18 (on 10pt scale)

*Expected year of completion

CURRENT WORK

- Hardware accelerator architectures for deep learning architectures and graph analytics with focus on processing-in-memory and approximate computing
- Exploring the emerging devices and technologies such as crossbar based non-volatile memories, monolithic 3D integration for enabling compute in memory.

AREAS OF INTEREST

- Hardware Accelerators, Computer Architecture, Digital Circuits and VLSI, Neural Networks and Deep Learning, Graph Analytics

WORK EXPERIENCE

- Research Intern — AMD Research — May'20 - Aug'20
  - Working on architectural modifications to CPU core and SoC pipelines to leverage the PIM capabilities of emerging main memory systems such as HBM
- Hardware Engineer — Intel Labs — June'16 - Dec'17
  - Worked in Microarchitecture Research Lab (MRL), Intel Labs, Bangalore.
  - Member of Hardware accelerators team, working on accelerating compute intensive aspects of Computer vision and Deep learning algorithms in ASIC. Primary responsibilities include Architecture exploration, RTL design, Power/Performance optimizations and verification.
- Systems Engineer — Infosys Limited — June'11 - Apr'13
- Senior Systems Engineer — Infosys Limited — May'13 - June'14
  - Worked in Education & Research vertical of Infosys Limited.
  - Worked in automation of Mainframe jobs scheduling and error recovery.

SCHOLASTIC ACHIEVEMENTS

- Outstanding TA award - 2016, Department of Electrical Engineering, Indian Institute of Technology Kanpur.
- Academic excellence award - 2015, Indian Institute of Technology Kanpur.
- Won first prize in "NETWARZ", a computer networking competition held jointly by CISCO Ltd. & Amrita Vishwa Vidyapeetham in october 2009.

TECHNICAL SKILLS

- **Languages:** System Verilog, Python, C, C++
- **Tools:** Questa ModelSim, Quartus Prime and QSys, Synopsys VCS, Synopsys Design Compiler, LaTeX, MATLAB

PUBLICATIONS

- Nagadastagiri Challapalle, Makesh Chandran, Sahithi Rampalli, and Vijaykrishnan Narayanan, "X-VS: Crossbar-based Processing-in-Memory Architecture for Video Summarization", ISVLSI 2020.
- Nagadastagiri Challapalle, Sahithi Rampalli, John Sampson, and Vijaykrishnan Narayanan, "FARM: A Flexible Accelerator for Recurrent and Memory Augmented Neural Networks", Journal of Signal Processing Systems, Springer, 2020.

- Nagadastagiri Challapalle, Sahithi Rampalli, Linghao Song, Nandhini Chandramoorthy, Karthik Swaminathan, John Sampson, Yiran Chen, Vijaykrishnan Narayanan, "GaaS-X: Graph Analytics Accelerator Supporting Sparse Data Representation using Crossbar Architectures" ISCA 2020.
- Nagadastagiri Challapalle, Sahithi Rampalli, Tarun Chandran, Gurpreet Kalsi, John Sampson, Sreenivas Subramoney, and Vijaykrishnan Narayanan, "PSB-RNN: A Processing-in-Memory based Systolic Array Architecture for Recurrent Neural Networks", DATE 2020.
- Skyler Anderson, Nagadastagiri Challapalle, John Sampson, and Vijaykrishnan Narayanan, "Adaptive Neural Network Architectures for Power Aware Inference", IEEE Design & Test 2019.
- P. Cadareanu, N. Reddy C, C. G. Almudever, A. Khanna, A. Raychowdhury, S. Datta, K. Bertels, V. Narayanan, M. Di Ventra, P. E. Gaillardon, "Rebooting Our Computing Models", DATE 2019.

PATENTS

- Dipan Mandal, Nagadastagiri Reddy C, Mahesh Mamidipaka and Omer Om J , "Hardware architecture for On-the-fly, ultra-low-latency Image Feature Detection, Sorting and Tracking" [US Patent filed in 2018].
- Sreenivas Subramoney, Srivastava Jandhyala, Mahesh Mamidipaka, Anish NK and Nagadastagiri Reddy C, "Hardware accelerator for selecting data elements" [US Patent filed in 2017].

ACADEMIC PROJECTS

- **Distributed Key-Value store using LSM Tree and ABD algorithm** Designed and implemented a distributed key value store using Log-Structured Merge(LSM) Tree as the data layout mechanism and the ABD algorithm to maintain the consistency across the different servers.
- **Surround Sensing** Surround Sensing/Obstacle Detection using RF Waves. Explored the possibility of using RF reflections from surroundings to localize the object. RF sensing over comes the limitations of GPS and vision based localization. It works well in low altitude surroundings and also doesn't depend on visibility.
- **Operating Systems Projects**
  - Designed and programmed a dynamic storage allocator (programmed malloc, free and realloc routines).
  - Coded channels with send, receive, close, destroy and select functionality.
  - Programmed system calls, mutexes, condition variables, semaphores and reader/writer locks for a miniature operating system called Pebbles.

RELEVANT COURSEWORK

- Computer Organization and Architecture, Operating Systems, IoT, Digital Systems, Pattern Recognition and Machine Learning, Computer Vision, Electronic Systems I & II, Embedded Systems
- Computer Architecture (Coursera), Analysis of Algorithms (Coursera), Neural Networks and Deep Learning (Coursera), Computational Neuroscience (Coursera), Introduction to Computer Science and Programming Using Python (Edx)