

Assembly Language			INSTRUCTION bit fields						Control PLAs										
MNEMONIC	ARGS	OPCODE binary	OP 31:26	RS 25:21	RT 20:16	RD 15:11	SA 10:6	FUNC 5:0	ALU	SH AMT	se	imm	C SEL	PC s1	PC s0	ret addr	dm EN*	dm WR*	load
sll	rd,rt,n	00 0000	0	0	rt	rd	n	0	func	sa	0	0	rd	0	0	0	1	1	0
srl	rd,rt,n	00 0000	0	0	rt	rd	n	2	func	sa	0	0	rd	0	0	0	1	1	0
sra	rd,rt,n	00 0000	0	0	rt	rd	n	3	func	sa	0	0	rd	0	0	0	1	1	0
sllv	rd,rt,rs	00 0000	0	rs	rt	rd	0	4	func	rs	0	0	rd	0	0	0	1	1	0
srlv	rd,rt,rs	00 0000	0	rs	rt	rd	0	6	func	rs	0	0	rd	0	0	0	1	1	0
srav	rd,rt,rs	00 0000	0	rs	rt	rd	0	7	func	rs	0	0	rd	0	0	0	1	1	0
jr	rs	00 0000	0	rs	0	0	0	8	func	sa	0	0	rd	1	1	0	1	1	0
jalr	rs,rd	00 0000	0	rs	0	rd	0	9	func	sa	0	0	rd	1	1	1	1	1	0
add	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x20	func	sa	0	0	rd	0	0	0	1	1	0
addu	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x21	func	sa	0	0	rd	0	0	0	1	1	0
sub	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x22	func	sa	0	0	rd	0	0	0	1	1	0
subu	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x23	func	sa	0	0	rd	0	0	0	1	1	0
and	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x24	func	sa	0	0	rd	0	0	0	1	1	0
or	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x25	func	sa	0	0	rd	0	0	0	1	1	0
xor	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x26	func	sa	0	0	rd	0	0	0	1	1	0
nor	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x27	func	sa	0	0	rd	0	0	0	1	1	0
slt	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x2a	func	sa	0	0	rd	0	0	0	1	1	0
sltu	rd,rs,rt	00 0000	0	rs	rt	rd	0	0x2b	func	sa	0	0	rd	0	0	0	1	1	0
bgez	rs,label	00 0001	1	rs	0x1	Instruction offset			0	0	0	0	0	0	!n	0	1	1	0
bgezal	rs,label	00 0001	1	rs	0x11	Instruction offset			0	0	0	0	0x1f	0	!n	1	1	1	0
bltz	rs,label	00 0001	1	rs	0x0	Instruction offset			0	0	0	0	0	0	n	0	1	1	0
bltzal	rs,label	00 0001	1	rs	0x10	Instruction offset			0	0	0	0	0x1f	0	n	1	1	1	0
j	label	00 0010	2	Destination Address 27:2					0	0	0	0	0	1	0	0	1	1	0
jal	label	00 0011	3	Destination Address 27:2					0	0	0	0	0x1f	1	0	1	1	1	0
beq	rs,rt,label	00 0100	4	rs	rt	Instruction offset			0	0	0	0	rt	0	eq	0	1	1	0
bne	rs,rt,label	00 0101	5	rs	rt	Instruction offset			0	0	0	0	rt	0	!eq	0	1	1	0
blez	rs,label	00 0110	6	rs	0	Instruction offset			0	0	0	0	0	0	n eq	0	1	1	0
bgtz	rs,label	00 0111	7	rs	0	Instruction offset			0	0	0	0	0	0	!n&&!eq	0	1	1	0
addi	rt,rs,imm	00 1000	8	rs	rt	IMMEDIATE			0x20	0	1	1	rt	0	0	0	1	1	0
addiu	rt,rs,imm	00 1001	9	rs	rt	IMMEDIATE			0x21	0	1	1	rt	0	0	0	1	1	0

slti	rt,rs,imm	00 1010	0xA	rs	rt	IMMEDIATE	0x2a	0	1	1	rt	0	0	0	1	1	0
sltiu	rt,rs,imm	00 1011	0xB	rs	rt	IMMEDIATE	0x2b	0	1	1	rt	0	0	0	1	1	0
andi	rt,rs,imm	00 1100	0xC	rs	rt	IMMEDIATE	0x24	0	0	1	rt	0	0	0	1	1	0
ori	rt,rs,imm	00 1101	0xD	rs	rt	IMMEDIATE	0x25	0	0	1	rt	0	0	0	1	1	0
xori	rt,rs,imm	00 1110	0xE	rs	rt	IMMEDIATE	0x26	0	0	1	rt	0	0	0	1	1	0
lui	rt,imm	00 1111	0xF	0	rt	IMMEDIATE	0	0x10	0	1	rt	0	0	0	1	1	0
lw	rt,addr(rs)	10 0011	0x23	rs	rt	BYTE OFFSET	0x21	0	1	1	rt	0	0	0	1	0	1
sw	rt,addr(rs)	10 1011	0x2B	rs	rt	BYTE OFFSET	0x21	0	1	1	0	0	0	0	0	0	0
