EE 140/240A discussion 2

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Outline

- Circuit Analysis vs Modeling
- Biasing Scheme
- When to approximate?
- Analysis Example

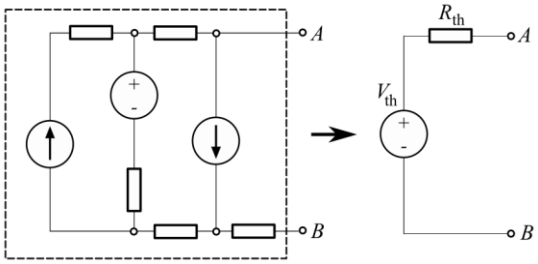
Stages of Circuit Analysis

1. Small Signal Model + KCL/KVL (EE 105).
   - The Golden Standard; gives you the 100% correct answer.
   - Too slow to do, no intuition of how the circuit works.
   - Fallback option on exams/interviews.
2. Inspection Analysis (EE 140).
   - Memorize solution to common circuit configuration.
     - It is recommended to memorize exact formula in case assumption break.
   - Offers some circuit intuition.
3. Current Flow Intuition.
   - Completely intuition driven.
   - Comes only after thousands of practices.

Circuit Analysis vs Modeling

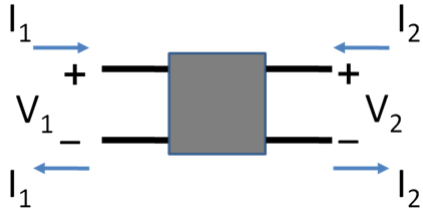
- Circuit analysis is given a circuit configuration, calculate its properties (gain, input impedance, etc.)
- Modeling is given a (possibly unknown) circuit, find the simplest equivalent circuit that captures all the properties of interest.
- Good models can simplify complex circuits and provide valuable insights into how it works.

1 Port Circuit Modeling



- Thévenin's/Norton's Theorem: Any **linear** circuit can be modeling as a voltage/current source in series/parallel to a resistor.
- Proof: Because we know it's linear, We must have $V_1 = V_{bias} - Z_{eq}I_1$, or $I_1 = I_{bias} + V_1/Z_{eq}$

2 Port Circuit Modeling



- We now have 4 variables, V_1, V_2, I_1, and I_2.
- Since it's linear, we can write:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

  - Why is this? **Superposition Principle**
- A 2 port circuit can be completely described by 4 parameters.

2 Port Circuit Modeling

- We can derive:

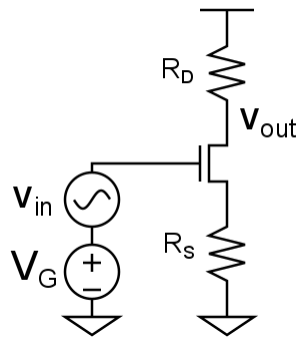
$$y_{11} = \frac{I_1}{V_1}\Big|_{V_2=0} \quad y_{12} = \frac{I_1}{V_2}\Big|_{V_1=0}$$

$$y_{21} = \frac{I_2}{V_1}\Big|_{V_2=0} \quad y_{22} = \frac{I_2}{V_2}\Big|_{V_1=0}$$

- For a transistor, we see that $y_{11} = \infty$, $y_{12} = 0$, $y_{21} = g_m$, and $y_{22} = 1/r_o$.
- For more information, Wikipedia has a good article.
  - Will revisit 2-port networks for feedback analysis near the end of the semester.

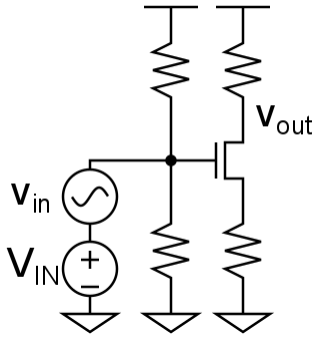
Biasing

- Circuit Design is 95% biasing - Ali Niknejad.
- How to bias the gate of a transistor?
- Following picture is ideal, but restrict previous stage to work with sub-optimal bias point.



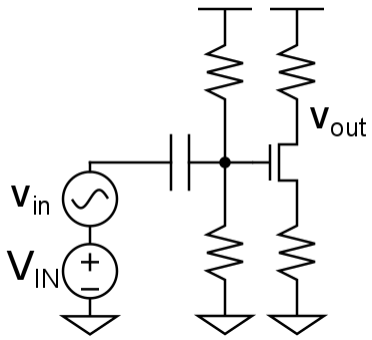
Biasing

- Doesn't work: input DC bias voltage overrides resistor divider network.
- We want to disconnect the input at DC.



Biasing

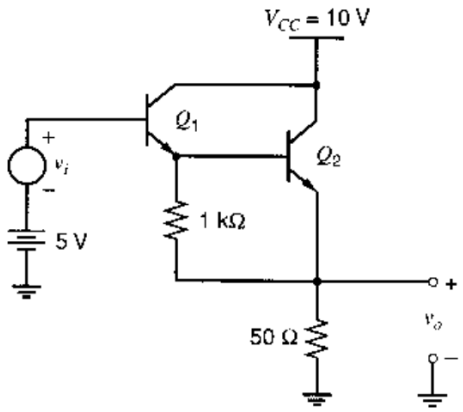
- Add a capacitor.
- $Z_C = \frac{1}{jwC}$
  - at DC ($w = 0$), infinite impedance -> open.
  - At frequencies for which $wC \gg 1$, 0 impedance -> short.
  - Pick C such that $wC \gg 1$ for all frequencies of interest.



When to approximate?

- Engineers are not mathematicians; we are lazy and only do minimum amount of work.
- Each specification usually comes with an error tolerance; as long as your approximation is within error tolerance, you're fine.
- In this class, unless otherwise stated, 10% error is acceptable.
- **ALWAYS** double check if assumption is valid!

Analysis Example

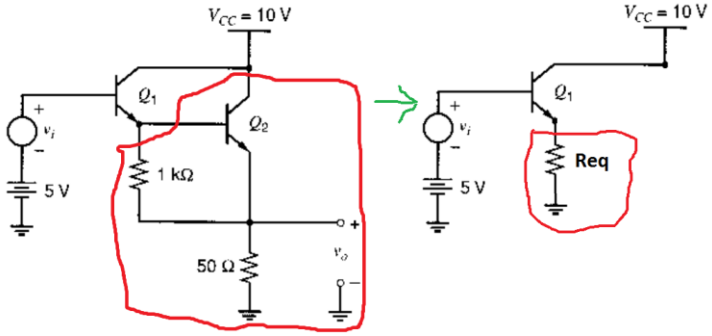


- Find bias currents, input/output resistance, and voltage gain. Ignore r_o, and $V_{BE(on)} = 0.7\text{V}, \beta_0 = 200.$

DC operating point

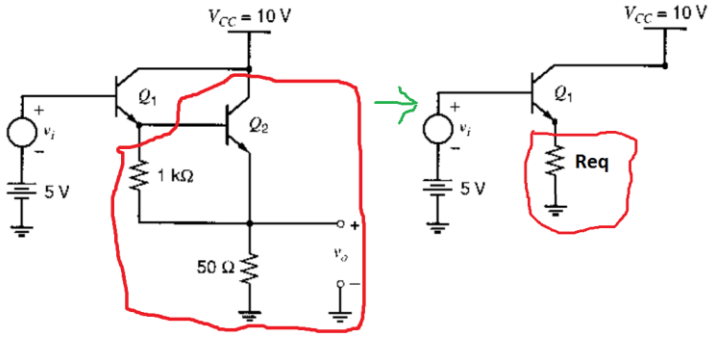
- $V_{E1} = 5 - V_{BE(on)} = 4.3\text{V}$
- $V_{E2} = V_{E1} - V_{BE(on)} = 3.6\text{V}$
- $I_{Q2} = \frac{V_{E2}}{50} - \frac{V_{E1}-V_{E2}}{1000} = 71.3\text{mA}$
- $g_{m2} = \frac{I_{Q2}}{V_T} = 2.74\text{S}, r_{\pi 2} = \frac{\beta_0}{g_{m2}} = 73\Omega,$
  $i_{b2} = \frac{I_{Q2}}{\beta_0} = 357\mu\text{A}$
- $I_{Q1} = \frac{V_{E1}-V_{E2}}{1000} + i_{b2} = 1.06\text{mA},$
  $g_{m1} = \frac{I_{Q1}}{V_T} = 40.8\text{mS}, r_{\pi 1} = \frac{\beta_0}{g_{m1}} = 4.9\text{k}\Omega$

Input impedance



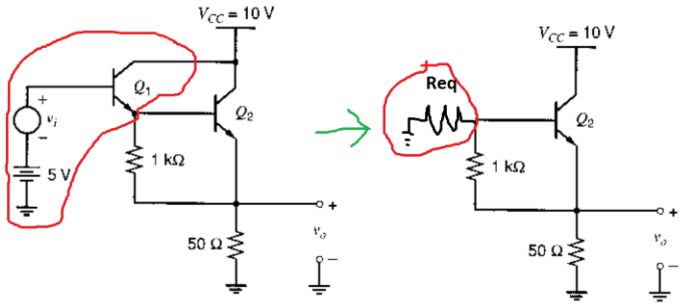
- We can put Q2 in a black box, and since it only has 1 port, we can replace it by an equivalent resistance.
- $1\text{k}\Omega$ transistor in parallel with $r_{\pi 2} = 73\Omega$, so we can ignore it.
  - Circuit in red box is effectively an emitter degenerated npn transistor.

Input impedance



- Using inspection formulas:
  - $R_{eq2} = r_{\pi 2} + (\beta_0 + 1)50 = 10.1\text{k}\Omega$
  - $r_{in} = r_{\pi 1} + (\beta_0 + 1)R_{eq2} = 2.04\text{M}\Omega$

Output Impedance



- Similarly, we can blackbox Q1 and find equivalent resistance.
- Inspection formula gives:
  - $R_{eq1} = \frac{1}{g_{m1}} = 24.5\Omega.$
  - $r_{e2} = \frac{1}{g_{m2}} + \frac{R_{eq}}{\beta_0 + 1} = 0.49\Omega$
  - $r_{out} = \left(\frac{1}{r_{e2}} + \frac{1}{50}\right)^{-1} = 0.49\Omega$

Gain

- Blackboxing also works for computing the gain of each stage.
- $A_{v1} = \frac{R_{eq2}}{R_{eq2}+r_{e1}} = \frac{R_{eq2}}{R_{eq2}+R_{eq1}} = \frac{10100}{10100+24.5} \approx 1$
- $A_{v2} = \frac{50}{50+r_{e2}} = \frac{50}{50+0.48} \approx 1$
- $A_v = A_{v1}A_{v2} = 1$