Questions and comments:

1. Do you have a presentation or material you would like to share that shows the physical structure of the terminals that you would like to include in the JEP-30 Part Model schema? (Support physical definitions of internal connections – i.e. C4 bumps both on upper and lower sides, TSV’s Thru Silicon Vias)
2. Are there any specific requirements for the multi-mode of operations of the terminals that should be captured in the JEDEC standards? (Multi-mode operations / Multi-Functional Terminals)
3. Are there any requirements for the hierarchical interfaces that should be captured? (Support Hierarchical Interfaces)

CDXML

| Signal\_group | Str |  | Used for grouping such as a bus or a pair sharing similar constraints. This should correspond to the mode for Pin\_name entry. |
| --- | --- | --- | --- |
| Int |  | Index - index of the pin in a group of signals. |
| Netlist\_name | Str |  | Default netname used internally (schematic can override). |
| Pin\_mode | Str |  | Mode - Mode of operation. Pins that are used for multiple usages can be described with multiple entries, but each mode should have a unique mode index. Valid values include 0,1,2.... |
| Int |  | Index - Index of Mode of operation. The total number of modes the current pin has. Most of the pins will have only one mode. |

CDXML to PM mapping

| cdxml/io/pin/pin\_mode/id | Integer | cdxml | io | pin | pin\_mode | id | PartModel/ElectricalSection/ElectricalParameters-Array/ElectricalParameters/TerminalDetails-Array/TerminalDetails/Properties-Array/Properties/ID | String |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| cdxml/io/pin/pin\_mode/name | String | cdxml | io | pin | pin\_mode | name | PartModel/ElectricalSection/ElectricalParameters-Array/ElectricalParameters/TerminalDetails-Array/TerminalDetails/Properties-Array/Properties | PropertiesType |
| cdxml/io/pin/signal\_mode/id | Integer | cdxml | io | pin | signal\_mode | id | PartModel/ElectricalSection/ElectricalParameters-Array/ElectricalParameters/TerminalDetails-Array/TerminalDetails/TerminalFunction-Array/TerminalFunction/ID | String |
| cdxml/io/pin/signal\_mode/name | String | cdxml | io | pin | signal\_mode | name | PartModel/ElectricalSection/ElectricalParameters-Array/ElectricalParameters/TerminalDetails-Array/TerminalDetails/TerminalFunction-Array/TerminalFunction/DigitalFunction | DigitalFunctionType |

| cdxml/io/pin/netlist\_name | String | cdxml | io | pin | netlist\_name |  | Default netname used internally (schematic can override) |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |

Main common chiplet physical interface:

1. C4 Bumps: Tiny balls of solder that are placed on the surface of the chip and then soldered to the substrate to create a connection.
2. Through-Silicon Vias (TSV): TSVs are vertical electrical connections that run through the silicon die, connecting the top and bottom surfaces.

Others:

1. Flip-Chip BGA (Ball Grid Array): The chip is flipped over and the bumps are placed on the bottom surface. The bumps are then soldered to the substrate to create a connection. This design offers high density and a low profile.
2. Micro-BGA (Ball Grid Array): Micro-BGA is similar to Flip-Chip BGA, but the bumps are smaller and closer together. This design offers even higher density and a lower profile than Flip-Chip BGA.
3. Wafer-Level Chip Scale Package (WLCSP): A packaging technique in which the chip is integrated into the package at the wafer level.