Circuits Lab 6

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Experiment 1

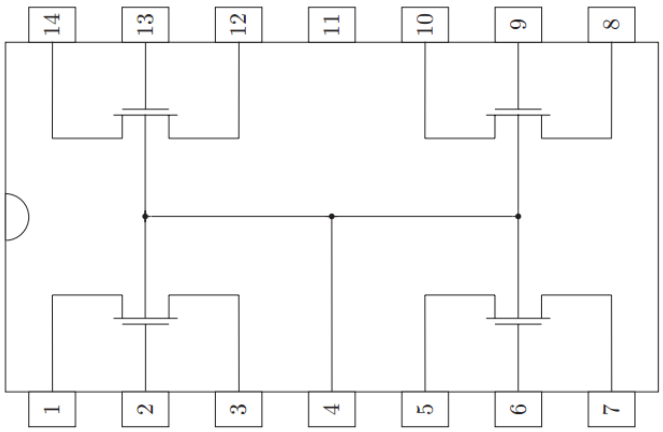

Figure 1: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

In this experiment, we wanted to evaluate how well-matched four nMOS transistors on the same die are. We used the ALD1106 Quad nMOS array, as seen in figure 1, as all four transistors on this chip are manufactured on the same substrate, which optimizes their similarity.

We first set the drain voltages of all four transistors to $V_{dd}$and the source voltages to 0, and used the SMU to measure the gate characteristic of each transistor separately.

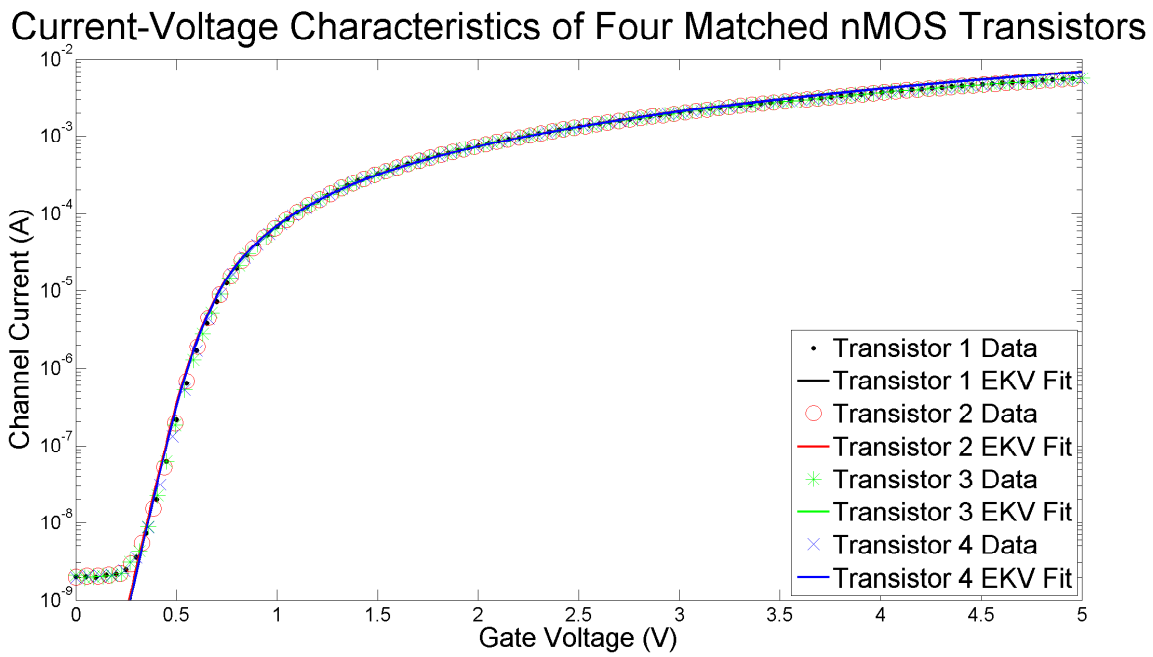

Figure 2: Channel current as a function of gate voltage for four matched nMOS transistors. Not only do the gate characteristics of the four transistors match incredibly closely, but the theoretical fits also match the data very closely, exemplifying how transistors manufabctured on the same substrate can be very similar.

We then used `ekvfit.m` to extract balues for I_s, κ, and V_{T0} for each transistor. Table has the values for these properties for each nMOS transistor:

Transistor	I_s (Amps)	κ	V_{T0} (Volts)
1	1.96×10^{-6}	0.5540	0.6912
2	2.02×10^{-6}	0.5521	0.6794
3	1.97×10^{-6}	0.5545	0.6868
4	1.96×10^{-6}	0.5539	0.6892

These properties vary little between each transistor, as we expect them to due to the manufacturing process used for the quad chip. The only obvious outlier is the I_s value for transistor 2, which deviates the most from the average I_s value, 1.9775 A. Otherwise we can see that these transistors are very well matched, which should allow for the most accurate current divider ratios in the later part of this lab.

We then used the properties of each transistor along with the EKV model to compare the gate characteristics of all four transistors with theoretical fits, which is shown in figure 2. Not only do the gate characteristics of the four transistors match incredibly closely, but the theoretical fits also match the data very closely, exemplifying how transistors manufactured on the same substrate can be very similar.

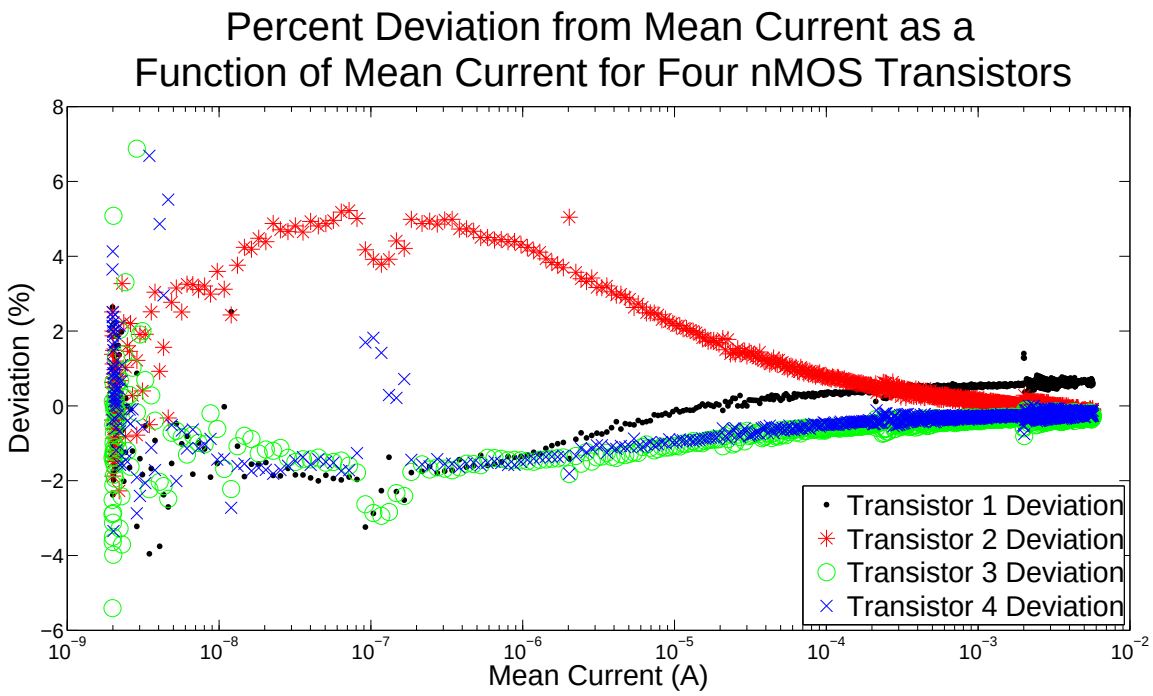

Figure 3: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

We also looked at all four channel currents as a function of the mean channel current, as seen in figure 3. At very low current values, leakage current and noise caused by the SMU cause the ratio to vary wildly. For currents about a nA, however, we saw that the channel currents for transistors 1, 3 and 4 all deviate at about the same percentage relative to the mean current, but the channel current of transistor 2 deviates far more. In fact, we think that the deviation we see in for transistors 1, 3 and 4 is likely due to transistor 2 having a higher strength ratio than the others, causing the higher extracted value for I_s, which means a higher channel current, and therefore adjusted the mean channel current causing the other channel currents to deviate below the mean.

Experiment 2

In this experiment, we explore how series and parallel combinations of nMOS transistors behave, and what affect these combinations have on the channel current, I_{sat}, as a function of gate voltage, V_G. In order to accomplish this comparison, we collected data for the channel current in both ohmic and saturation regions of operation for a single nMOS transistor, two transistors in parallel, and two transistors in series, using $V_{gb} = 10mV$ and $V_{ds} = V_{dd}$ and respectively.

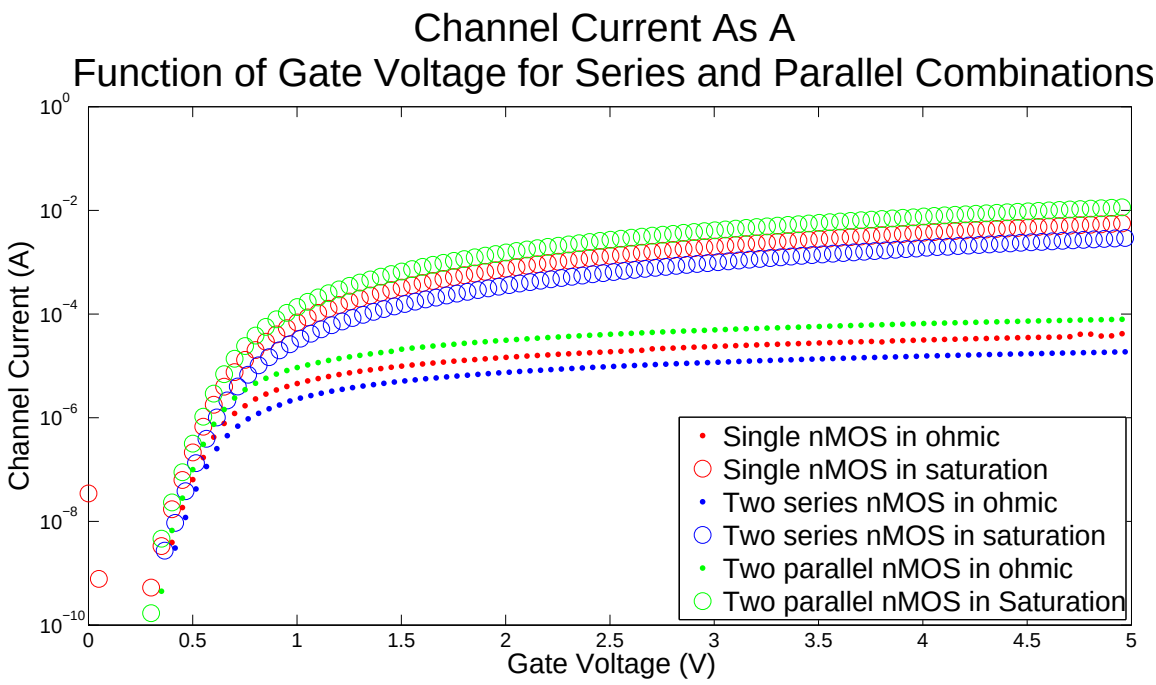

Figure 4: Note that after SMU is able to accurately measure current, after the channel current increases past roughly 10^{-8}, the three different arrangements are separated by a constant distance in logspace, and thus appear to differ by a constant factor.

At first glance, it seems that the channel current through the series combination is half of that through a single nMOS with the same gate, source, drain and bulk voltages.