Circuits Lab 6

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Experiment 1

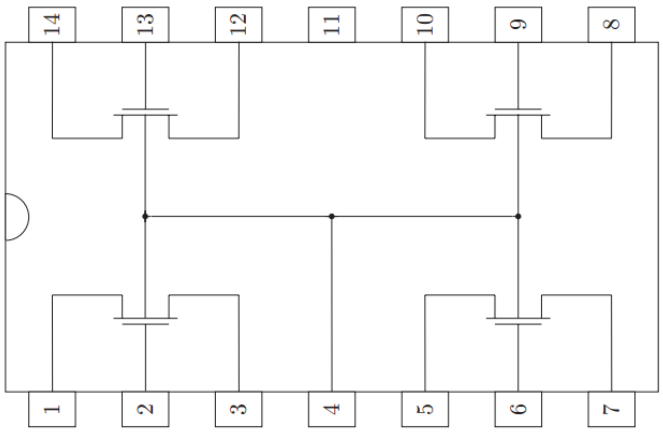

Figure 1: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

In this experiment, we wanted to evaluate how well-matched four nMOS transistors on the same die are. We used the ALD1106 Quad nMOS array, as seen in figure 1, as all four transistors on this chip are manufactured on the same substrate, which optimizes their similarity.

We first set the drain voltages of all four transistors to $V_{dd}$and the source voltages to 0, and used the SMU to measure the gate characteristic of each transistor separately.

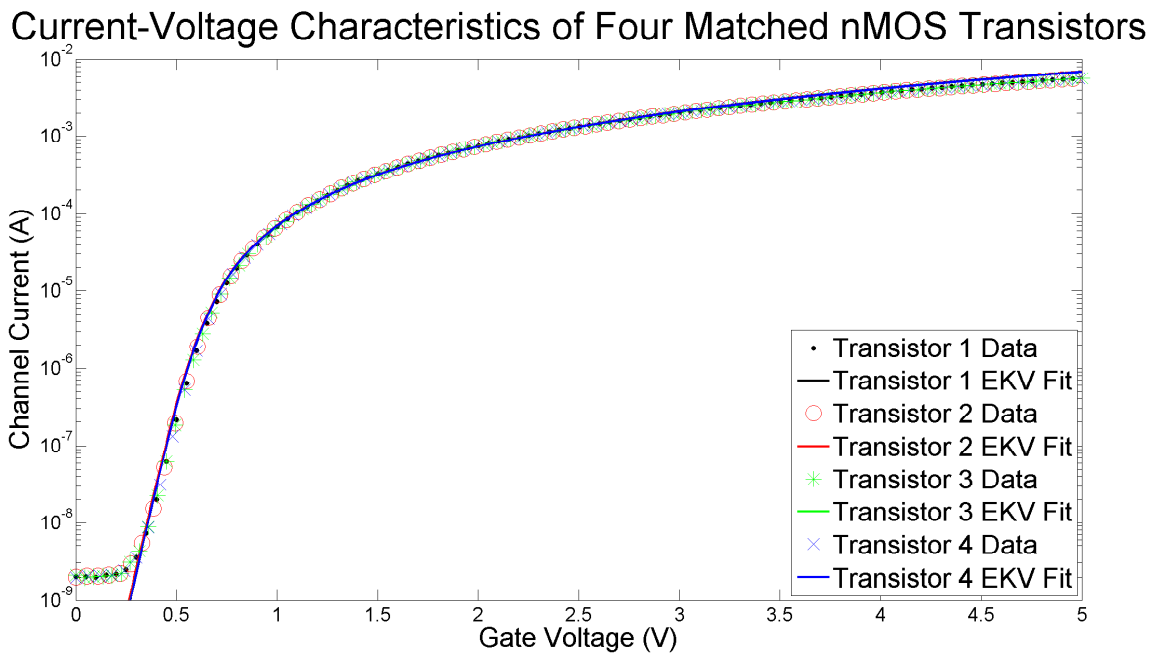

Figure 2: Channel current as a function of gate voltage for four matched nMOS transistors. The theoretical fits generated using the EKV model match the data closely near the middle of the graph, but deviate at small values of gate voltage due to leakage current. The small deviation at large values of gate voltage could be due to `ekvfit` extracted somewhat incorrect values for I_s, which causes the different slopes at large values of gate voltage.

We then used `ekvfit.m` to extract balues for I_s, κ, and V_{T0} for each transistor. Table has the values for these properties for each nMOS transistor:

Transistor	I_s (Amps)	κ	V_{T0} (Volts)
1	1.96×10^{-6}	0.5540	0.6912
2	2.02×10^{-6}	0.5521	0.6794
3	1.97×10^{-6}	0.5545	0.6868
4	1.96×10^{-6}	0.5539	0.6892

These properties vary little between each transistor, as we expect them to due to the manufacturing process used for the quad chip. The only obvious outlier is the I_s value for transistor 2, which deviates the most from the average I_s value, 1.9775 A. Otherwise we can see that these transistors are very well matched, which should allow for the most accurate current divider ratios in the later part of this lab.

We then used the properties of each transistor along with the EKV model to compare the gate characteristics of all four transistors with theoretical fits, which is shown in figure 2. The theoretical fits generated using the EKV model match the data closely near the middle of the graph, but deviate at small values of gate voltage due to leakage current. The small deviation at large values of gate voltage could be due to `ekvfit` extracted somewhat incorrect values for I_s, which causes the different slopes at large values of gate voltage.

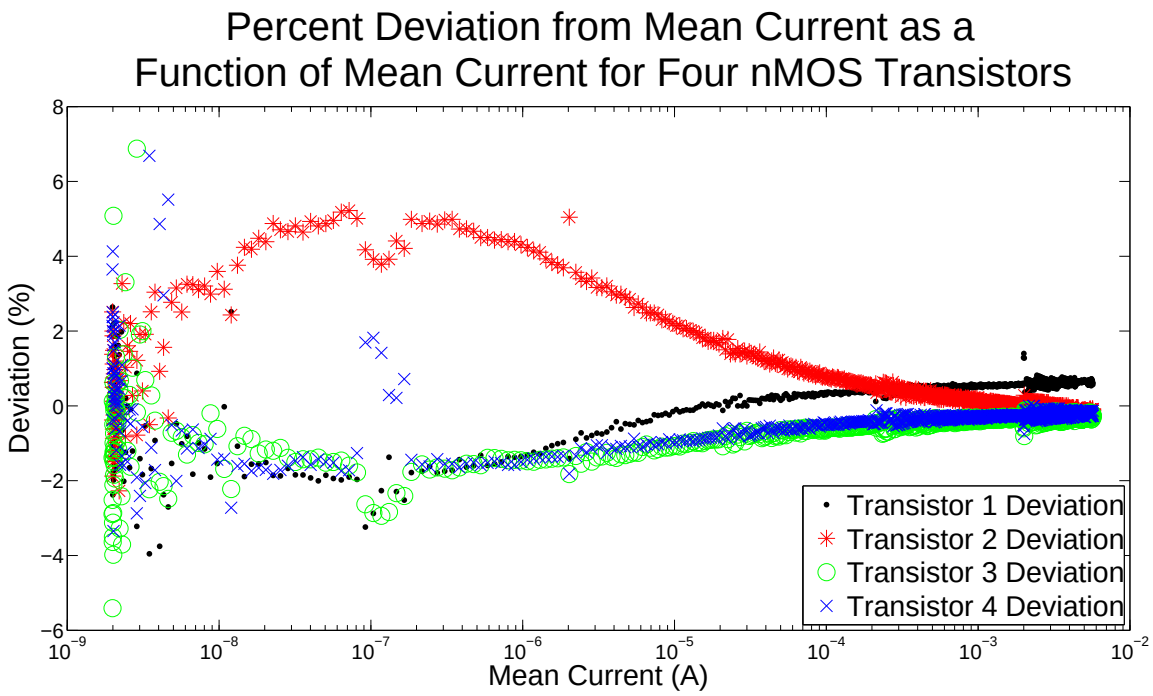

Figure 3: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

We also looked at all four channel currents as a function of the mean channel current, as seen in figure 3. At very low current values, leakage current and noise caused by the SMU cause the ratio to vary wildly. For currents about a nA, however, we saw that the channel currents for transistors 1, 3 and 4 all deviate at about the same percentage relative to the mean current, but the channel current of transistor 2 deviates far more. In fact, we think that the deviation we see in for transistors 1, 3 and 4 is likely due to transistor 2 having a higher strength ratio than the others, causing the higher extracted value for I_s, which means a higher channel current, and therefore adjusted the mean channel current causing the other channel currents to deviate below the mean.

Experiment 2

In this experiment, we explore how series and parallel combinations of nMOS transistors behave, and what affect these combinations have on the channel current, I_{sat}, as a function of gate voltage, V_G. In order to accomplish this comparison, we collected data for the channel current in both ohmic and saturation regions of operation for a single nMOS transistor, two transistors in parallel, and two transistors in series, with the same gate, source, drain and bulk voltages. We tested the configurations in both the ohmic and saturation regions of operation, using $V_{gb} = 10mV$ and $V_{ds} = V_{dd}$ and respectively.

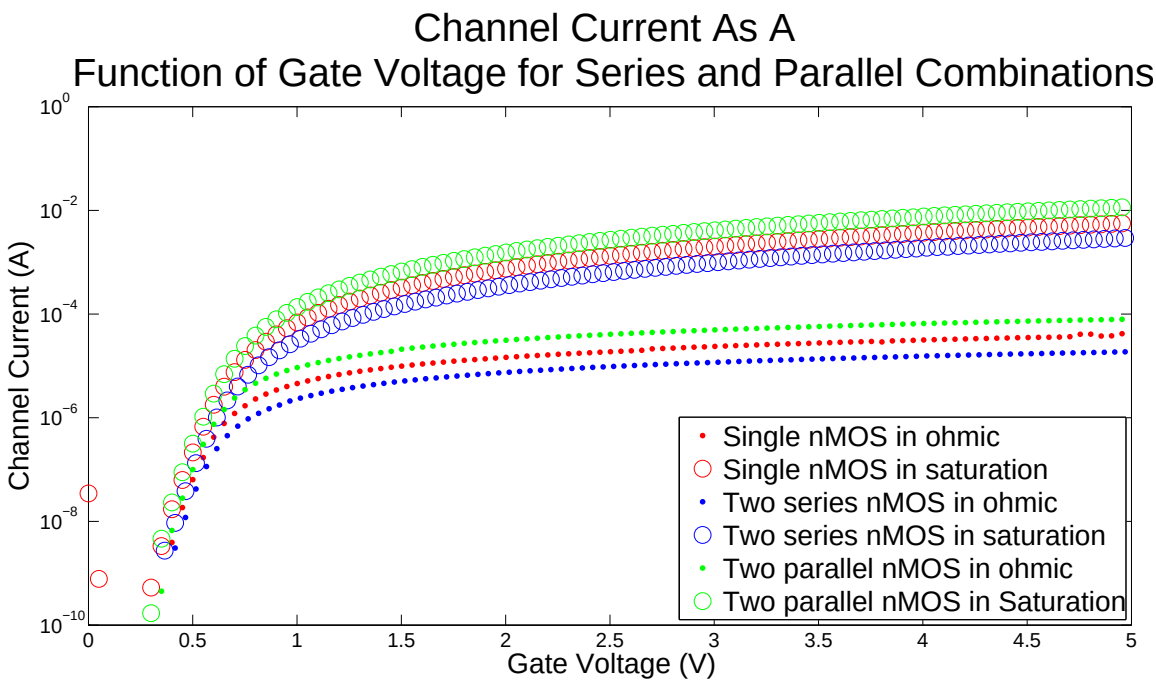

Figure 4: Note that after SMU is able to accurately measure current, after the channel current increases past roughly 10^{-8}, the three different arrangements are separated by a constant distance in logspace, and thus appear to differ by a constant factor.

By analyzing Figure 4, we can see that the series, parallel and single curves appear to be offset by a linear distance in logspace, thus indicating that there is a linear factor between the relationships.

From the pre-lab, we know that two transistors in series with unit strength ratios act as a single nMOS transistor with strength ratio $\frac{1}{2}$, and that two nMOS transistors in parallel act as a single nMOS transistor with strength ratio 2. The parallel case is relatively simple to prove, where $f(\dot{)}$ is a function that assumes an exponential form in weak inversion and a quadratic one in strong inversion. Allowing I_1 and I_2 to be the current through each parallel branch:

$$I = I_1 + I_2$$

$$I_1 = I_{s1}(f(V_{GB}, V_{SB}) - f(V_{GB}, V_{DB}))$$
$$I_2 = I_{s2}(f(V_{GB}, V_{SB}) - f(V_{GB}, V_{DB}))$$

Assuming the two transistors are matched, $I_{s1} = I_{s2}$, and thus:

$$I = (I_{s1} + I_{s2})(f(V_{GB}, V_{SB}) - (V_{GB}, V_{DB}))$$

$$I = 2I_1$$

In order to find the true relationship, we explored the ratio of both the series and parallel combination of nMOS transistors with the same V_G, V_D, $V_S$and V_B, plotting these ratios as a function of the gate voltage, V_G, below in Figure 5. In the strong inversion region, the ratio between both the series and parallel combinations to that of a single transistor is consistently, 0.5 and 2, respectively. That is to say, from our experimental data, a pair of series transistors sinks half the current as a single transistor, and a pair of transistors in parallel sinks twice the current of a single transistor, when matched.

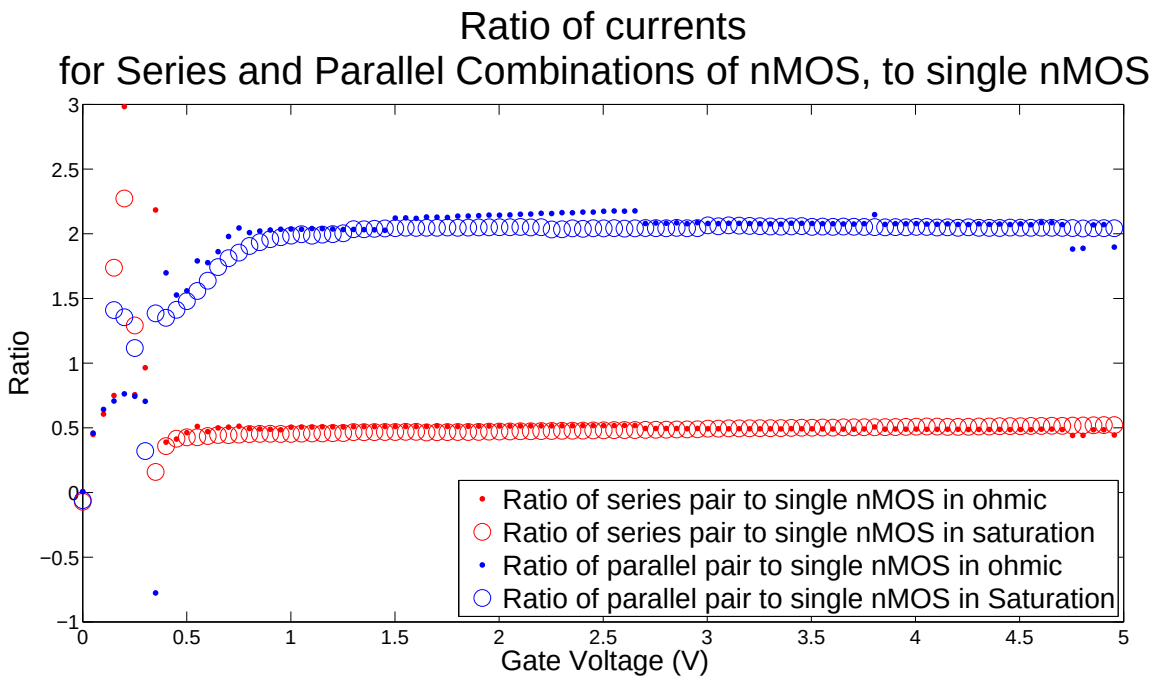

Figure 5: After the two curves stabilize, past roughly $0.75V$, the ratio between both series and parallel combinations to a single nMOS is consistent, and produces the expected value; a pair of nMOS transistors in series has half the current of one, and a pair of nMOS transistors in parallel has twice the current as a single transistors.

Meanwhile, in the weak inversion region of operation, the series combination of transistors much better maintains a consistent ratio, quickly approaching a 1:2 ratio as the SMU is able to accurately measure current. Before this value, we believe a combination of SMU error at low current and measurement of leakage current cause the deviation.

On the other hand, the parallel combination does not approach the ratio of 2:1 until $1V$. We believe it takes this parallel combination much longer because the leakage current measured is effectively double. Further, since different individual transistors were used in this test, it may be due to the relatively large deviation of Transistor 2, shown in Figure 3. We used Transistor 2 in the parallel combination, and since it had a higher strength factor than the other three resistors, more current would flow through it, thus making the parallel pair have a ratio closer to 1:1, rather than the 2:1 it eventually achieves, as the voltage increases.

Experiment 3

In this experiment, we constructed a two-way current divider, with the divider ratio is a ratio of two small integers by connecting them in series and in parallel. We used two nMOS transistors in series for one branch of the current dividers, and two nMOS transistors in parallel for the other current. We took turns setting the input of the current divider at the sources of both branches and then the drain of both branches, as shown in figures 6 and 8.

From the pre-lab, we know that two matched transistors in series act as a single nMOS transistor with strength ratio $\frac{1}{2}$, and that two nMOS transistors in parallel act as a single nMOS transistor with strength ratio 2. We attached the SMU probe to the drains of the two parallel nMOS transistors while tying the drain of the series nMOS branch to V_{dd}.

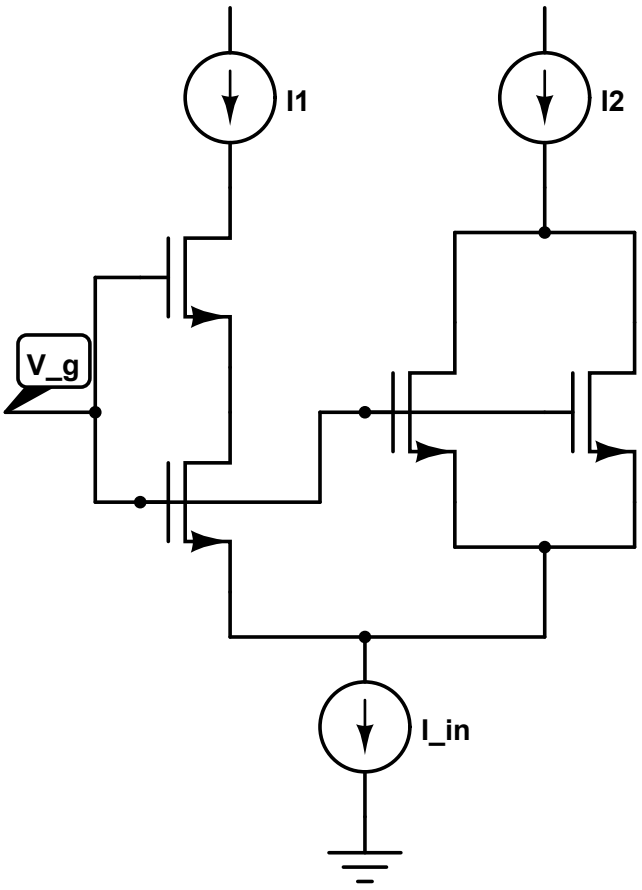

Figure 6: A diagram of the circuit used in Experiment 3.

We first set I_{in}using the sources of both branches of the current divider, and measured I_{out}as a function of I_{in}as we varied I_{in}on a log scale. We attached the SMU leads to the parallel transistor branch, so we expected a current divider ratio of 0.8. As figure 7 shows, the current transistor characteristic of the circuit is very linear on a log scale, and we confirmed using `polyfit` that the slope of the line was 0.7870, which is very close to the predicted ratio of 0.8.

We can see that the theoretical fit, which was created by multiplying $I_{in}0.8$, matches the data very closely through many orders of magnitude of I_{in}. This indicates that this current divider can be expected to operate as theoretically predicted for many values of I_{in}.

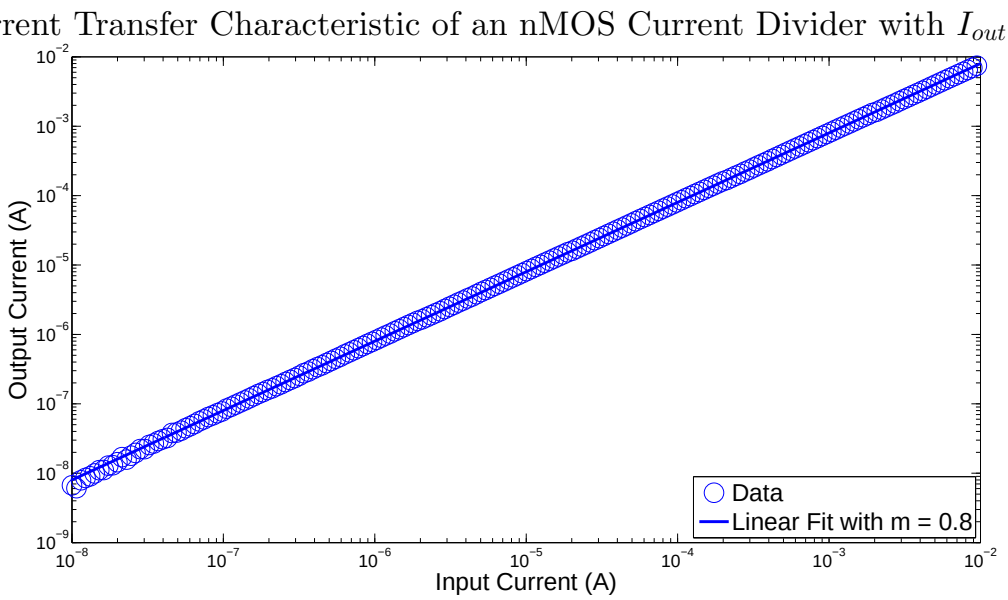

Figure 7: A diagram of the circuit used in Experiment 3.

Next, we constructed the two-way current divider shown in Figure 8, such that the divider ratio was a small integer multiple. We measured the output current as we swept the input current, fitting a straight line to the data collected.

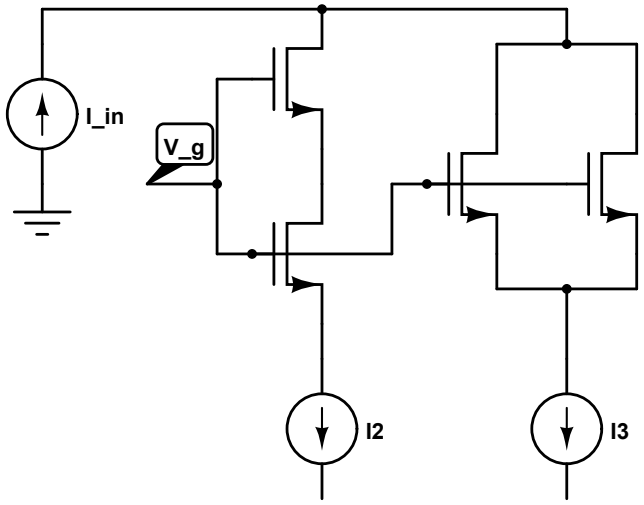

Figure 8: A diagram of the circuit used in Experiment 3 Section 2

As can be seen in Figure 9, the data fit a straight line well, with an extracted slope of 0.80298. Drawing upon our previous knowledge from Experiment 2, where we found that the series combination of two nMOS transistors passed half the current as a single nMOS , and the parallel combination passed twice the current of a single nMOS , we can infer that the series combination passed one quarter the current of a parallel combination. Thus, for a given set of voltages, V_G, V_D, V_B, $V_D$and V_S, we expect the theoretical ratio of current passed to be 1:4 between the series and parallel combinations, respectively. A 1:4 ratio is the same as a fifth of the current being passed through the series

combination, and four-fifths of the current through the parallel combination. As seen in Figure 9, the extract slope was almost exactly 4/5 or 0.8.

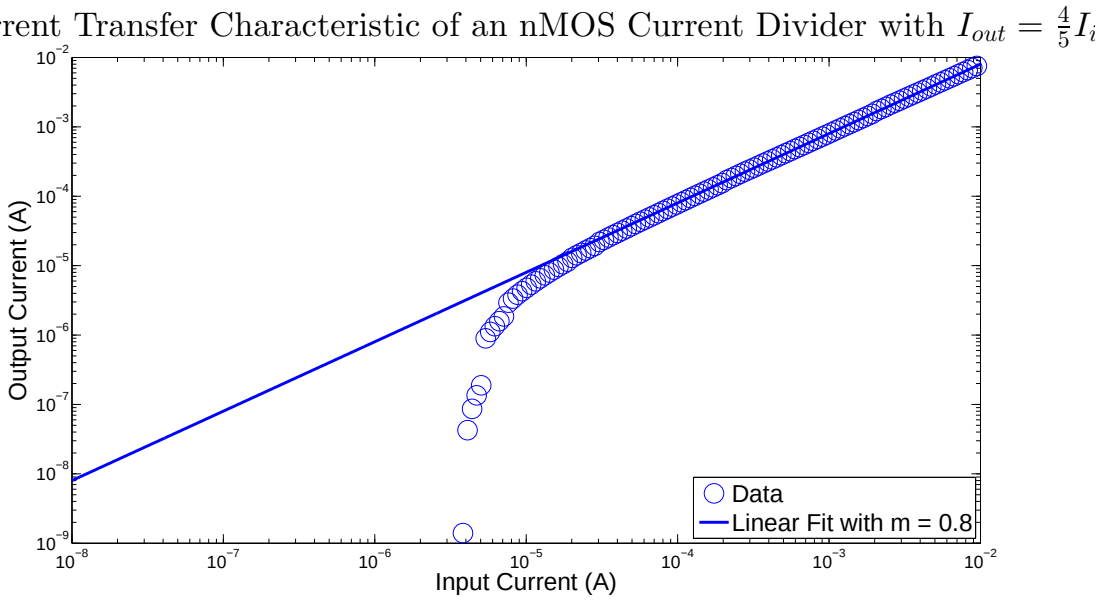

Figure 9: A plot of the current through the parallel combinaton of nMOS , as a function of input current.

To explain the difference between the two current divider circuits, we need to understand how V_{DS} changes for both circuits as we increase I_{in}. In the case where we pull current from the sources of both branches, small currents will induce a small source voltage, which will be more than V_{DSSat} away from V_{dd}, ensuring that both branches will remain in saturation. In the second circuit, where we push I_{in}through the drains of both branches, we see that the circuit only begins operating as we expect it to once we pass a certain current threshold. This can be explained by examining the drain voltage for small values of I_{in}. When $I_{in}$is small, we expect the drain voltage to be small, as only a small amount of current passes through the branch of each transistor. The branch of the current divider with the series transistors requires that the input voltage be at least $2V_{DSSat}$, as both transistors need to be in saturation for proper circuit operation. This minimum voltage threshold is the analog to the minimum current threshold we saw in figure 9, and explains why the circuit in figure 6 is a better current divider circuit compared to the circuit in figure 8.