

Circuits Lab 6

Cory Dolphin and Noam Rubin

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Experiment 1

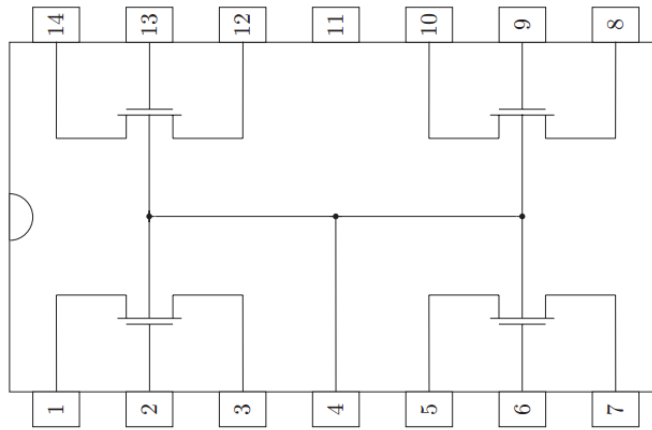


Figure 1: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

In this experiment, we wanted to evaluate how well-matched four nMOS transistors on the same die are. We used the ALD1106 Quad nMOS array, as seen in figure 1, as all four transistors on this chip are manufactured on the same substrate, which optimizes their similarity.

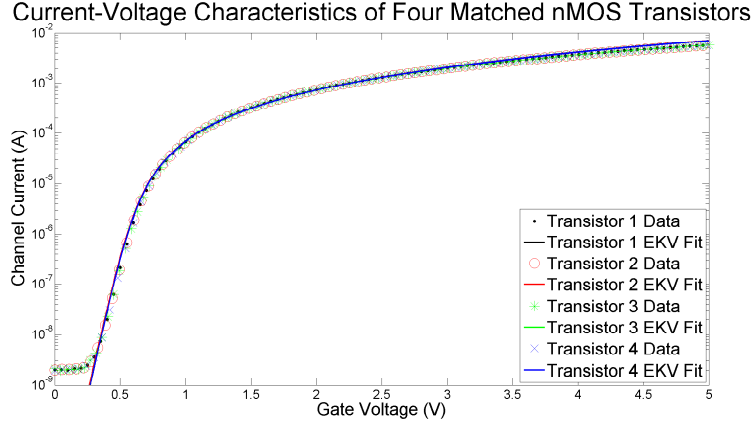


Figure 2: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

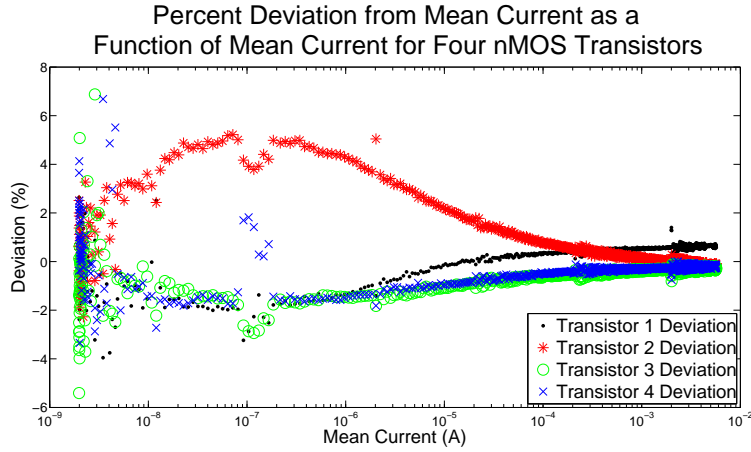


Figure 3: Picture of the ALD1106 QUAD nMOS transistor array which was used in Experiment 1 to analyze the similarities between nMOS transistors. Using a Quad array is ideal as all transistors are manufactured on the same substrate, optimizing their similarity.

Experiment 2

In this experiment, we explore how series and parallel combinations of nMOS transistors behave, and what affect these combinations have on the channel current, I_{sat} , as a function of gate voltage, V_G . In order to accomplish this comparison, we collected data for the channel current in both ohmic and saturation regions of operation for a single nMOS transistor, two transistors in parallel, and two transistors in series, using $V_{gb} = 10mV$ and $V_{ds} = V_{dd}$ and respectively.

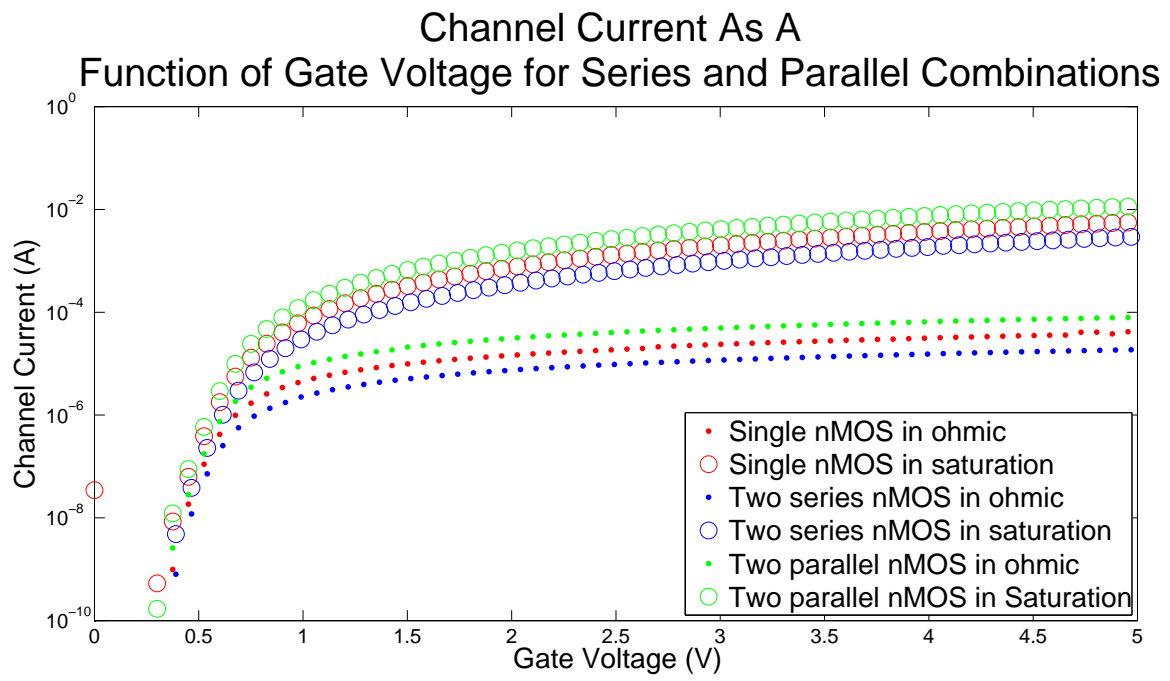


Figure 4: