Circuits Lab 6

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Experiment 1

Figure 1: Picture of the ALD1106 QUAD nMOS transistor array

In this experiment, we wanted to evaluate how well-matched four nMOS transistors on the same die are. We used the ALD1106 Quad nMOS array, as seen in figure **??**

Experiment 2

In this experiment, we explore how series and parallel combinations of nMOS transistors behave, and what affect these combinations have on the channel current, I_{sat}, as a function of gate voltage, V_G. In order to accomplish this comparison, we collected data for the channel current in both ohmic and saturation regions of operation for a single nMOS transistor, two transistors in parallel, and two transistors in series, using $V_{gb} = 10mV$ and $V_{ds} = V_{dd}$ and respectively.

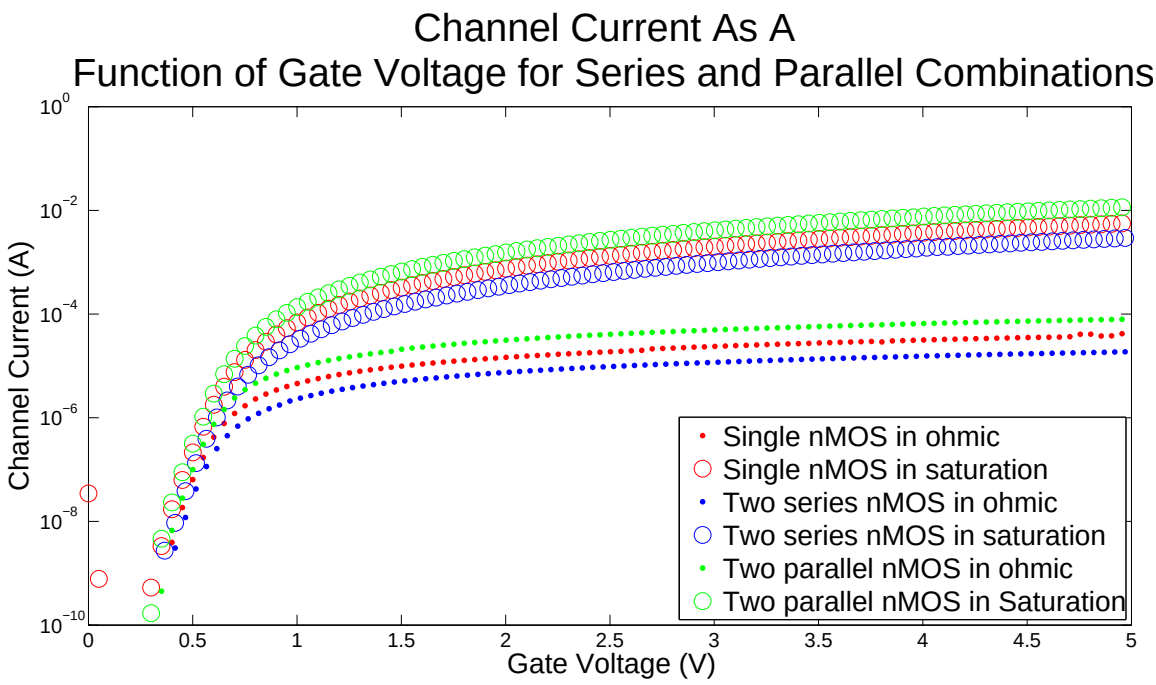

Figure 2: Note that after SMU is able to accurately measure current, after the channel current increases past roughly 10^{-8}, the three different arrangements are separated by a constant distance in logspace, and thus appear to differ by a constant factor.

At first glance, it seems that the channel current through the series combination is half of that through a single nMOS with the same gate, source, drain and bulk voltages.