Circuits Lab 8

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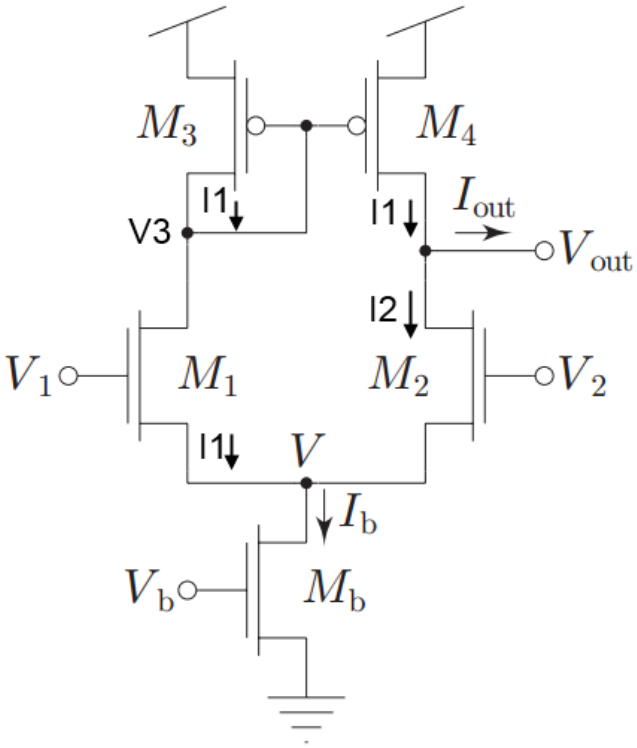

Figure 1: A schematic of the differential amplifier used in this lab, with some extra voltages and currents annotated for the purpose of analysis.

Experiment 1

We began by building a simple differential amplifier from an nMOS differential pair and a pMOS current mirror. We set the bias transistor just at threshold by applying a bias voltage of $V_B = 0.6V$ We connected both inputs together such that the differential mode voltage was zero, and swept the common mode voltage from $+5V$ to $0V$, measuring the output voltage, V_{out} . A plot of V_{out} as a function of V_{cm} can be seen below in Figure 2. For values of V_{cm} greater than the bias voltage, $0.6V$, V_{out} appears to change very little with large changes in V_{cm} . We determined the common-mode gain of the amplifier by applying a linear fit to the data. The linear fit found had a slope -0.202, thus from our data, we experimentally found $A_{cm} = -0.202$. Notably, the output voltage appeared to

stabilize at approximately $4.3V$. Though we expected a negative common-mode gain on the order of a few percent, our gain is larger than expected, on the order of a tens of percents, instead of percents. This is likely caused by transistor mismatch.

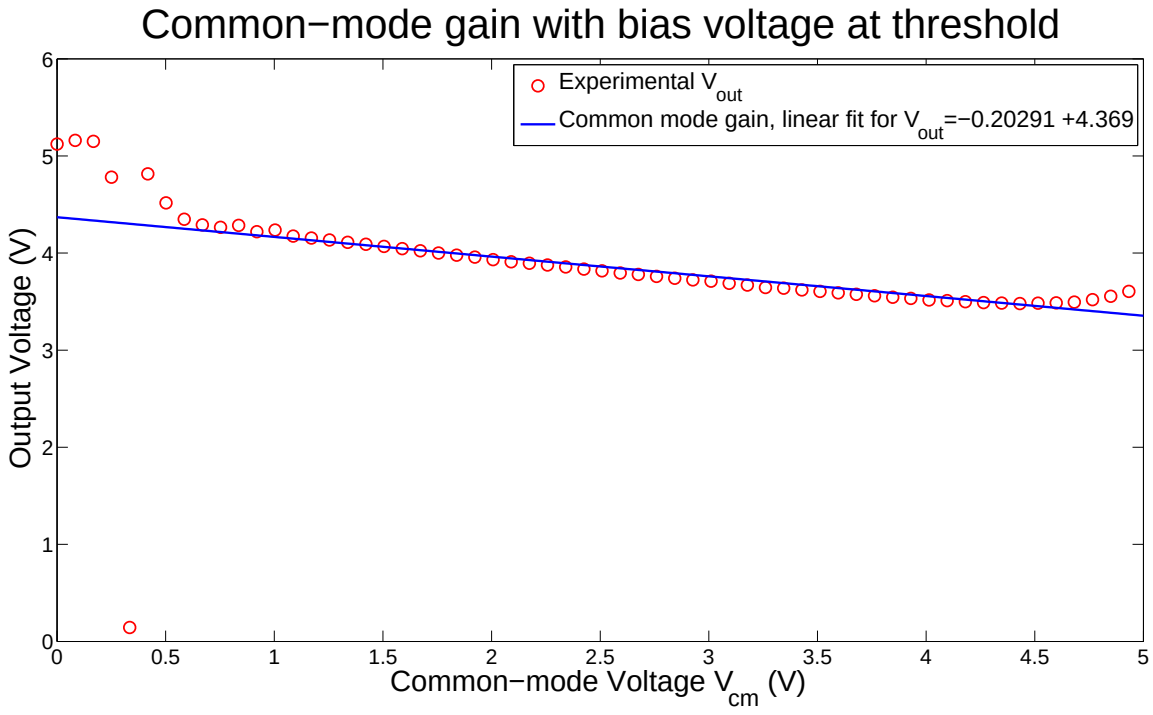

Figure 2: For values of V_{cm} greater than the bias voltage, $0.6V$, V_{out} appears to change very little with large changes in V_{cm} . We determined the common-mode gain of the amplifier by applying a linear fit to the data. The linear fit found had a slope -0.202.

We then connected V_2 to a constant voltage source and sweep V_1 from one $+5V$ to $0V$, measuring V_{out} for V_2 set to three different voltages, $2V$, $3V$ and $4V$.

The voltage transfer characteristic for these experiments, shown in Figure 3 show three major regions of operation: one in which V_{out} increases linearly with a small slope relative to V_1 , when V_1 is less than V_2 ; another in which V_{out} rapidly increases to the positive rail over a small voltage range, when V_1 is slightly greater than V_2 ; and a third, in which V_{out} is pinned at the $+5V$ rail.

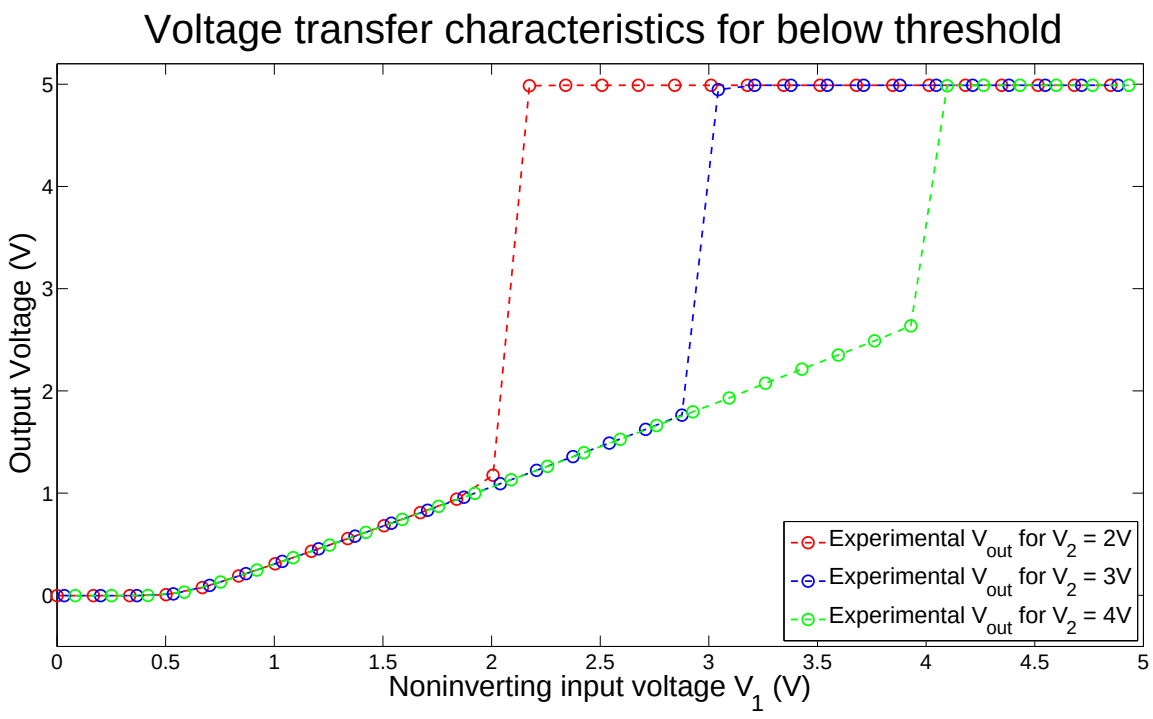

Figure 3: Note that the three series are similar in shape, with the point of inflection equaling the second input voltage for each series.

Repeating the experiment with the bias transistor in strong inversion, with $V_b = 1.5V$, we found a similar pattern to the previous experiment, though the time-scale seemed to be extended.

In the case of the common-mode gain, we found that V_{out} ultimately achieved a voltage of roughly $3.8V$, roughly $0.5V$ less than in the weak inversion case. Further, V_{out} changed even less relative to V_{cm} when V_{cm} was greater than V_b . With the bias transistor strongly inverted, we found a common-mode gain of -0.039, a magnitude more similar to the value expected. Meanwhile, for common-mode voltages less than V_b , V_{out} changed far more rapidly.

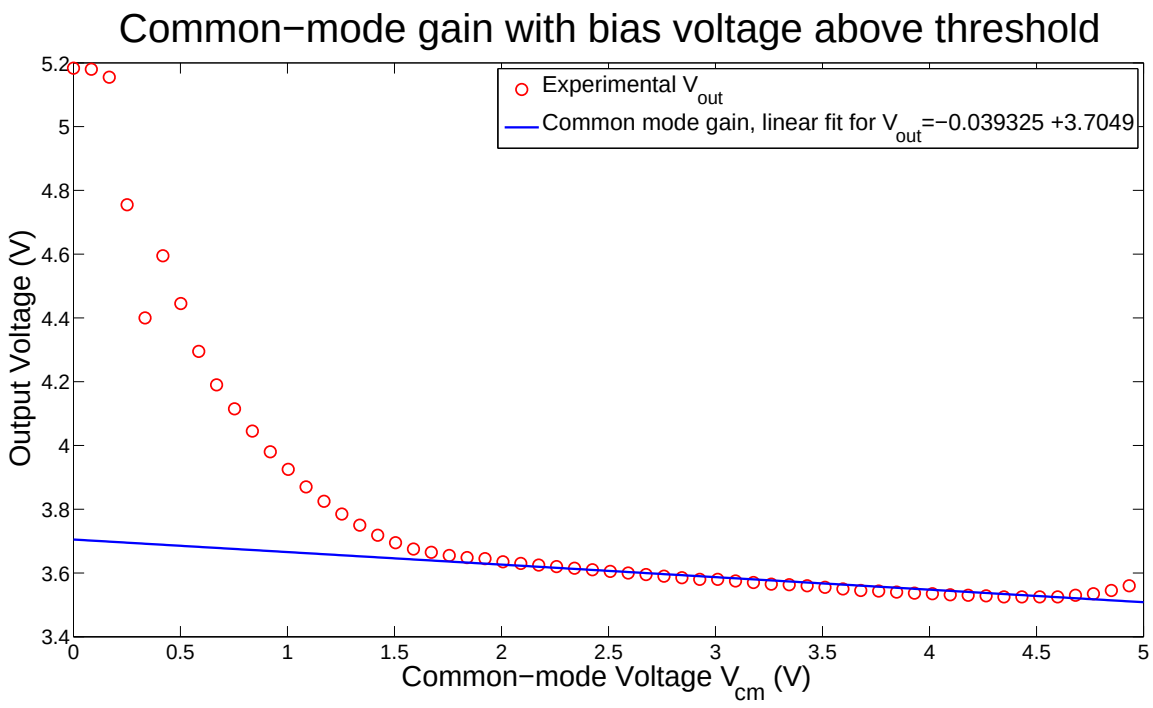

Figure 4: In this case, V_{out} changed even less relative to V_{cm} when V_{cm} was greater than V_b . With the bias transistor strongly inverted, we found a common-mode gain of -0.039, a magnitude more similar to the value expected

When sweeping V_{dm} through a range of values, we found that a similar relationship held, three major regions were found on the voltage transfer characteristic shown in Figure 5:one in which V_{out} increases linearly with a small slope relative to V_1 , when V_1 is less than V_2 ; another in which V_{out} rapidly increases to the positive rail over a small voltage range, when V_1 is slightly greater than V_2 ; and a third, in which V_{out} is pinned at the $+5V$ rail. One major difference between the behavior with the bias transistor in strong inversion was the rate at which V_{out} changed when V_1 increased just past V_2 ; the output voltage approached the $+5V$ rail more slowly than in the weak inversion case, and appeared to somewhat smooth the discontinuities found in the previous case, linking the three regions with a more sigmoidal shape.

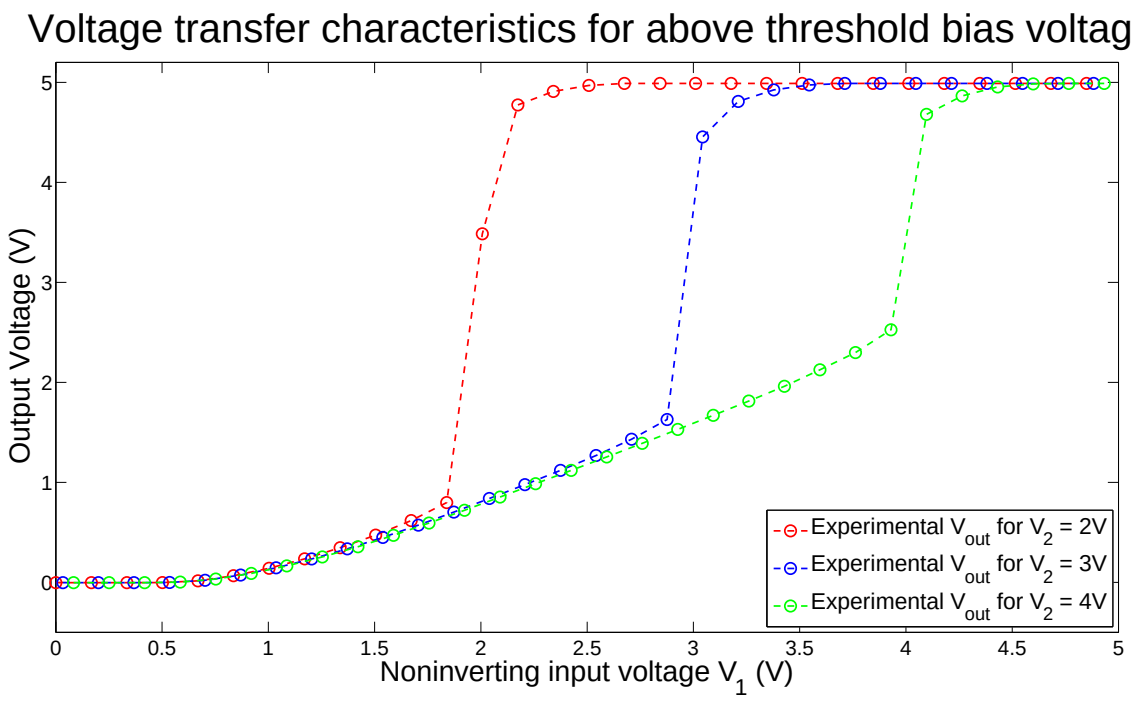

Figure 5: Note that the three series are similar in shape, with the point of inflection equaling the second input voltage for each series.

The behavior of the circuit does not seem to differ substantially when biased in strong inversion, when compared to that which it exhibits in weak inversion. The major difference is the somewhat diluted affect of V_{dm}, that is to say, when in strong inversion, larger swings in V_{dm} were necessary to produce similar changes in V_{out} . This can be seen in the comparison of Figure 4 and Figure 3, where the abrupt discontinuities seen in weak inversion are smoothed out in strong inversion, as can be seen by the rounding of the sharp angles.

Experiment 2

We then studied the incremental properties of the differential amplifier, most importantly the differential-mode voltage gain, A_{dm} . We define

$$A_{dm} = \frac{\partial V_{out}}{\partial V_{dm}} = \frac{\partial V_{out}}{\partial I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{dm}} \tag{1}$$

We can estimate A_{dm} for this circuit in two ways: the first is to measure V_{out} as a function of V_{dm} , and extracting the slope for small values of V_{dm} . We can also collect curves for V_{out} as a function of I_{out} and I_{out} as a function of V_{dm} , and then multiply the linear region of those plots together in order to extract a value for A_{dm} .

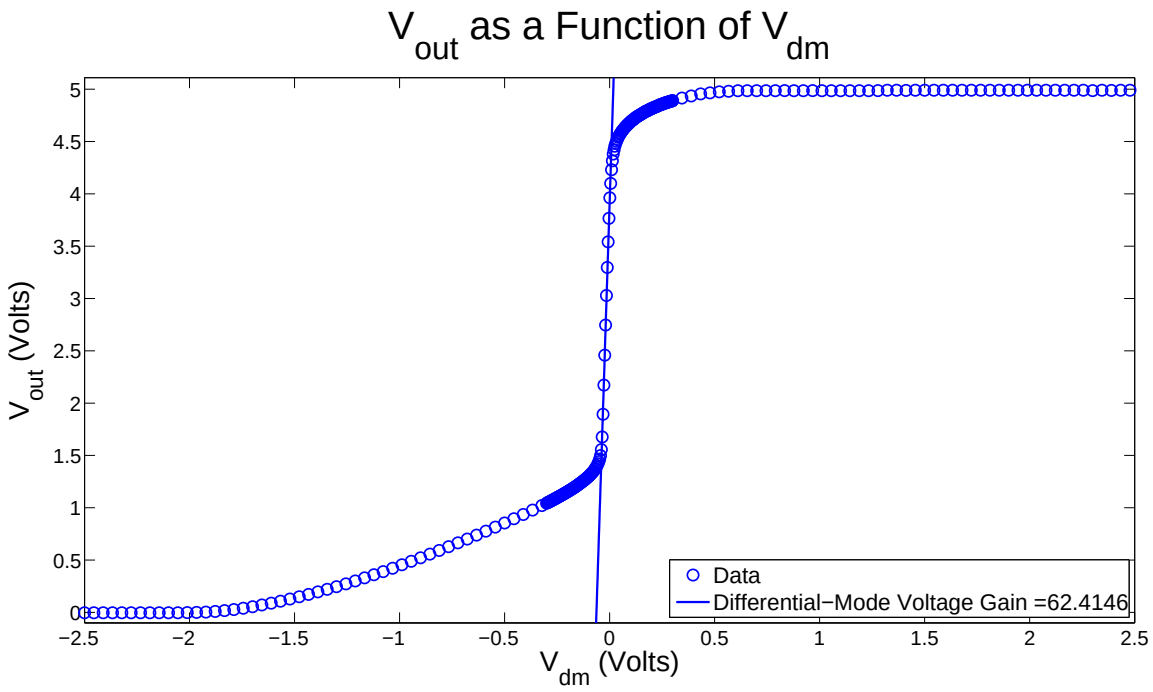

Figure 6: V_{out} as a function of V_{dm} . The interesting region in this graph is the near-vertical region around $|V_{out}| < 0.05V$, as the slope of this region can be interpreted as A_{dm} , the differential mode voltage gain. From this plot we extracted an A_{dm} value of 62.4146.

We first measured V_{out} as we help V_{cm} at 1.2 V and swept V_{dm} from -0.5 V to 0.5 V. We plotted V_{out} as a functions of V_{dm} , as seen in figure 6. In order to get a large number of points in the high-gain region, we collected data at different densities along V_{dm} .

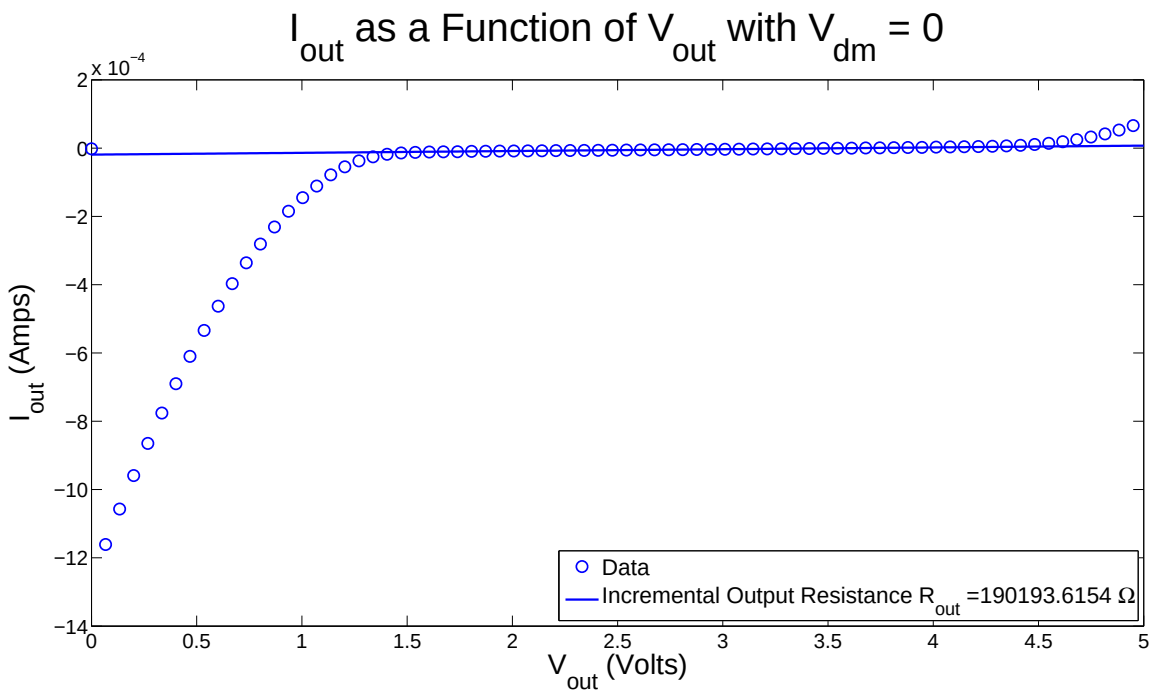

Figure 7: I_{out} as a function of V_{out} . The inverse of the slope of the shallow region of this graph is R_o , the incremental resistance of the circuit. We extracted a value of 190193.615 Ω for R_o , and used this to calculate A_{dm} in a separate manner than simply taking the slope of the vertical region in figure 6

We then fit a line to the steep linear region around $V_{dm} = \pm 0.005V$, and used the slope to extract a value for A_{dm} . We fit to about 20 points along the line and found that $A_{dm} \approx 62.4146$. This large gain was theorized in the pre-lab (where we expected A_{dm} to be near infinite), but is not as large as expected. We expect V_{out} to change drastically with V_{dm} because the sign of V_{dm} defines the flow of current, and opposite current flows likely cause large swings in V_{out} . When $V_{dm} < 0$, $I_2 > I_1$, so V_{out} lowers to allow more current through M_4 , as M_2 pulls more current. Conversely, when $V_{dm} > 0$, $I_1 > I_2$, which causes V_{out} to rise to prevent current flow through M_4 , as M_2 cannot sink all of the current. We see the large swings in V_{out} for small values of V_{dm} as expected.

We next took the approach of calculating R_{out} and G_m , and multiplying these two properties of the circuit together in order to extract a different value for A_{dm} . Figure 8 shows I_{out} as a function of V_{out} , with an extracted slope that represents $\frac{1}{R_{out}}$. Figure 8 shows I_{out} as a function of V_{dm} , with an extracted value for G_m . From these lines we found that $R_out = 190193.6154\Omega$ and $G_m = 0.00044197\Omega^{-1}$, which results in an extracted value for the differential mode gain of 84.0599. This is higher than the value we extracted from figure 6, which could be due to compound error in the separate experiments or lines that don't exactly match the data they are fit to. Regardless, we see that A_{dm} is large, which is what we expect.

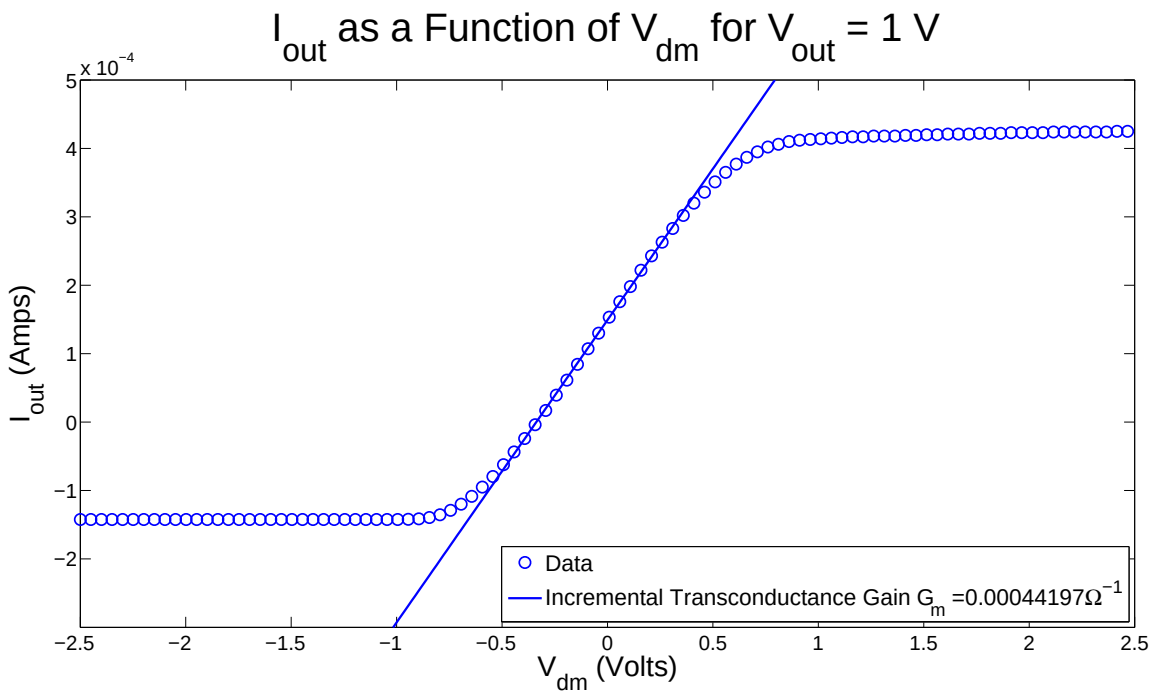

Figure 8: I_{out} as a function of V_{dm} . The slope of the linear region of this plot, around $|V_{out}| < 0.05V$, can be used to extract G_m , the incremental transconductance gain of this circuit. We extracted a value of 0.00044197 Ω^{-1} for G_m , and used this value to calculate A_{dm} .

An important attribute of a differential voltage amplifier is the Common-Mode-Rejection-Ratio, which we call the CMRR and is defined as:

$$CMRR = 20\log_{10}(\frac{A_{dm}}{|A_{cm}|}) \tag{2}$$

For the value of A_{dm} derived from figure 6, we found that the CMRR of this circuit is 49.7987, and for the A_{dm} value derived using figures 7 and 8, the CMRR of this circuit is 52.3847. These two values for the CMRR are not very different, which indicates that the two different values of A_{dm} we calculated may not significantly affect the circuit behavior.

Experiment 3

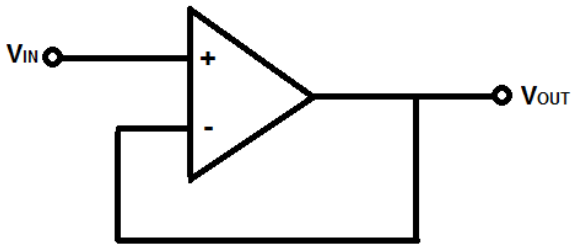

Figure 9: Simple voltage follower we built in Experiment 3.

The last experiment we conducted involved connecting the inverting input of the differential amplifier, V_2 , to the output of the differential amplifier, V_{out} . We expected the circuit to then behave like a unity-gain voltage follower, as seen in figure 9. In a unity-gain voltage follower, the output follows the non-inverting input, so we expect the ratio between V_{out} and V_{in} to be 1.

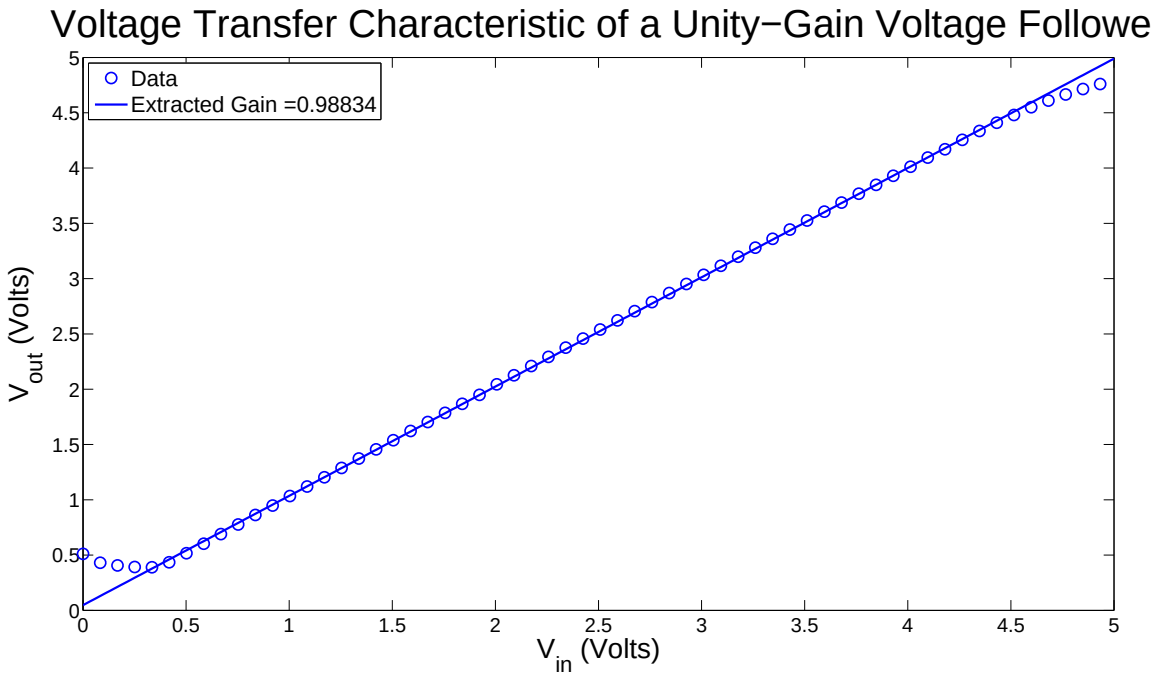

Figure 10: The voltage transfer characteristic of the unity-gain follower we made. The slope of this line is very close to 1, except at minima and maxima of V_{out} .

So we connected the output and the input of the differential amplifier and measured V_{out} as we swept V_{in} from ground to V_{dd} . The results are shown in figure 10, in addition to a line fitted to the linear region of the voltage transfer characteristic. We extract the slope of this line and found that the actual gain of the follower was 0.98834, very close to the anticipated gain of 1. The slight deviation, a little over 1%, can likely be attributed to experimental error. The behavior of the circuit for small values of V_{in} can likely be attributed to both M_1 and M_2 operating in weak inversion, which causes I_{out} to be the difference between their very small leakage currents, which therefore causes V_{out} to change little for $0 \leq V_{in} \leq \approx 0.5V$.

We can also see that the near-unity gain between V_{out} and V_{in} breaks down for values of V_{in} near V_{dd} . This could be due to the bias transistor not passing as much current as M_1 can pass, so as the gate voltage of M_1 increases, I_b increases less than expected, which causes V_{out} to increase less than linearly.

Since we expected $\frac{V_{out}}{V_{in}} \approx 1$, we next looked at the offset voltage of the bias transistor $(V_{out} - V_{in})$ in order to gain further insight into how our unity-gain buffer behaves compared to the ideal form of the circuit, which would have an offset voltage of 0.

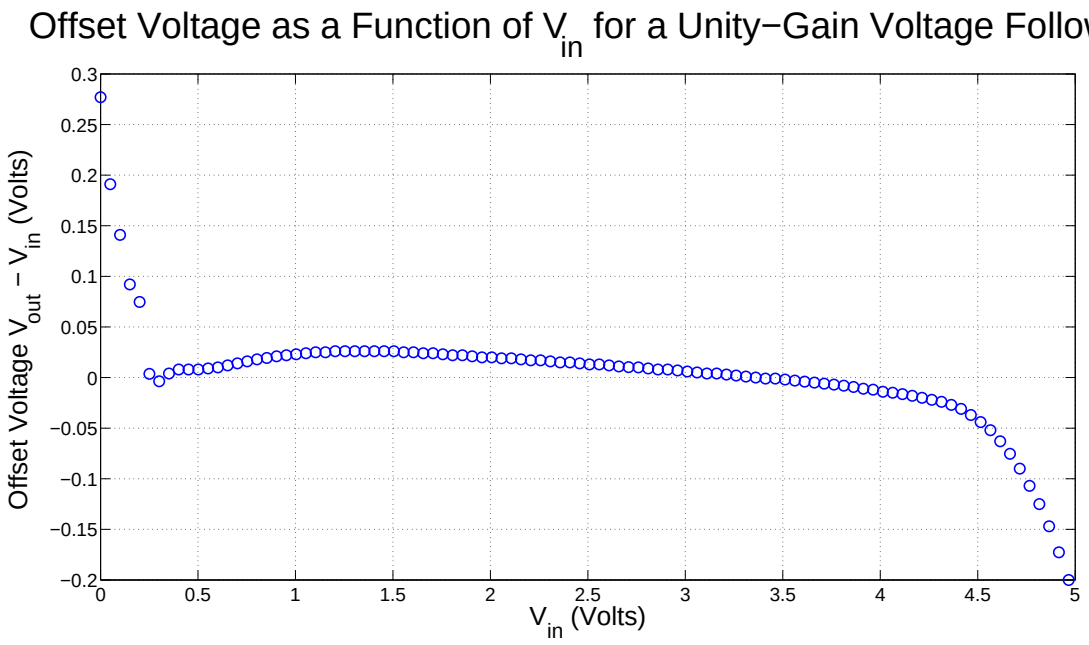

Figure 11: The offset voltage of the unity-gain buffer as a function of V_{in} , where we see that even though the offset voltage changes a lot when $V_{in} < 0.3V$, it generally stays around 0.05 V for most of regions of operation of the circuit.

Figure 7 shows the offset voltage of the buffer as a function of V_{in} , and some interesting trends appear. We again see large deviations from the theoretical ideal at values of V_{in} near ground and near V_{dd} , which could be explained by leakage current and a saturated M_b , respectively.

The trend in the middle of the data seems to take two forms: for $0.5 < V_{in} < 1.5$, the offset voltage has a small positive slope, but for $1.5 < V_{in} < 4.5$, this slope becomes negative, and the trend is far more linear. Generally, however, the offset voltage hovers around 0, and deviates by about $\pm 0.02V$ throughout the region of linear operation that we saw in figure 10.