

ENGINEERING DEPARTMENT OF ELECTRICAL, COMPUTER, AND SOFTWARE ENGINEERING

COMPSYS 304: Computer Architecture

Lecture Notes

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Introduction

These notes are compiled from the lectures of COMPSYS 304. They are intended as a personal reference to help with assignments, exam preparation, and understanding key concepts in Computer Architecture.

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Part I Morteza's Content

Chapter 1

Introduction & Course Overview

This chapter provides an introduction to the course, some background, and an overview of the course itself.

1.1 Background

In the last six decades, computer technology has made incredible progress due to innovations in both **semiconductor technology** and computer **architecture**.

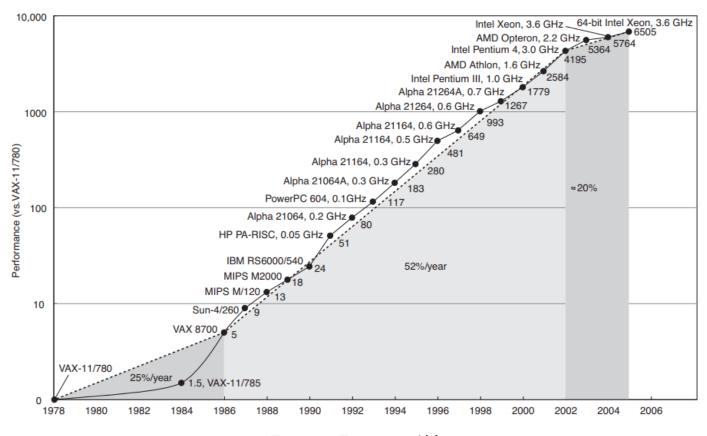


Figure 1.1: Figure 1.17 of [1]

1.1.1 What do we mean from *Performance*?

The relative performance can be measured by standard benchmarks, which depend on the specific target applications.

Performance depends on clock frequency and other factors, as discussed more in later chapters.

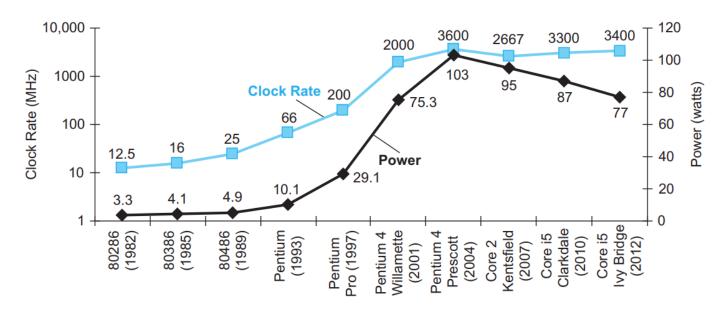


Figure 1.2: Figure 1.16 of [1]

1.1.2 Intel X86 Processor from 1978 to 2018:

• Intel 8086 - (1978): 1 core, 1 W, 5 - 10 MHz

• Core i7-8086K - (2018): 6 cores, 95 W, 4 GHz

1.2 Course Details

1.2.1 Learning outcomes

The main learning outcomes of this course are:

- To understand the basics of modern computer architectures and quantitative principles of computer design in order to develop a conceptual understanding of issues involved in designing a high performance computer system.
- To use and apply this knowledge to design computer systems or select computers for specific tasks. This course will give you an understanding of the effects of design decisions on system performance and makes you a well-informed consumer in addition to a processor designer.

Recommended Textbook:

- David A. Patterson and John L. Hennessey, Computer Organization and Design: The Hardware/Software Interface, Fifth edition, 2013 by Elsevier/Morgan Kaufmann Publishers (or 3rd or 4th editions). [1]
- Lecture notes provided on canvas (these will be summarised in these notes).

1.2.2 Course Overview (learning outcomes)

Part 1: In this part you will learn to:

- Design and evaluate the instruction set architectures (both RISC and CISC) and how it can be related to the hardware/software interface in a computer system with a quick review of assembly programming.
- Understand different processor implementation methods including the basic single-cycle implementation and how it can be extended to a multi-cycle, pipelined and superscalar implementations.
- Understand performance evaluation techniques and their relation to the target applications and the processor workload.

Part 2: In this part you will learn to:

- Understand the memory hierarchy in a modern computer system and its impact on the performance of the system. This includes physical and virtual memory systems and basics of cache memories.
- Understand some basic principles of parallel computing using special topics in this course (more advanced materials covered in some elective courses).

1.2.3 Assessment

Three assignments and one test in addition to the final exam. The first assignment is mainly on the instruction set architecture design, hardware/software interfacing and review of assembly programming. The second assignment is related to processor implementation and performance issues. The third assignment is related to memory hierarchy system and multiprocessing.

The test only covers the first part of the course. The final exam covers the whole course.

- Assignment 1: 8% due Fri. 9 August.
- Assignment 2: 7% due Fri. 23 August.
- Assignment 3: 15% due Fri. 4 October.
- Test: 20% (in week 7, Wednesday 11 September)
- Final exam: 50%

Appendix A

[1] D. A. Patterson and J. L. Hennessy, Computer organization and design: The hardware/software interface, 5th ed. Morgan Kaufmann/Elsevier, 2014.