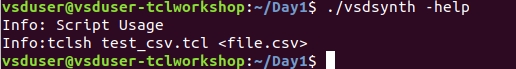
# Introduction to TCL

Tcl is a general-purpose multi-paradigm system programming language. It is a scripting language that aims at providing the ability for applications to communicate with each other.

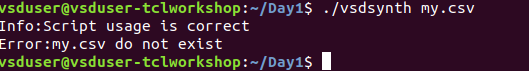
Day -1:

To check the usage of vsdsynth

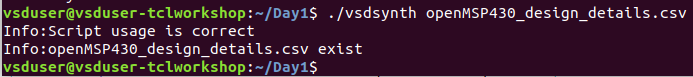




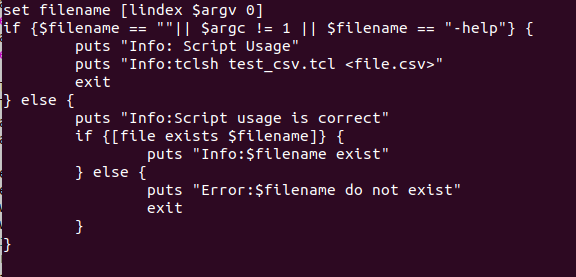
Incorrect CSV file



Usage of command and check to correct if csv file exist

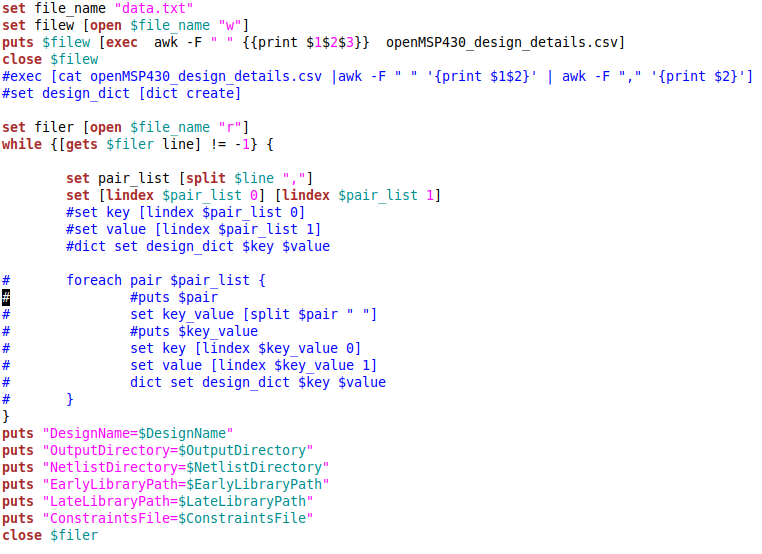


Test\_csv.tcl

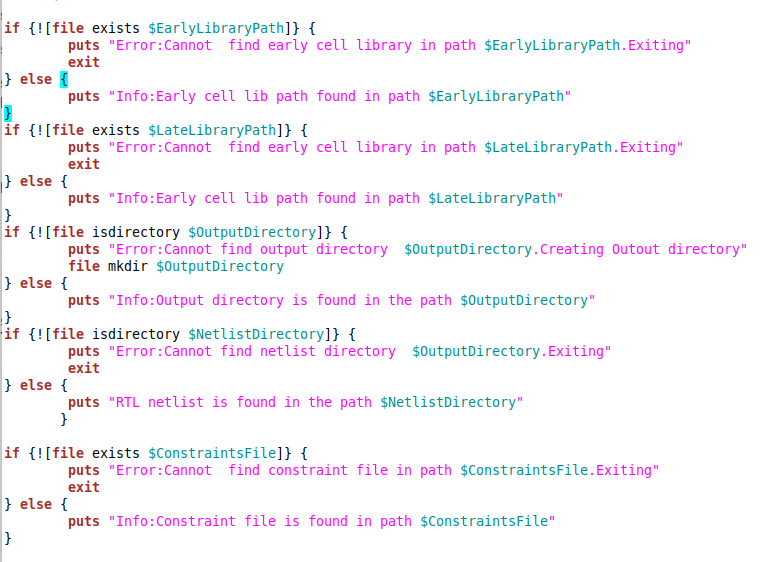


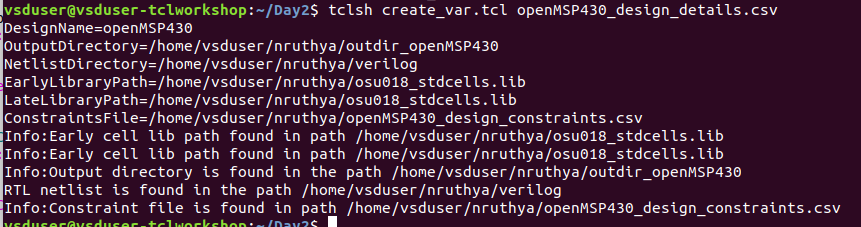
Day-2

Auto create variable using awk command



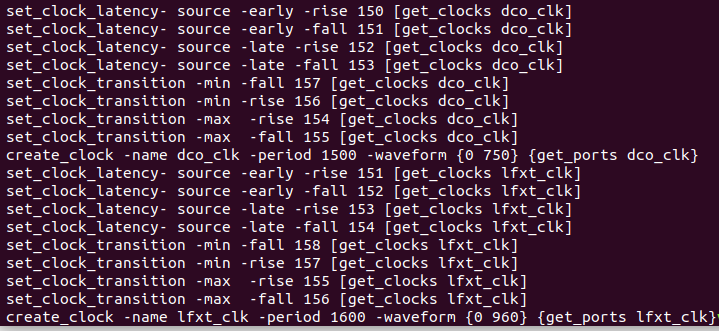
To check if files and folders exist



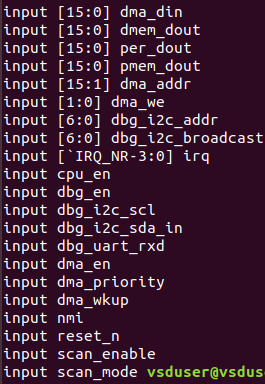


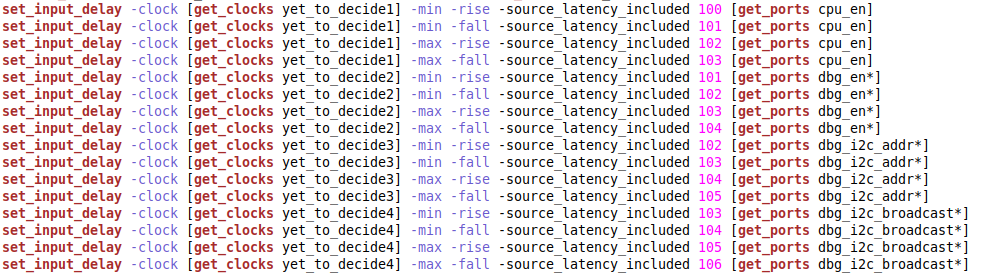
Day-3

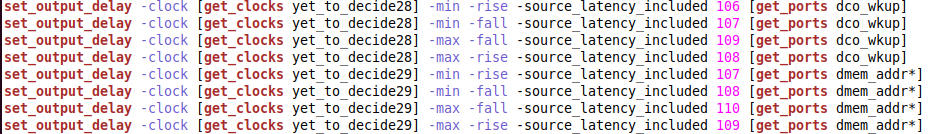
Create clock constraints

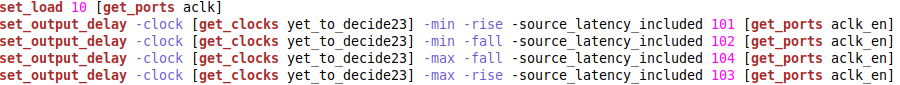


Categorize between busses and bits



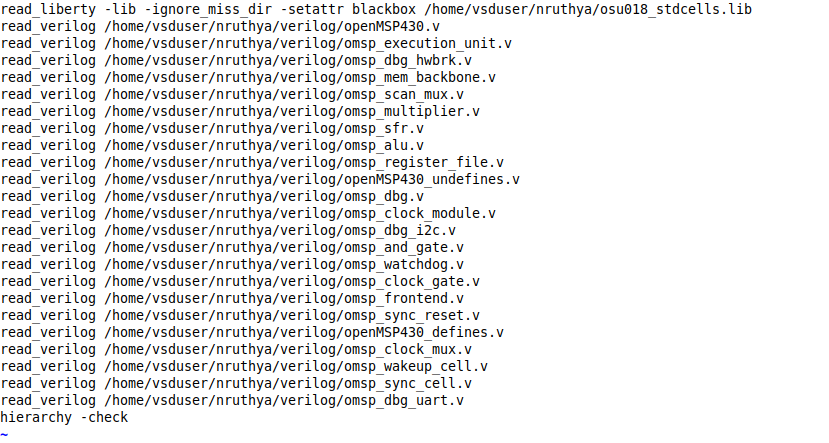






Day-4

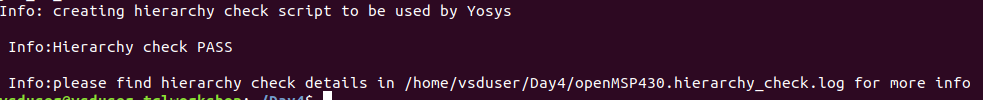
Creating hierarchical check script for yosys open source tool.



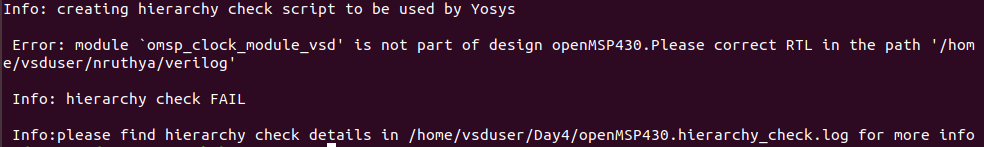
Error handling for hierarchy check

If all the modules in the top module.v file is defined then error\_flag is 0.

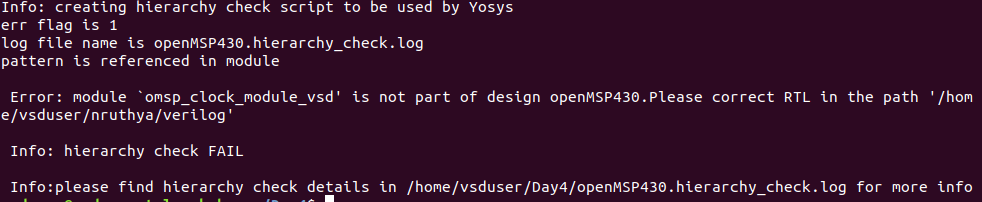
hierarchy check PASS

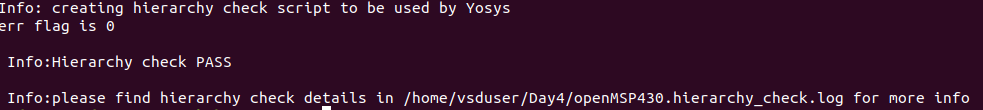


When module is not found=> hierarchy check FAIL



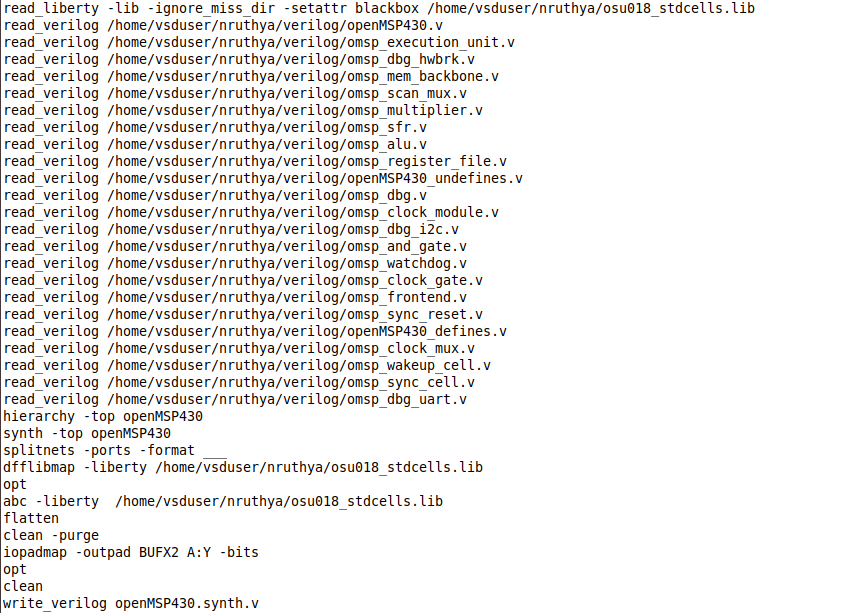




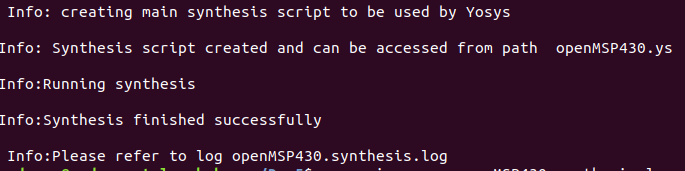


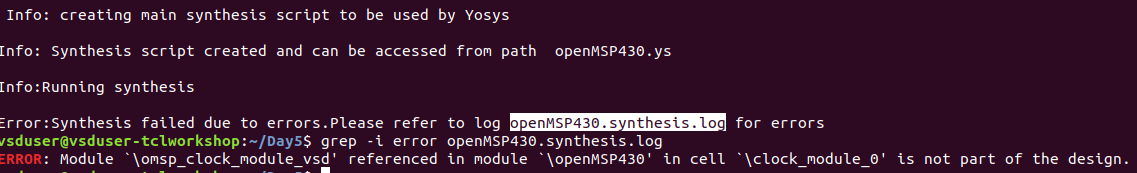
Day-5

Main synthesis script



Running synthesis

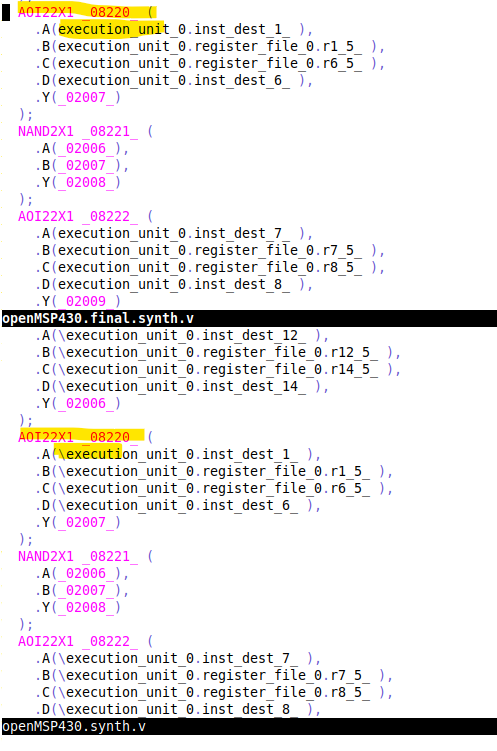




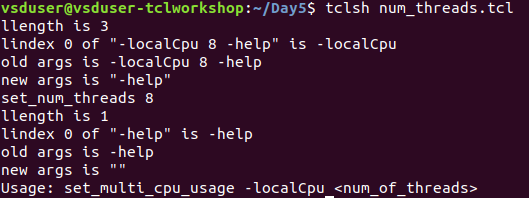
Editing the output netlist

1.removing the statements having stars

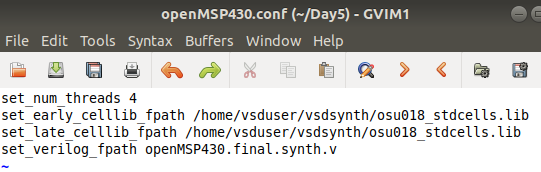
2.Removing slashes to make it compatible to Opentimer tool.

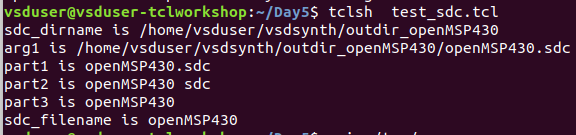


Procs

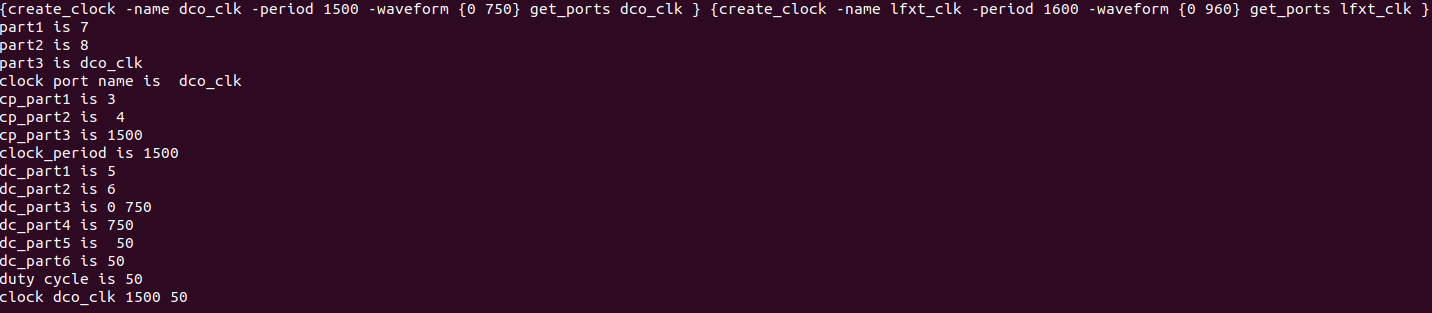


Preparing .conf file for openTimer



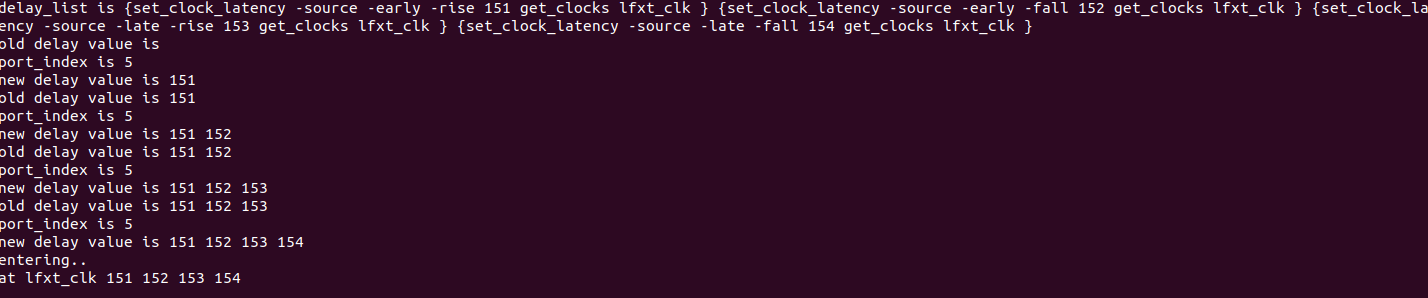
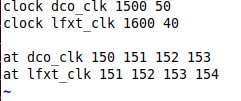


Clock period and duty cycle constraints

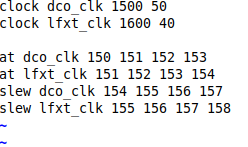




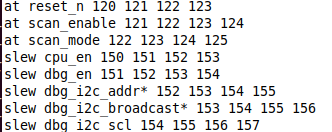
Clock latency constraints are added to the same file.



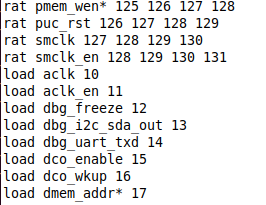
Clock transition Constraints



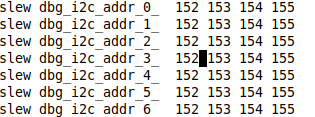
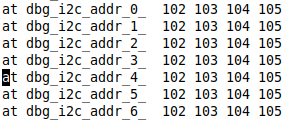
Input delay and transition constraints

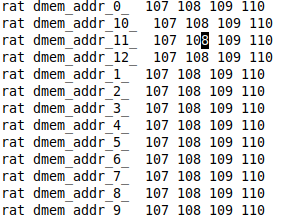


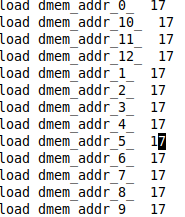
Output delay and load constraints



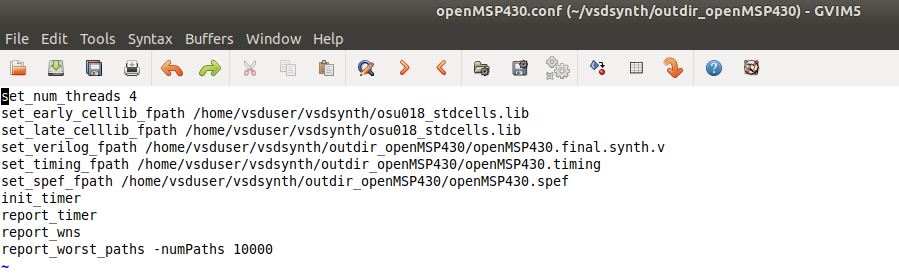
Expand the bussed ports and apply constraints to each and every bit of bussed port







Configuration file for opentimer



Runtime elapsed and Worst RAT slack

Number of Violations

