DVS-MIPI 1GHz Register Configuration

SETFILE INFORMATION

Frame Rate	: 2000 fps
Global Reset	: Off
Global Hold	: On
Fixed Frame	: On
Event Clock	: 125.6 Mhz
MIPI Lane Speed	: 1Gbps
Num Of MIPI Lane	: 4
Data Type	: AER
Payload Size	: 8192
Num of Payload	: 128
OUTPUT Mode	: MIPI
PCLK Speed	: NONE

SYSTEM SETTING

```
s322512     // DTAG_GR_ON_NUM_r
s016631     // EVTH_REF_LSB_r
s300c00     // STREAM_OUT_MODE_r(0 : MIPI, 1 : PARALLEL)
s30a100     // [0] : OUTIF_PARA_ENABLE
s307004     // PLL_P : Default 0x04, 20MHz 0x02
s307101     // PLL_M_MSB : Default 0x01, 20MHz 0x00
s30722C     // PLL_M_LSB : Default 0x2C, 20MHz 0xFA
s307300     // PLL_S : Default 0x00, 20MHz 0x00
s307961     // [7:4] PLL_DIV_G , [3:0] PLL_DIV_DBR
s307a11     // [7:4] PLL_DIV_OP, [3:0] PLL_DIV_OS
s307b25     // [7:4] PLL_DIV_VS, [3:0] PLL_DIV_VP
s307e00     // PLL_PD
s30a001     // OUTIF_ENABLE
s30a211     // DPHY_ENABLE
s30a31f     // DPHY_ENABLE
s30a500     // DPHY_PLL_PMS
s30a68D     // DPHY_PLL_PMS
s30a700     // DPHY_PLL_PMS
s303b40     // TEST PAD CONTROL

s30803F     // CLOCK_ENABLE ([0] : MULTICLK_ENABLE)
s308106     // CLOCK_ENABLE ([3] : DTPDTAG_ENABLE)
s30836c     // CLOCK_ENABLE
```

SYSTEM SETTING

```
s391524     // [5:4] mipi_ck_mode, [3] : use_line, [2] : use_frm, [1] : use_2_lane, [0] : use_1_lane
s39012a     // MIPI_CSI2_DI_r
s390200     // csi2_pkt_size_low
s390320     // csi2_pkt_size_high
s390800     // D-PHY ULPS disable(0x00) enable(0x01)
s391A7F     // frm_cnt_low
s391B00     // frm_cnt_high
s391081     // [7] : use_timeout, [0] : use_big_endian
s39117C     // to_scnt0 (event clock) (1us)
s3912E7     // to_scnt1_low
s391303      // to_scnt1_high (1ms)
s391401     // to_mcnt
s391640     // pkt_gap_low
s391700     // pkt_gap_high
s391800     // frm_gap_low
s391995     // frm_gap_high
s39314c     // [1:0] : HS-TX Regulator Output Level Control,
            // [2] : HS TX Regulator Source Control,
            // [3] : LP TX Regulator Source Control,
            // [6:4] : LP TX Regulator Output Level Control at Current mode
```

SCAN RATE SETTING

```
s321604     // DTAG_SELX_r
s321702     // DTAG_SENSE_r
s32180C     // DTAG_AY_r
s321905     // DTAG_AY_RST_GAP_r
s321A07     // DTAG_APS_RST_r
s321C04     // DTAG_COL_MARGIN_r
```

ANALOG SETTING

```
s01571F     // CRGS Setting
s01660F     // REG_DIV_BCM_BOT_UNIT_AMP
s016707     // REG_DIV_BCM_BOT_UNIT_ON
s01680f     // REG_DIV_BCM_BOT_UNIT_nOFF
```

TIMESTAMP SETTING

```
s32B100     // TSTAMP_SUB_UNIT_VAL_r_MSB
s32B27D     // TSTAMP_SUB_UNIT_VAL_r_LSB
s32B303     // TSTAMP_REF_UNIT_VAL_r_MSB
s32B4E7     // TSTAMP_REF_UNIT_VAL_r_LSB

s311f00
s304001
s430801
s430001
s490001
```

CROP SETTING

```
s330001     // CROP_BYPASS_r
s330100     // CROP_Y_GROUP_START_r
s3302FF     // CROP_Y_START_MASK_r
s330359     // CROP_Y_GROUP_END_r
s3304FF     // CROP_Y_END_MASK_r
s330500     // CROP_START_X_r_MSB
s330600     // CROP_START_X_r_LSB
s330703     // CROP_END_X_r_MSB
s3308BF     // CROP_END_X_r_LSB
s330900     // CROP_FRAME_SKIP_ENABLE_r
s330A01     // CROP_FRAME_REPEAT_NUM_r
s330B00     // CROP_VALID_FRAME_START_NUM_r
s330C00     // CROP_VALID_FRAME_END_NUM_r
```

SLAVE MODE SETTING

```
s3A0001     // [0] : EXT_SYNC_IN_EN_r
s3A0101     // [0] : EXT_SYNC_RISING_SEL_r
s3A0200     // [0] : BURST_TRIGGER_MODE_EN_r
s3A0C00     // ECLK_FINE_COUNT_WIDTH_r_MSB
s3A0D7C     // ECLK_FINE_COUNT_WIDTH_r_LSB
s3A0E03     // ECLK_COARSE_COUNT_WIDTH_r_MSB
s3A0F1F     // ECLK_COARSE_COUNT_WIDTH_r_LSB (1us / LSB)
s3A1000     // FRAME_WIDTH_r
s328300     // [0] : DTAG_MULTI_SENSOR_r
s303B02     // [1] : EXT_SYNC_IN_EN_r
s32B600     // [1] : TSTAMP_EXT_RESET_r
s4c0001
```

STREAMING ON

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s30916C // CCI_ADDRESS_CONTROL_2ND_r
s010001 // MODE_SELECT_r // [0]: Software Standby, [1]: Stream