Summary

Design Name	Hydra_CPLD
Fitting Status	Successful
Software Version	P.20131013
Device Used	XC2C128-7-VQ100
Date	3-21-2024, 10:24AM

RESOURCES SUMMARY

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
70/128 (55%)	222/448 (50%)	46/128 (36%)	46/80 (58%)	181/320 (57%)

PIN RESOURCES

Signal Type	Required	Mapped	Pin Type	Used	Total
Input	34	34	I/O	41	70
Output	11	11	GCK/IO	1	3
Bidirectional	0	0	GTS/IO	3	4
GCK	1	1	GSR/IO	1	1
GTS	0	0	CDR/IO	0	1
GSR	0	0	DGE/IO	0	1

GLOBAL RESOURCES

Signal mapped onto global clock net (GCK0)	IN_clk

back to top print page