```
cpldfit:  version P.20131013                        Xilinx Inc.
                                  Fitter Report
Design Name: Hydra_CPLD                           Date:  3-21-2024, 10:24AM
Device Used: XC2C128-7-VQ100
Fitting Status: Successful

************************  Mapped Resource Summary  **************************

Macrocells     Product Terms    Function Block   Registers      Pins
Used/Tot       Used/Tot         Inps Used/Tot    Used/Tot       Used/Tot
70 /128  ( 55%) 222 /448  ( 50%) 181 /320  ( 57%) 46 /128 ( 36%) 46 /80  ( 57%)

** Function Block Resources **

Function Mcells   FB Inps  Pterms   IO       CTC      CTR      CTS      CTE
Block    Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot
FB1      16/16*    35/40    46/56     4/10    0/1      0/1      0/1      0/1
FB2      16/16*    38/40*   53/56     4/10    0/1      0/1      0/1      0/1
FB3      15/16     38/40*   36/56     2/11    0/1      0/1      0/1      0/1
FB4       8/16     38/40*   35/56     0/11    0/1      0/1      0/1      0/1
FB5      15/16     32/40    52/56     1/10    0/1      0/1      0/1      0/1
FB6       0/16      0/40     0/56     0/ 9    0/1      0/1      0/1      0/1
FB7       0/16      0/40     0/56     0/10    0/1      0/1      0/1      0/1
FB8       0/16      0/40     0/56     0/ 9    0/1      0/1      0/1      0/1
         -----    -------  -------   -----    ---      ---      ---      ---
Total    70/128   181/320  222/448   11/80    0/8      0/8      0/8      0/8

CTC - Control Term Clock
CTR - Control Term Reset
CTS - Control Term Set
CTE - Control Term Output Enable

* - Resource is exhausted

** Global Control Resources **

GCK         GSR         GTS         DGE
Used/Tot    Used/Tot    Used/Tot    Used/Tot
1/3         0/1         0/4         0/1

Signal 'IN_clk' mapped onto global clock net GCK0.

** Pin Resources **

Signal Type    Required     Mapped  |  Pin Type            Used    Total
------------------------------------|------------------------------------
Input          :   34          34    |  I/O              :    41     70
Output         :   11          11    |  GCK/IO           :     1      3
Bidirectional  :    0           0    |  GTS/IO           :     3      4
GCK            :    1           1    |  GSR/IO           :     1      1
GTS            :    0           0    |  CDR/IO           :     0      1
GSR            :    0           0    |  DGE/IO           :     0      1
                  ----        ----
        Total     46          46

End of Mapped Resource Summary
 *************************  Errors and Warnings  ***************************

WARNING:Cpld - Unable to retrieve the path to the iSE Project Repository. Will
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   use the default filename of 'Hydra_CPLD.ise'.
WARNING:Cpld - PULLUP specified for net 'OUT_clkbuf_en<2>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'OUT_clkbuf_en<1>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<7>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<6>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<5>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<4>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<3>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<2>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<1>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_period_dip<0>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<9>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<8>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<7>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<6>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<5>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<4>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<3>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<31>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<30>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<2>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<29>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<28>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<27>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<26>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<25>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<24>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<23>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<22>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<21>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<20>' conflicts with
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   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<1>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<19>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<18>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<17>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<16>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<15>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<14>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<13>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<12>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<11>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<10>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLUP specified for net 'IN_delay_dip<0>' conflicts with
   previous KEEPER specification.  PULLUP is ignored.
WARNING:Cpld - PULLDOWN specified for net 'IN_aux_fakra' conflicts with previous
   KEEPER specification.  PULLDOWN is ignored.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<0>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<1>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<2>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<3>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<4>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<5>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
WARNING:Cpld:1007 - Removing unused input(s) 'IN_period_dip<6>'.  The input(s)
   are unused after optimization. Please verify functionality via simulation.
 *************************  Summary of Mapped Logic  ************************

** 11 Outputs **

Signal                                  Total  Total  Bank  Loc      Pin   Pin       Pin
Name                                    Pts    Inps                  No.   Type      Use
OUT_clkbuf_en<1>                        0      0      2     FB1_1    13    I/O       O
OUT_clkbuf_en<2>                        0      0      2     FB1_3    12    I/O       O
OUT_delay_clk                           3      5      2     FB1_15   4     GTS/I/O   O
OUT_delay_d                             12     19     2     FB1_16   3     GTS/I/O   O
OUT_led<7>                              2      3      1     FB2_2    14    I/O       O
OUT_led<8>                              2      4      1     FB2_3    15    I/O       O
OUT_led<9>                              2      4      1     FB2_4    16    I/O       O
OUT_led<10>                             3      5      1     FB2_5    17    I/O       O
OUT_delay_e                             3      7      2     FB3_3    1     GTS/I/O   O
OUT_frame_trig                          4      7      2     FB3_4    99    GSR/I/O   O
OUT_aux_fakra                           1      1      2     FB5_1    65    I/O       O

** 59 Buried Nodes **
```

Signal Name	Total Pts	Total Inps	Loc	Reg Use	Reg Init State
i<0>	2	6	FB1_2	TFF	RESET
ctr_mux0000<9>12	2	4	FB1_4		
i<7>	1	3	FB1_5	TFF	RESET
i<6>	1	3	FB1_6	TFF	RESET
N_PZ_303	9	16	FB1_7		
i<1>	2	7	FB1_8	TFF	RESET
i<2>	2	8	FB1_9	TFF	RESET
i<3>	2	8	FB1_10	TFF	RESET
i<5>	1	3	FB1_11	TFF	RESET
N_PZ_309	4	8	FB1_12		
state_FSM_FFd2	3	5	FB1_13	DFF	RESET
i<4>	2	9	FB1_14	TFF	RESET
ctr<11>	7	10	FB2_1	DFF	RESET
ctr<10>	3	6	FB2_6	TFF	RESET
ctr<12>	5	8	FB2_7	TFF	RESET
ctr_mux0000<15>1	2	4	FB2_8		
ctr_mux0000<9>17	3	8	FB2_9		
state_FSM_FFd1	4	8	FB2_10	DFF	RESET
N_PZ_377	2	7	FB2_11		
state_FSM_FFd3	4	8	FB2_12	DFF	RESET
N_PZ_193	2	15	FB2_13		
state_cmp_le0000	7	19	FB2_14		
ctr<26>	3	23	FB2_15	TFF	RESET
ctr<25>	3	22	FB2_16	TFF	RESET
ctr<21>	3	21	FB3_1	TFF	RESET
N_PZ_372	2	3	FB3_5		
N_PZ_257	1	4	FB3_6		
ctr<8>	3	4	FB3_7	DFF	RESET
ctr<7>	3	8	FB3_8	TFF	RESET
ctr<6>	3	6	FB3_9	TFF	RESET
ctr<0>	2	3	FB3_10	DFF	RESET
N_PZ_262	1	5	FB3_11		
N_PZ_253	1	3	FB3_12		
N_PZ_169	2	12	FB3_13		
ctr<19>	3	22	FB3_14	TFF	RESET
ctr<23>	3	22	FB3_15	TFF	RESET
ctr<22>	3	22	FB3_16	TFF	RESET
ctr<4>	3	8	FB4_2	DFF	RESET
ctr<3>	3	6	FB4_3	TFF	RESET
ctr<2>	3	5	FB4_8	DFF	RESET

Signal Name	Total Pts	Total Inps	Loc	Reg Use	Reg Init State
ctr<1>	2	4	FB4_9	DFF	RESET
Mmux__COND_1_Result122	16	21	FB4_10		
ctr<13>	2	7	FB4_14	DFF	RESET
ctr<9>	3	5	FB4_15	TFF	RESET
ctr<5>	3	5	FB4_16	DFF	RESET
N_PZ_362	1	3	FB5_3		
ctr<24>	3	19	FB5_4	DFF	RESET
state_cmp_le0001	3	10	FB5_5		
ctr<18>	3	13	FB5_6	DFF	RESET
Mcompar_state_cmp_le0001_G_B_000_02730	5	12	FB5_7		
ctr<17>	3	12	FB5_8	DFF	RESET
ctr<16>	3	10	FB5_9	TFF	RESET
ctr<15>	3	9	FB5_10	DFF	RESET
ctr<20>	4	16	FB5_11	DFF	RESET

state_cmp_lt0004	7	20	FB5_12		
state_cmp_lt0000	6	20	FB5_13		
state_cmp_lt0002	5	21	FB5_14		
state_cmp_lt0001	3	20	FB5_15		
ctr<14>	2	8	FB5_16	DFF	RESET

** 35 Inputs **

Signal Name	Bank	Loc	Pin No.	Pin Type	Pin Use	I/O STD
IN_clk	1	FB2_13	22	GCK/I/O	GCK	LVCMOS1
IN_delay_dip<15>	2	FB3_6	96	I/O	I	LVCMOS3
IN_delay_dip<14>	2	FB3_7	95	I/O	I	LVCMOS3
IN_delay_dip<13>	2	FB3_11	94	I/O	I	LVCMOS3
IN_delay_dip<12>	2	FB3_13	93	I/O	I	LVCMOS3
IN_delay_dip<11>	2	FB3_14	92	I/O	I	LVCMOS3
IN_delay_dip<10>	2	FB3_15	91	I/O	I	LVCMOS3
IN_delay_dip<9>	2	FB3_16	90	I/O	I	LVCMOS3
IN_aux_fakra	2	FB5_2	66	I/O	I	LVCMOS3
IN_delay_dip<24>	2	FB5_3	67	I/O	I	LVCMOS3
IN_delay_dip<25>	2	FB5_5	68	I/O	I	LVCMOS3
IN_delay_dip<26>	2	FB5_7	70	I/O	I	LVCMOS3
IN_delay_dip<27>	2	FB5_11	71	I/O	I	LVCMOS3
IN_delay_dip<28>	2	FB5_12	72	I/O	I	LVCMOS3
IN_delay_dip<29>	2	FB5_13	73	I/O	I	LVCMOS3
IN_delay_dip<30>	2	FB5_14	74	I/O	I	LVCMOS3
IN_delay_dip<31>	2	FB5_15	76	I/O	I	LVCMOS3
IN_delay_dip<7>	1	FB6_1	64	I/O	I	LVCMOS1
IN_delay_dip<6>	1	FB6_2	63	I/O	I	LVCMOS1
IN_delay_dip<5>	1	FB6_3	61	I/O	I	LVCMOS1
IN_delay_dip<4>	1	FB6_4	60	I/O	I	LVCMOS1
IN_delay_dip<3>	1	FB6_5	59	I/O	I	LVCMOS1
IN_delay_dip<2>	1	FB6_6	58	I/O	I	LVCMOS1
IN_delay_dip<1>	1	FB6_16	54	I/O	I	LVCMOS1
IN_delay_dip<16>	2	FB7_1	77	I/O	I	LVCMOS3
IN_delay_dip<17>	2	FB7_2	78	I/O	I	LVCMOS3
IN_delay_dip<18>	2	FB7_4	79	I/O	I	LVCMOS3
IN_delay_dip<19>	2	FB7_5	80	I/O	I	LVCMOS3
IN_delay_dip<20>	2	FB7_6	81	I/O	I	LVCMOS3
IN_delay_dip<21>	2	FB7_11	82	I/O	I	LVCMOS3
IN_delay_dip<22>	2	FB7_13	85	I/O	I	LVCMOS3
IN_delay_dip<23>	2	FB7_14	86	I/O	I	LVCMOS3
IN_delay_dip<8>	2	FB7_15	87	I/O	I	LVCMOS3
IN_delay_dip<0>	1	FB8_2	53	I/O	I	LVCMOS1
IN_period_dip<7>	1	FB8_13	44	I/O	I	LVCMOS1

Legend:
Pin No. - ~ - User Assigned
I/O Style - OD - OpenDrain
- PU - Pullup
- KPR - Keeper
- S - SchmittTrigger
- DG - DataGate
Reg Use - LATCH - Transparent latch
- DFF - D-flip-flop
- DEFF - D-flip-flop with clock enable
- TFF - T-flip-flop
- TDFF - Dual-edge-triggered T-flip-flop
- DDFF - Dual-edge-triggered flip-flop
- DDEFF - Dual-edge-triggered flip-flop with clock enable

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          /S (after any above flop/latch type) indicates initial state is Set
  *************************  Function Block Details  ************************
Legend:
Total Pt     - Total product terms used by the macrocell signal
Loc          - Location where logic was mapped in device
Pin Type/Use - I   - Input             GCK - Global clock
               O   - Output            GTS - Global Output Enable
              (b) - Buried macrocell   GSR - Global Set/Reset
              VRF - Vref
Pin No.      - ~   - User Assigned
 ********************************** FB1  ***********************************
This function block is part of I/O Bank number:                 2
Number of function block inputs used/remaining:                 35/5
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     46/10
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
OUT_clkbuf_en<1>                0     FB1_1   13   I/O     O
i<0>                            2     FB1_2        (b)     (b)
OUT_clkbuf_en<2>                0     FB1_3   12   I/O     O
ctr_mux0000<9>12                2     FB1_4   11   I/O     (b)
i<7>                            1     FB1_5   10   I/O     (b)
i<6>                            1     FB1_6   9    I/O     (b)
N_PZ_303                        9     FB1_7        (b)     (b)
i<1>                            2     FB1_8        (b)     (b)
i<2>                            2     FB1_9        (b)     (b)
i<3>                            2     FB1_10       (b)     (b)
i<5>                            1     FB1_11  8    I/O     (b)
N_PZ_309                        4     FB1_12  7    I/O     (b)
state_FSM_FFd2                  3     FB1_13  6    I/O     (b)
i<4>                            2     FB1_14       (b)     (b)
OUT_delay_clk                   3     FB1_15  4    GTS/I/O O
OUT_delay_d                     12    FB1_16  3    GTS/I/O O

Signals Used by Logic in Function Block
  1: IN_delay_dip<11>  13: IN_delay_dip<3>         25: i<2>
  2: IN_delay_dip<13>  14: IN_delay_dip<5>         26: i<3>
  3: IN_delay_dip<15>  15: IN_delay_dip<7>         27: i<4>
  4: IN_delay_dip<17>  16: IN_delay_dip<9>         28: i<5>
  5: IN_delay_dip<19>  17: Mmux__COND_1_Result122  29: i<6>
  6: IN_delay_dip<1>   18: N_PZ_303                30: i<7>
  7: IN_delay_dip<21>  19: N_PZ_309                31: state_FSM_FFd1
  8: IN_delay_dip<23>  20: OUT_delay_clk           32: state_FSM_FFd2
  9: IN_delay_dip<25>  21: OUT_delay_d             33: state_FSM_FFd3
 10: IN_delay_dip<27>  22: ctr_mux0000<9>12        34: state_cmp_lt0001
 11: IN_delay_dip<29>  23: i<0>                    35: state_cmp_lt0002
 12: IN_delay_dip<31>  24: i<1>

Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
OUT_clkbuf_en<1>  ..................................... 0
i<0>              ................X...X........XXXX..... 6
OUT_clkbuf_en<2>  ..................................... 0
ctr_mux0000<9>12  ............................XXXX..... 4
i<7>              ...........................X.XX....... 3
i<6>              ............................X..XX....... 3
N_PZ_303          .X.X.XX.X.X..X.XX......XXXX....XXX...... 16
i<1>              ................X...XX.......XXXX..... 7
i<2>              ................X...XXX......XXXX..... 8
i<3>              ................X..XXXXX.....XX....... 8
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i<5>              ........................X...XX....... 3
N_PZ_309          ......................XXXXXXXX.......... 8
state_FSM_FFd2    ..................X..X........XXX....... 5
i<4>              ..................X..XXXXXX....XX....... 9
OUT_delay_clk     ...................X.X.........XXX...... 5
OUT_delay_d       X.X.X..X.X.XX.X.XX..X.XXXXX....XXX...... 19
                 0----+----1----+----2----+----3----+----4
                           0         0         0         0
 ********************************* FB2  ***********************************
```

This function block is part of I/O Bank number: 1
Number of function block inputs used/remaining: 38/2
Number of function block control terms used/remaining: 0/4
Number of PLA product terms used/remaining: 53/3

Signal Name	Total Pt	Loc	Pin No.	Pin Type	Pin Use	CTC	CTR	CTS	CTE
ctr<11>	7	FB2_1		(b)	(b)				
OUT_led<7>	2	FB2_2	14	I/O	O				
OUT_led<8>	2	FB2_3	15	I/O	O				
OUT_led<9>	2	FB2_4	16	I/O	O				
OUT_led<10>	3	FB2_5	17	I/O	O				
ctr<10>	3	FB2_6	18	I/O	(b)				
ctr<12>	5	FB2_7		(b)	(b)				
ctr_mux0000<15>1	2	FB2_8		(b)	(b)				
ctr_mux0000<9>17	3	FB2_9		(b)	(b)				
state_FSM_FFd1	4	FB2_10		(b)	(b)				
N_PZ_377	2	FB2_11	19	I/O	(b)				
state_FSM_FFd3	4	FB2_12		(b)	(b)				
N_PZ_193	2	FB2_13	22	GCK/I/O	GCK				
state_cmp_le0000	7	FB2_14	23	GCK/I/O	(b)				
ctr<26>	3	FB2_15	24	CDR/I/O	(b)				
ctr<25>	3	FB2_16	27	GCK/I/O	(b)				

Signals Used by Logic in Function Block

1: IN_aux_fakra	14: ctr<14>	27: ctr<8>
2: IN_period_dip<7>	15: ctr<15>	28: ctr<9>
3: N_PZ_253	16: ctr<16>	29: ctr_mux0000<15>1
4: N_PZ_262	17: ctr<17>	30: ctr_mux0000<9>12
5: N_PZ_362	18: ctr<18>	31: ctr_mux0000<9>17
6: OUT_led<10>	19: ctr<19>	32: state_FSM_FFd1
7: OUT_led<7>	20: ctr<20>	33: state_FSM_FFd2
8: OUT_led<8>	21: ctr<21>	34: state_FSM_FFd3
9: OUT_led<9>	22: ctr<22>	35: state_cmp_le0000
10: ctr<10>	23: ctr<23>	36: state_cmp_le0001
11: ctr<11>	24: ctr<24>	37: state_cmp_lt0000
12: ctr<12>	25: ctr<25>	38: state_cmp_lt0004
13: ctr<13>	26: ctr<26>	

```
Signal                  1         2         3         4 FB
Name             0----+----0----+----0----+----0----+----0 Inputs
ctr<11>           ..XXX....XX..............XXXXX......... 10
OUT_led<7>        ......X.........................XX...... 3
OUT_led<8>        .......X......................XXX...... 4
OUT_led<9>        ..X.....X.....................XX...... 4
OUT_led<10>       ..X..X........................XXX...... 5
ctr<10>           ..XX.....X.............XX..X......... 6
ctr<12>           ..XXX......X............X.XXX......... 8
ctr_mux0000<15>1  ..............................XXX..X... 4
ctr_mux0000<9>17  ............................XX.X.XXXXX.. 8
state_FSM_FFd1    X.X............................X.XXXXX.. 8
N_PZ_377          ..XXX......XX............X...X......... 7
```

```
state_FSM_FFd3    XXX............................XXX..XX.. 8
N_PZ_193          ....X......XXXXXXXXXXXXX..X.............. 15
state_cmp_le0000  .........XXXXXXXXXXXXXXXXXXX............ 19
ctr<26>           ..XXX....XXXXXXXXXXXXXXXXXXX..X......... 23
ctr<25>           ..XXX....XXXXXXXXXXXXXXXX.XX..X......... 22
                 0----+----1----+----2----+----3----+----4
                           0         0         0         0
 ********************************* FB3  ***********************************
This function block is part of I/O Bank number:                 2
Number of function block inputs used/remaining:                 38/2
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     36/20
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
ctr<21>                         3     FB3_1        (b)     (b)
(unused)                        0     FB3_2   2    GTS/I/O
OUT_delay_e                     3     FB3_3   1    GTS/I/O O
OUT_frame_trig                  4     FB3_4   99   GSR/I/O O
N_PZ_372                        2     FB3_5   97   I/O     (b)
N_PZ_257                        1     FB3_6   96   I/O     I
ctr<8>                          3     FB3_7   95   I/O     I
ctr<7>                          3     FB3_8        (b)     (b)
ctr<6>                          3     FB3_9        (b)     (b)
ctr<0>                          2     FB3_10       (b)     (b)
N_PZ_262                        1     FB3_11  94   I/O     I
N_PZ_253                        1     FB3_12       (b)     (b)
N_PZ_169                        2     FB3_13  93   I/O     I
ctr<19>                         3     FB3_14  92   I/O     I
ctr<23>                         3     FB3_15  91   I/O     I
ctr<22>                         3     FB3_16  90   I/O     I

Signals Used by Logic in Function Block
  1: Mcompar_state_cmp_le0001_G_B_000_02730  14: ctr<16>           27: ctr<6>
  2: N_PZ_253                                15: ctr<17>           28: ctr<7>
  3: N_PZ_257                                16: ctr<18>           29: ctr<8>
  4: N_PZ_262                                17: ctr<19>           30: ctr_mux0000<9
  5: N_PZ_309                                18: ctr<1>            31: state_FSM_FFd
  6: N_PZ_362                                19: ctr<20>           32: state_FSM_FFd
  7: OUT_delay_e                             20: ctr<21>           33: state_FSM_FFd
  8: OUT_frame_trig                          21: ctr<22>           34: state_cmp_le0
  9: ctr<0>                                  22: ctr<23>           35: state_cmp_le0
 10: ctr<12>                                 23: ctr<2>            36: state_cmp_lt0
 11: ctr<13>                                 24: ctr<3>            37: state_cmp_lt0
 12: ctr<14>                                 25: ctr<4>            38: state_cmp_lt0
 13: ctr<15>                                 26: ctr<5>

Signal                    1         2         3         4 FB
Name                 0----+----0----+----0----+----0----+----0 Inputs
ctr<21>               XXXX.X..XXXXXXXXX.XX.....XXXXX.......... 21
OUT_delay_e           ....X.X.......................XX..XXX.. 7
OUT_frame_trig        .......X......................XXXXXX.... 7
N_PZ_372              .X......X.....................X.......... 3
N_PZ_257              ..................X....XXX............... 4
ctr<8>                .X.X........................XX.......... 4
ctr<7>                .XXX....X..................XXX.X.......... 8
ctr<6>                .XX.....X..................XX..X.......... 6
ctr<0>                .X......X.....................X.......... 3
N_PZ_262              ..X.....X..................XXX............ 5
N_PZ_253              ............................XXX........ 3
N_PZ_169              X....X..XXX....XX.X......XXXX.......... 12
```

```
ctr<19>           XX.X.X..XXXXXXXXXX....XXXXXXXX.......... 22
ctr<23>           .XXX.X..XXXXXXXXX.XXXX...XXXXX.......... 22
ctr<22>           XXXX.X..XXXXXXXXX.XXX....XXXXX.......... 22
                 0----+----1----+----2----+----3----+----4
                           0         0         0         0
 ********************************** FB4  **********************************
This function block is part of I/O Bank number:                1
Number of function block inputs used/remaining:                38/2
Number of function block control terms used/remaining:         0/4
Number of PLA product terms used/remaining:                    35/21
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
(unused)                        0     FB4_1   28   DGE/I/O
ctr<4>                          3     FB4_2        (b)     (b)
ctr<3>                          3     FB4_3        (b)     (b)
(unused)                        0     FB4_4   29   I/O
(unused)                        0     FB4_5   30   I/O
(unused)                        0     FB4_6   32   I/O
(unused)                        0     FB4_7   33   I/O
ctr<2>                          3     FB4_8        (b)     (b)
ctr<1>                          2     FB4_9        (b)     (b)
Mmux__COND_1_Result122          16    FB4_10       (b)     (b)
(unused)                        0     FB4_11  34   I/O
(unused)                        0     FB4_12  35   I/O
(unused)                        0     FB4_13  36   I/O
ctr<13>                         2     FB4_14  37   I/O     (b)
ctr<9>                          3     FB4_15  39   I/O     (b)
ctr<5>                          3     FB4_16  40   I/O     (b)

Signals Used by Logic in Function Block
  1: IN_delay_dip<0>   14: IN_delay_dip<4>   27: ctr<2>
  2: IN_delay_dip<10>  15: IN_delay_dip<6>   28: ctr<3>
  3: IN_delay_dip<12>  16: IN_delay_dip<8>   29: ctr<4>
  4: IN_delay_dip<14>  17: N_PZ_253          30: ctr<5>
  5: IN_delay_dip<16>  18: N_PZ_257          31: ctr<8>
  6: IN_delay_dip<18>  19: N_PZ_262          32: ctr<9>
  7: IN_delay_dip<20>  20: N_PZ_362          33: ctr_mux0000<9>17
  8: IN_delay_dip<22>  21: N_PZ_372          34: i<0>
  9: IN_delay_dip<24>  22: N_PZ_377          35: i<1>
 10: IN_delay_dip<26>  23: ctr<0>            36: i<2>
 11: IN_delay_dip<28>  24: ctr<12>           37: i<3>
 12: IN_delay_dip<2>   25: ctr<13>           38: i<4>
 13: IN_delay_dip<30>  26: ctr<1>

Signal                      1         2         3         4 FB
Name               0----+----0----+----0----+----0----+----0 Inputs
ctr<4>              .................X..X.X..XXXX...X....... 8
ctr<3>              ...................X.X..XXX....X....... 6
ctr<2>              ...................X.X..XX.....X....... 5
ctr<1>              ...................X.X..X......X....... 4
Mmux__COND_1_Result122
                    XXXXXXXXXXXXXXXX.................XXXXX.. 21
ctr<13>             .................XX.X.XX.....X.X....... 7
ctr<9>              ...............X.X...........XXX....... 5
ctr<5>              .................X..X.X......X..X....... 5
                   0----+----1----+----2----+----3----+----4
                             0         0         0         0
 ********************************** FB5  **********************************
This function block is part of I/O Bank number:                2
Number of function block inputs used/remaining:                32/8
```

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Number of function block control terms used/remaining:        0/4
Number of PLA product terms used/remaining:                   52/4
Signal                        Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                          Pt            No.  Type    Use
OUT_aux_fakra                 1     FB5_1   65   I/O     O
(unused)                      0     FB5_2   66   I/O     I
N_PZ_362                      1     FB5_3   67   I/O     I
ctr<24>                       3     FB5_4        (b)     (b)
state_cmp_le0001              3     FB5_5   68   I/O     I
ctr<18>                       3     FB5_6        (b)     (b)
Mcompar_state_cmp_le0001_G_B_000_02730
                              5     FB5_7   70   I/O     I
ctr<17>                       3     FB5_8        (b)     (b)
ctr<16>                       3     FB5_9        (b)     (b)
ctr<15>                       3     FB5_10       (b)     (b)
ctr<20>                       4     FB5_11  71   I/O     I
state_cmp_lt0004              7     FB5_12  72   I/O     I
state_cmp_lt0000              6     FB5_13  73   I/O     I
state_cmp_lt0002              5     FB5_14  74   I/O     I
state_cmp_lt0001              3     FB5_15  76   I/O     I
ctr<14>                       2     FB5_16       (b)     (b)

Signals Used by Logic in Function Block
  1: IN_aux_fakra                              12: ctr<12>          23: ctr<23>
  2: Mcompar_state_cmp_le0001_G_B_000_02730    13: ctr<13>          24: ctr<24>
  3: N_PZ_169                                  14: ctr<14>          25: ctr<25>
  4: N_PZ_193                                  15: ctr<15>          26: ctr<26>
  5: N_PZ_253                                  16: ctr<16>          27: ctr<5>
  6: N_PZ_257                                  17: ctr<17>          28: ctr<6>
  7: N_PZ_262                                  18: ctr<18>          29: ctr<7>
  8: N_PZ_362                                  19: ctr<19>          30: ctr<8>
  9: N_PZ_377                                  20: ctr<20>          31: ctr<9>
 10: ctr<10>                                   21: ctr<21>          32: ctr_mux0000<9
 11: ctr<11>                                   22: ctr<22>

Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
OUT_aux_fakra      X..................................... 1
N_PZ_362           .........XX...................X........ 3
ctr<24>            ...X..XXX..XXXXXXXXXXXXX.....X.X..... 19
state_cmp_le0001   .X..............XXXXXXXXX.............. 10
ctr<18>            .X....XXX..XXXXXXX...........X.X..... 13
Mcompar_state_cmp_le0001_G_B_000_02730
                   .......X.XXXXXXXX..........XXX.......... 12
ctr<17>            .X....XXX..XXXXXX............X.X..... 12
ctr<16>            ......XXX..XXXXX.............X.X..... 10
ctr<15>            ......XXX..XXXX..............X.X..... 9
ctr<20>            ..X.XXXX...XXXXXXXXX.........X.X..... 16
state_cmp_lt0004   .........XXXXXXXXXXXXXXXXX..XXX..... 20
state_cmp_lt0000   .........XXXXXXXXXXXXXXXXX..XXX..... 20
state_cmp_lt0002   .........XXXXXXXXXXXXXXXXX.XXXX..... 21
state_cmp_lt0001   .......X...XXXXXXXXXXXXXXXXXXX..... 20
ctr<14>            ......XXX..XXX...............X.X..... 8
                  0----+----1----+----2----+----3----+----4
                            0         0         0         0
 ********************************** FB6  ***********************************
This function block is part of I/O Bank number:               1
Number of function block inputs used/remaining:               0/40
Number of function block control terms used/remaining:        0/4
Number of PLA product terms used/remaining:                   0/56
```

Signal Name	Total Pt	Loc	Pin No.	Pin Type	Pin Use	CTC	CTR	CTS	CTE
(unused)	0	FB6_1	64	I/O	I				
(unused)	0	FB6_2	63	I/O	I				
(unused)	0	FB6_3	61	I/O	I				
(unused)	0	FB6_4	60	I/O	I				
(unused)	0	FB6_5	59	I/O	I				
(unused)	0	FB6_6	58	I/O	I				
(unused)	0	FB6_7		(b)					
(unused)	0	FB6_8		(b)					
(unused)	0	FB6_9		(b)					
(unused)	0	FB6_10		(b)					
(unused)	0	FB6_11		(b)					
(unused)	0	FB6_12	56	I/O					
(unused)	0	FB6_13		(b)					
(unused)	0	FB6_14	55	I/O					
(unused)	0	FB6_15		(b)					
(unused)	0	FB6_16	54	I/O	I				

********** FB7 **********

This function block is part of I/O Bank number: 2
Number of function block inputs used/remaining: 0/40
Number of function block control terms used/remaining: 0/4
Number of PLA product terms used/remaining: 0/56

Signal Name	Total Pt	Loc	Pin No.	Pin Type	Pin Use	CTC	CTR	CTS	CTE
(unused)	0	FB7_1	77	I/O	I				
(unused)	0	FB7_2	78	I/O	I				
(unused)	0	FB7_3		(b)					
(unused)	0	FB7_4	79	I/O	I				
(unused)	0	FB7_5	80	I/O	I				
(unused)	0	FB7_6	81	I/O	I				
(unused)	0	FB7_7		(b)					
(unused)	0	FB7_8		(b)					
(unused)	0	FB7_9		(b)					
(unused)	0	FB7_10		(b)					
(unused)	0	FB7_11	82	I/O	I				
(unused)	0	FB7_12		(b)					
(unused)	0	FB7_13	85	I/O	I				
(unused)	0	FB7_14	86	I/O	I				
(unused)	0	FB7_15	87	I/O	I				
(unused)	0	FB7_16	89	I/O					

********** FB8 **********

This function block is part of I/O Bank number: 1
Number of function block inputs used/remaining: 0/40
Number of function block control terms used/remaining: 0/4
Number of PLA product terms used/remaining: 0/56

Signal Name	Total Pt	Loc	Pin No.	Pin Type	Pin Use	CTC	CTR	CTS	CTE
(unused)	0	FB8_1		(b)					
(unused)	0	FB8_2	53	I/O	I				
(unused)	0	FB8_3	52	I/O					
(unused)	0	FB8_4	50	I/O					
(unused)	0	FB8_5		(b)					
(unused)	0	FB8_6	49	I/O					
(unused)	0	FB8_7		(b)					
(unused)	0	FB8_8		(b)					
(unused)	0	FB8_9		(b)					
(unused)	0	FB8_10		(b)					
(unused)	0	FB8_11		(b)					
(unused)	0	FB8_12	46	I/O					

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(unused)                        0     FB8_13  44   I/O     I
(unused)                        0     FB8_14  43   I/O
(unused)                        0     FB8_15  42   I/O
(unused)                        0     FB8_16  41   I/O
 ********************************  Equations  ********************************

********** Mapped Logic **********


Mcompar_state_cmp_le0001_G_B_000_02730 <= ((ctr(14) AND ctr(12) AND ctr(16) AND ctr(
        ctr(17))
        OR (ctr(14) AND ctr(13) AND ctr(16) AND ctr(15) AND
        ctr(17))
        OR (ctr(14) AND ctr(16) AND ctr(15) AND N_PZ_362 AND
        ctr(17))
        OR (ctr(14) AND ctr(11) AND ctr(10) AND ctr(8) AND ctr(16) AND
        ctr(15) AND ctr(7) AND ctr(17))
        OR (ctr(14) AND ctr(11) AND ctr(10) AND ctr(8) AND ctr(16) AND
        ctr(15) AND ctr(6) AND ctr(17)));


Mmux__COND_1_Result122 <= ((i(4) AND i(3) AND i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(30))
        OR (i(4) AND i(3) AND i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(28))
        OR (i(4) AND i(3) AND NOT i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(26))
        OR (i(4) AND i(3) AND NOT i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(24))
        OR (i(4) AND NOT i(3) AND i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(22))
        OR (i(4) AND NOT i(3) AND i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(20))
        OR (i(4) AND NOT i(3) AND NOT i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(18))
        OR (i(4) AND NOT i(3) AND NOT i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(16))
        OR (NOT i(4) AND i(3) AND i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(14))
        OR (NOT i(4) AND i(3) AND i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(12))
        OR (NOT i(4) AND i(3) AND NOT i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(10))
        OR (NOT i(4) AND i(3) AND NOT i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(8))
        OR (NOT i(4) AND NOT i(3) AND i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(6))
        OR (NOT i(4) AND NOT i(3) AND i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(4))
        OR (NOT i(4) AND NOT i(3) AND NOT i(2) AND i(1) AND NOT i(0) AND
        IN_delay_dip(2))
        OR (NOT i(4) AND NOT i(3) AND NOT i(2) AND NOT i(1) AND NOT i(0) AND
        IN_delay_dip(0)));


N_PZ_169 <= ((NOT ctr(20))
        OR (ctr(12) AND ctr(13) AND ctr(8) AND N_PZ_362 AND ctr(7) AND
        ctr(6) AND ctr(0) AND ctr(5) AND
        Mcompar_state_cmp_le0001_G_B_000_02730 AND ctr(18) AND ctr(19)));
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N_PZ_193 <= ((NOT ctr(24))
        OR (ctr(14) AND ctr(12) AND ctr(13) AND ctr(8) AND ctr(16) AND
        ctr(15) AND N_PZ_362 AND ctr(17) AND ctr(18) AND ctr(19) AND
        ctr(20) AND ctr(21) AND ctr(22) AND ctr(23)));


N_PZ_253 <= (NOT state_FSM_FFd3 AND NOT state_FSM_FFd1 AND state_FSM_FFd2);


N_PZ_257 <= (ctr(1) AND ctr(2) AND ctr(3) AND ctr(4));


N_PZ_262 <= (ctr(7) AND ctr(6) AND ctr(0) AND ctr(5) AND N_PZ_257);


N_PZ_303 <= ((state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND i(1) AND NOT Mmux__COND_1_Result122)
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND i(4) AND i(3) AND i(2) AND NOT Mmux__COND_1_Result122
        NOT IN_delay_dip(29))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND i(4) AND i(3) AND NOT i(2) AND NOT Mmux__COND_1_Resul
        NOT IN_delay_dip(25))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND i(4) AND NOT i(3) AND i(2) AND NOT Mmux__COND_1_Resul
        NOT IN_delay_dip(21))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND i(4) AND NOT i(3) AND NOT i(2) AND NOT Mmux__COND_1_R
        NOT IN_delay_dip(17))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT i(4) AND i(3) AND i(2) AND NOT Mmux__COND_1_Resul
        NOT IN_delay_dip(13))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT i(4) AND i(3) AND NOT i(2) AND NOT Mmux__COND_1_R
        NOT IN_delay_dip(9))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT i(4) AND NOT i(3) AND i(2) AND NOT Mmux__COND_1_R
        NOT IN_delay_dip(5))
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT i(4) AND NOT i(3) AND NOT i(2) AND NOT Mmux__COND
        NOT IN_delay_dip(1)));


N_PZ_309 <= ((i(5))
        OR (i(6))
        OR (i(7))
        OR (i(4) AND i(3) AND i(2) AND i(1) AND i(0)));


N_PZ_362 <= (ctr(11) AND ctr(10) AND ctr(9));


N_PZ_372 <= ((N_PZ_253)
        OR (NOT ctr_mux0000(9)17 AND NOT ctr(0)));


N_PZ_377 <= ((ctr_mux0000(9)17 AND NOT N_PZ_253)
        OR (ctr(12) AND ctr(13) AND ctr(8) AND NOT N_PZ_253 AND
        N_PZ_362 AND N_PZ_262));
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OUT_aux_fakra <= IN_aux_fakra;


OUT_clkbuf_en(1) <= NOT ('0');


OUT_clkbuf_en(2) <= '0';

FDCPE_OUT_delay_clk: FDCPE port map (OUT_delay_clk,OUT_delay_clk_D,IN_clk,'0','0','1
OUT_delay_clk_D <= ((NOT state_cmp_lt0001 AND ctr_mux0000(9)12)
        OR (state_FSM_FFd3 AND NOT ctr_mux0000(9)12 AND
        OUT_delay_clk)
        OR (state_FSM_FFd2 AND NOT ctr_mux0000(9)12 AND
        OUT_delay_clk));

FDCPE_OUT_delay_d: FDCPE port map (OUT_delay_d,OUT_delay_d_D,IN_clk,'0','0','1');
OUT_delay_d_D <= ((state_FSM_FFd2 AND OUT_delay_d)
        OR (NOT i(1) AND N_PZ_303)
        OR (NOT state_cmp_lt0001 AND state_FSM_FFd3 AND OUT_delay_d)
        OR (state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT i(0) AND NOT Mmux__COND_1_Result122)
        OR (i(4) AND i(3) AND i(2) AND NOT IN_delay_dip(31) AND
        N_PZ_303)
        OR (i(4) AND i(3) AND NOT i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(27))
        OR (i(4) AND NOT i(3) AND i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(23))
        OR (i(4) AND NOT i(3) AND NOT i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(19))
        OR (NOT i(4) AND i(3) AND i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(15))
        OR (NOT i(4) AND i(3) AND NOT i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(11))
        OR (NOT i(4) AND NOT i(3) AND i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(7))
        OR (NOT i(4) AND NOT i(3) AND NOT i(2) AND N_PZ_303 AND
        NOT IN_delay_dip(3)));

FTCPE_OUT_delay_e: FTCPE port map (OUT_delay_e,OUT_delay_e_T,IN_clk,'0','0','1');
OUT_delay_e_T <= ((NOT state_FSM_FFd3 AND state_cmp_lt0000 AND
        NOT state_FSM_FFd2 AND OUT_delay_e)
        OR (NOT state_FSM_FFd3 AND NOT state_cmp_lt0000 AND
        NOT state_FSM_FFd2 AND NOT OUT_delay_e)
        OR (NOT state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT state_cmp_lt0002 AND N_PZ_309 AND OUT_delay_e));

FDCPE_OUT_frame_trig: FDCPE port map (OUT_frame_trig,OUT_frame_trig_D,IN_clk,'0','0'
OUT_frame_trig_D <= ((state_FSM_FFd3 AND state_cmp_lt0000 AND
        state_FSM_FFd1)
        OR (state_FSM_FFd3 AND NOT state_FSM_FFd1 AND OUT_frame_trig)
        OR (NOT state_FSM_FFd1 AND state_FSM_FFd2 AND OUT_frame_trig)
        OR (NOT state_FSM_FFd3 AND state_FSM_FFd1 AND
        NOT state_cmp_le0000 AND state_cmp_le0001));

FDCPE_OUT_led7: FDCPE port map (OUT_led(7),OUT_led_D(7),IN_clk,'0','0','1');
OUT_led_D(7) <= NOT (((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2)
        OR (state_FSM_FFd2 AND NOT OUT_led(7))));
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FTCPE_OUT_led8: FTCPE port map (OUT_led(8),OUT_led_T(8),IN_clk,'0','0','1');
OUT_led_T(8) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND OUT_led(8))
        OR (state_FSM_FFd3 AND NOT state_FSM_FFd1 AND state_FSM_FFd2 AND
        NOT OUT_led(8)));

FDCPE_OUT_led9: FDCPE port map (OUT_led(9),OUT_led_D(9),IN_clk,'0','0','1');
OUT_led_D(9) <= NOT (((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2)
        OR (NOT N_PZ_253 AND NOT OUT_led(9))));

FDCPE_OUT_led10: FDCPE port map (OUT_led(10),OUT_led_D(10),IN_clk,'0','0','1');
OUT_led_D(10) <= ((state_FSM_FFd3 AND state_FSM_FFd1)
        OR (state_FSM_FFd3 AND NOT N_PZ_253 AND OUT_led(10))
        OR (NOT N_PZ_253 AND state_FSM_FFd2 AND OUT_led(10)));

FDCPE_ctr0: FDCPE port map (ctr(0),ctr_D(0),IN_clk,'0','0','1');
ctr_D(0) <= ((NOT ctr_mux0000(9)17 AND NOT ctr(0))
        OR (N_PZ_253 AND ctr(0)));

FDCPE_ctr1: FDCPE port map (ctr(1),ctr_D(1),IN_clk,'0','0','1');
ctr_D(1) <= ((ctr(1) AND N_PZ_372)
        OR (NOT ctr_mux0000(9)17 AND ctr(0) AND NOT ctr(1)));

FDCPE_ctr2: FDCPE port map (ctr(2),ctr_D(2),IN_clk,'0','0','1');
ctr_D(2) <= ((N_PZ_372 AND ctr(2))
        OR (NOT ctr_mux0000(9)17 AND NOT ctr(1) AND ctr(2))
        OR (NOT ctr_mux0000(9)17 AND ctr(0) AND ctr(1) AND NOT ctr(2)));

FTCPE_ctr3: FTCPE port map (ctr(3),ctr_T(3),IN_clk,'0','0','1');
ctr_T(3) <= ((ctr_mux0000(9)17 AND NOT N_PZ_372 AND ctr(3))
        OR (ctr(1) AND NOT N_PZ_372 AND ctr(2) AND ctr(3))
        OR (NOT ctr_mux0000(9)17 AND ctr(0) AND ctr(1) AND ctr(2) AND
        NOT ctr(3)));

FDCPE_ctr4: FDCPE port map (ctr(4),ctr_D(4),IN_clk,'0','0','1');
ctr_D(4) <= ((N_PZ_372 AND ctr(4))
        OR (NOT ctr_mux0000(9)17 AND NOT N_PZ_257 AND ctr(4))
        OR (NOT ctr_mux0000(9)17 AND ctr(0) AND NOT N_PZ_257 AND ctr(1) AND
        ctr(2) AND ctr(3)));

FDCPE_ctr5: FDCPE port map (ctr(5),ctr_D(5),IN_clk,'0','0','1');
ctr_D(5) <= ((ctr(5) AND N_PZ_372)
        OR (NOT ctr_mux0000(9)17 AND ctr(5) AND NOT N_PZ_257)
        OR (NOT ctr_mux0000(9)17 AND ctr(0) AND NOT ctr(5) AND N_PZ_257));

FTCPE_ctr6: FTCPE port map (ctr(6),ctr_T(6),IN_clk,'0','0','1');
ctr_T(6) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(6))
        OR (NOT ctr_mux0000(9)17 AND NOT ctr(6) AND ctr(0) AND ctr(5) AND
        N_PZ_257)
        OR (NOT N_PZ_253 AND ctr(6) AND ctr(0) AND ctr(5) AND N_PZ_257));

FTCPE_ctr7: FTCPE port map (ctr(7),ctr_T(7),IN_clk,'0','0','1');
ctr_T(7) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(7))
        OR (NOT N_PZ_253 AND N_PZ_262 AND ctr(7))
        OR (NOT ctr_mux0000(9)17 AND NOT N_PZ_262 AND ctr(6) AND ctr(0) AND
        ctr(5) AND N_PZ_257));

FDCPE_ctr8: FDCPE port map (ctr(8),ctr_D(8),IN_clk,'0','0','1');
ctr_D(8) <= ((ctr(8) AND N_PZ_253)
        OR (NOT ctr_mux0000(9)17 AND ctr(8) AND NOT N_PZ_262)
        OR (NOT ctr_mux0000(9)17 AND NOT ctr(8) AND N_PZ_262));
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FTCPE_ctr9: FTCPE port map (ctr(9),ctr_T(9),IN_clk,'0','0','1');
ctr_T(9) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(9))
        OR (NOT ctr_mux0000(9)17 AND ctr(8) AND NOT ctr(9) AND N_PZ_262)
        OR (ctr(8) AND NOT N_PZ_253 AND ctr(9) AND N_PZ_262));

FTCPE_ctr10: FTCPE port map (ctr(10),ctr_T(10),IN_clk,'0','0','1');
ctr_T(10) <= ((ctr(10) AND ctr_mux0000(9)17 AND NOT N_PZ_253)
        OR (ctr(10) AND ctr(8) AND NOT N_PZ_253 AND ctr(9) AND
        N_PZ_262)
        OR (NOT ctr(10) AND NOT ctr_mux0000(9)17 AND ctr(8) AND ctr(9) AND
        N_PZ_262));

FDCPE_ctr11: FDCPE port map (ctr(11),ctr_D(11),IN_clk,'0','0','1');
ctr_D(11) <= NOT (((NOT ctr(11) AND NOT ctr(10))
        OR (NOT ctr(11) AND NOT ctr(8))
        OR (NOT ctr(11) AND NOT ctr(9))
        OR (NOT ctr(11) AND NOT N_PZ_262)
        OR (NOT ctr_mux0000(15)1 AND NOT ctr(11) AND ctr_mux0000(9)17 AND
        NOT ctr_mux0000(9)12)
        OR (NOT ctr_mux0000(15)1 AND ctr_mux0000(9)17 AND NOT N_PZ_253 AND
        NOT ctr_mux0000(9)12)
        OR (ctr(8) AND NOT N_PZ_253 AND N_PZ_362 AND N_PZ_262)));

FTCPE_ctr12: FTCPE port map (ctr(12),ctr_T(12),IN_clk,'0','0','1');
ctr_T(12) <= ((ctr(12) AND NOT ctr_mux0000(15)1 AND ctr_mux0000(9)17 AND
        NOT N_PZ_253 AND NOT ctr_mux0000(9)12)
        OR (ctr(12) AND ctr(8) AND NOT N_PZ_253 AND N_PZ_362 AND
        N_PZ_262)
        OR (NOT ctr(12) AND ctr_mux0000(15)1 AND ctr(8) AND N_PZ_362 AND
        N_PZ_262)
        OR (NOT ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(8) AND N_PZ_362 AND
        N_PZ_262)
        OR (NOT ctr(12) AND ctr(8) AND ctr_mux0000(9)12 AND N_PZ_362 AND
        N_PZ_262));

FDCPE_ctr13: FDCPE port map (ctr(13),ctr_D(13),IN_clk,'0','0','1');
ctr_D(13) <= ((ctr(13) AND NOT N_PZ_377)
        OR (ctr(12) AND NOT ctr_mux0000(9)17 AND NOT ctr(13) AND ctr(8) AND
        N_PZ_362 AND N_PZ_262));

FDCPE_ctr14: FDCPE port map (ctr(14),ctr_D(14),IN_clk,'0','0','1');
ctr_D(14) <= ((ctr(14) AND NOT N_PZ_377)
        OR (NOT ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND N_PZ_362 AND N_PZ_262));

FDCPE_ctr15: FDCPE port map (ctr(15),ctr_D(15),IN_clk,'0','0','1');
ctr_D(15) <= ((ctr(15) AND NOT N_PZ_377)
        OR (NOT ctr(14) AND NOT ctr_mux0000(9)17 AND ctr(15))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND NOT ctr(15) AND N_PZ_362 AND N_PZ_262));

FTCPE_ctr16: FTCPE port map (ctr(16),ctr_T(16),IN_clk,'0','0','1');
ctr_T(16) <= ((ctr_mux0000(9)17 AND ctr(16) AND N_PZ_377)
        OR (ctr(14) AND ctr(16) AND ctr(15) AND N_PZ_377)
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND NOT ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262));

FDCPE_ctr17: FDCPE port map (ctr(17),ctr_D(17),IN_clk,'0','0','1');
ctr_D(17) <= ((NOT N_PZ_377 AND ctr(17))
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        OR (NOT ctr_mux0000(9)17 AND ctr(17) AND
        NOT Mcompar_state_cmp_le0001_G_B_000_02730)
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        NOT ctr(17)));

FDCPE_ctr18: FDCPE port map (ctr(18),ctr_D(18),IN_clk,'0','0','1');
ctr_D(18) <= ((NOT N_PZ_377 AND ctr(18))
        OR (NOT ctr_mux0000(9)17 AND
        NOT Mcompar_state_cmp_le0001_G_B_000_02730 AND ctr(18))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND NOT ctr(18)));

FTCPE_ctr19: FTCPE port map (ctr(19),ctr_T(19),IN_clk,'0','0','1');
ctr_T(19) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(19))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND NOT ctr(19))
        OR (ctr(12) AND ctr(13) AND ctr(8) AND NOT N_PZ_253 AND
        N_PZ_362 AND ctr(7) AND ctr(6) AND ctr(0) AND ctr(5) AND ctr(1) AND
        ctr(2) AND ctr(3) AND ctr(4) AND
        Mcompar_state_cmp_le0001_G_B_000_02730 AND ctr(18) AND ctr(19)));

FDCPE_ctr20: FDCPE port map (ctr(20),ctr_D(20),IN_clk,'0','0','1');
ctr_D(20) <= ((NOT ctr_mux0000(9)17 AND NOT N_PZ_169)
        OR (N_PZ_253 AND ctr(20))
        OR (NOT ctr_mux0000(9)17 AND NOT N_PZ_257 AND ctr(20))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND NOT ctr(20)));

FTCPE_ctr21: FTCPE port map (ctr(21),ctr_T(21),IN_clk,'0','0','1');
ctr_T(21) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(21))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND NOT ctr(21))
        OR (ctr(12) AND ctr(13) AND ctr(8) AND NOT N_PZ_253 AND
        N_PZ_362 AND ctr(7) AND ctr(6) AND ctr(0) AND ctr(5) AND N_PZ_257 AND
        Mcompar_state_cmp_le0001_G_B_000_02730 AND ctr(18) AND ctr(19) AND ctr(20) A

FTCPE_ctr22: FTCPE port map (ctr(22),ctr_T(22),IN_clk,'0','0','1');
ctr_T(22) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(22))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND ctr(21) AND
        NOT ctr(22))
        OR (ctr(12) AND ctr(13) AND ctr(8) AND NOT N_PZ_253 AND
        N_PZ_362 AND ctr(7) AND ctr(6) AND ctr(0) AND ctr(5) AND N_PZ_257 AND
        Mcompar_state_cmp_le0001_G_B_000_02730 AND ctr(18) AND ctr(19) AND ctr(20) A
        ctr(22)));

FTCPE_ctr23: FTCPE port map (ctr(23),ctr_T(23),IN_clk,'0','0','1');
ctr_T(23) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(23))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND ctr(21) AND
        ctr(22) AND NOT ctr(23))
        OR (ctr(14) AND ctr(12) AND ctr(13) AND ctr(8) AND
        NOT N_PZ_253 AND ctr(16) AND ctr(15) AND N_PZ_362 AND ctr(7) AND ctr(6) AND
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        ctr(0) AND ctr(5) AND N_PZ_257 AND ctr(17) AND ctr(18) AND
        ctr(19) AND ctr(20) AND ctr(21) AND ctr(22) AND ctr(23)));

FDCPE_ctr24: FDCPE port map (ctr(24),ctr_D(24),IN_clk,'0','0','1');
ctr_D(24) <= ((NOT ctr_mux0000(9)17 AND NOT N_PZ_193)
        OR (NOT N_PZ_377 AND ctr(24))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND ctr(21) AND
        ctr(22) AND ctr(23) AND NOT ctr(24)));

FTCPE_ctr25: FTCPE port map (ctr(25),ctr_T(25),IN_clk,'0','0','1');
ctr_T(25) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(25))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND ctr(21) AND
        ctr(22) AND ctr(23) AND ctr(24) AND NOT ctr(25))
        OR (ctr(14) AND ctr(12) AND ctr(11) AND ctr(10) AND
        ctr(13) AND ctr(8) AND NOT N_PZ_253 AND ctr(16) AND ctr(15) AND ctr(9) AND
        N_PZ_262 AND ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND
        ctr(21) AND ctr(22) AND ctr(23) AND ctr(24) AND ctr(25)));

FTCPE_ctr26: FTCPE port map (ctr(26),ctr_T(26),IN_clk,'0','0','1');
ctr_T(26) <= ((ctr_mux0000(9)17 AND NOT N_PZ_253 AND ctr(26))
        OR (ctr(14) AND ctr(12) AND NOT ctr_mux0000(9)17 AND ctr(13) AND
        ctr(8) AND ctr(16) AND ctr(15) AND N_PZ_362 AND N_PZ_262 AND
        ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND ctr(21) AND
        ctr(22) AND ctr(23) AND ctr(24) AND ctr(25) AND NOT ctr(26))
        OR (ctr(14) AND ctr(12) AND ctr(11) AND ctr(10) AND
        ctr(13) AND ctr(8) AND NOT N_PZ_253 AND ctr(16) AND ctr(15) AND ctr(9) AND
        N_PZ_262 AND ctr(17) AND ctr(18) AND ctr(19) AND ctr(20) AND
        ctr(21) AND ctr(22) AND ctr(23) AND ctr(24) AND ctr(25) AND
        ctr(26)));


ctr_mux0000(9)17 <= ((NOT ctr_mux0000(15)1 AND NOT state_FSM_FFd1 AND
        NOT ctr_mux0000(9)12)
        OR (NOT ctr_mux0000(15)1 AND NOT state_FSM_FFd3 AND
        NOT state_cmp_le0000 AND NOT state_cmp_le0001)
        OR (state_FSM_FFd3 AND NOT state_cmp_lt0000 AND
        NOT state_cmp_lt0004 AND NOT ctr_mux0000(9)12));


ctr_mux0000(9)12 <= ((state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2)
        OR (state_FSM_FFd3 AND NOT state_FSM_FFd2 AND
        state_cmp_lt0002));


ctr_mux0000(15)1 <= ((NOT state_FSM_FFd3 AND state_cmp_lt0000 AND
        NOT state_FSM_FFd2)
        OR (state_FSM_FFd3 AND state_cmp_lt0000 AND
        NOT state_FSM_FFd1 AND state_FSM_FFd2));

FTCPE_i0: FTCPE port map (i(0),i_T(0),IN_clk,'0','0','1');
i_T(0) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(0))
        OR (NOT state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT state_cmp_lt0002 AND NOT N_PZ_309));

FTCPE_i1: FTCPE port map (i(1),i_T(1),IN_clk,'0','0','1');
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i_T(1) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(1))
        OR (NOT state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT state_cmp_lt0002 AND NOT N_PZ_309 AND i(0)));

FTCPE_i2: FTCPE port map (i(2),i_T(2),IN_clk,'0','0','1');
i_T(2) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(2))
        OR (NOT state_cmp_lt0001 AND state_FSM_FFd3 AND
        NOT state_FSM_FFd2 AND NOT state_cmp_lt0002 AND NOT N_PZ_309 AND i(1) AND i(

FTCPE_i3: FTCPE port map (i(3),i_T(3),IN_clk,'0','0','1');
i_T(3) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(3))
        OR (state_FSM_FFd3 AND NOT state_FSM_FFd2 AND
        NOT ctr_mux0000(9)12 AND NOT N_PZ_309 AND i(2) AND i(1) AND i(0)));

FTCPE_i4: FTCPE port map (i(4),i_T(4),IN_clk,'0','0','1');
i_T(4) <= ((NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(4))
        OR (state_FSM_FFd3 AND NOT state_FSM_FFd2 AND
        NOT ctr_mux0000(9)12 AND NOT N_PZ_309 AND i(3) AND i(2) AND i(1) AND i(0)));

FTCPE_i5: FTCPE port map (i(5),i_T(5),IN_clk,'0','0','1');
i_T(5) <= (NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(5));

FTCPE_i6: FTCPE port map (i(6),i_T(6),IN_clk,'0','0','1');
i_T(6) <= (NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(6));

FTCPE_i7: FTCPE port map (i(7),i_T(7),IN_clk,'0','0','1');
i_T(7) <= (NOT state_FSM_FFd3 AND NOT state_FSM_FFd2 AND i(7));

FDCPE_state_FSM_FFd1: FDCPE port map (state_FSM_FFd1,state_FSM_FFd1_D,IN_clk,'0','0'
state_FSM_FFd1_D <= NOT (((NOT IN_aux_fakra AND N_PZ_253)
        OR (NOT state_FSM_FFd1 AND NOT N_PZ_253)
        OR (state_FSM_FFd3 AND NOT state_cmp_lt0000 AND
        NOT state_cmp_lt0004)
        OR (NOT state_FSM_FFd3 AND NOT N_PZ_253 AND NOT state_cmp_le0000 AND
        NOT state_cmp_le0001)));

FDCPE_state_FSM_FFd2: FDCPE port map (state_FSM_FFd2,state_FSM_FFd2_D,IN_clk,'0','0'
state_FSM_FFd2_D <= ((state_FSM_FFd1)
        OR (state_FSM_FFd2 AND NOT ctr_mux0000(9)12)
        OR (state_FSM_FFd3 AND NOT ctr_mux0000(9)12 AND N_PZ_309));

FDCPE_state_FSM_FFd3: FDCPE port map (state_FSM_FFd3,state_FSM_FFd3_D,IN_clk,'0','0'
state_FSM_FFd3_D <= ((state_FSM_FFd3 AND state_cmp_lt0000)
        OR (NOT state_cmp_lt0000 AND NOT state_FSM_FFd2)
        OR (IN_aux_fakra AND N_PZ_253 AND IN_period_dip(7))
        OR (state_FSM_FFd3 AND state_FSM_FFd1 AND
        state_cmp_lt0004));


state_cmp_le0000 <= ((NOT ctr(20) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AN
        NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND
        NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(16) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(22) AND
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(22) AND
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(12) AND NOT ctr(15) AND NOT ctr(18) AND
        NOT ctr(19) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25)
        NOT ctr(26))
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        OR (NOT ctr(14) AND NOT ctr(13) AND NOT ctr(15) AND NOT ctr(18) AND
        NOT ctr(19) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25)
        NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(11) AND NOT ctr(10) AND NOT ctr(8) AND NOT ctr(1
        NOT ctr(9) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(22) AND NOT ctr(23) A
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26)));


state_cmp_le0001 <= ((NOT ctr(20) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AN
        NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND
        NOT ctr(25) AND NOT ctr(26))
        OR (NOT Mcompar_state_cmp_le0001_G_B_000_02730 AND NOT ctr(18) AND
        NOT ctr(19) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25)
        NOT ctr(26)));


state_cmp_lt0000 <= ((NOT ctr(17) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AN
        NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AND
        NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(12) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(15) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22)
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(11) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(15) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22)
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(10) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(15) AND NOT ctr(9) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) A
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(10) AND NOT ctr(13) AND NOT ctr(8) AND NOT ctr(1
        NOT ctr(15) AND NOT ctr(7) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) A
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26)));


state_cmp_lt0001 <= ((NOT ctr(14) AND NOT ctr(16) AND NOT ctr(15) AND NOT ctr(17) AN
        NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22)
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(12) AND NOT ctr(13) AND NOT ctr(16) AND NOT ctr(15) AND
        NOT N_PZ_362 AND NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20)
        NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25)
        NOT ctr(26))
        OR (NOT ctr(12) AND NOT ctr(13) AND NOT ctr(8) AND NOT ctr(16) AND NOT ctr(1
        NOT ctr(7) AND NOT ctr(6) AND NOT ctr(5) AND NOT ctr(17) AND NOT ctr(18) AND
        NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24)
        NOT ctr(25) AND NOT ctr(26)));


state_cmp_lt0002 <= ((NOT ctr(16) AND NOT ctr(15) AND NOT ctr(17) AND NOT ctr(18) AN
        NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23)
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(12) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21)
        NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(11) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21)
        NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(10) AND NOT ctr(13) AND NOT ctr(16) AND
        NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AND NOT ctr(20) AND NOT ctr(21)
        NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
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        OR (NOT ctr(14) AND NOT ctr(13) AND NOT ctr(8) AND NOT ctr(16) AND NOT ctr(9
        NOT ctr(7) AND NOT ctr(6) AND NOT ctr(17) AND NOT ctr(18) AND NOT ctr(19) AN
        NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25)
        NOT ctr(26)));


state_cmp_lt0004 <= ((NOT ctr(17) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AN
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(18) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(19) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(20) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23) AND
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(16) AND NOT ctr(15) AND NOT ctr(21) AND NOT ctr(22) AND
        NOT ctr(23) AND NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(12) AND NOT ctr(11) AND NOT ctr(10) AND
        NOT ctr(13) AND NOT ctr(16) AND NOT ctr(21) AND NOT ctr(22) AND NOT ctr(23)
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26))
        OR (NOT ctr(14) AND NOT ctr(12) AND NOT ctr(11) AND NOT ctr(13) AND NOT ctr(
        NOT ctr(16) AND NOT ctr(9) AND NOT ctr(7) AND NOT ctr(21) AND NOT ctr(22) AN
        NOT ctr(24) AND NOT ctr(25) AND NOT ctr(26)));


Register Legend:
 FDCPE (Q,D,C,CLR,PRE,CE);
 FDDCPE (Q,D,C,CLR,PRE,CE);
 FTCPE (Q,D,C,CLR,PRE,CE);
 FTDCPE (Q,D,C,CLR,PRE,CE);
 LDCP  (Q,D,G,CLR,PRE);

 ******************************  Device Pin Out *****************************

Device : XC2C128-7-VQ100


   ----------------------------------------------------
  /100 98  96  94  92  90  88  86  84  82  80  78  76  \
 |   99  97  95  93  91  89  87  85  83  81  79  77    |
 | 1                                                75  |
 | 2                                                74  |
 | 3                                                73  |
 | 4                                                72  |
 | 5                                                71  |
 | 6                                                70  |
 | 7                                                69  |
 | 8                                                68  |
 | 9                                                67  |
 | 10                                               66  |
 | 11                                               65  |
 | 12                                               64  |
 | 13               XC2C128-7-VQ100                 63  |
 | 14                                               62  |
 | 15                                               61  |
 | 16                                               60  |
 | 17                                               59  |
 | 18                                               58  |
 | 19                                               57  |
 | 20                                               56  |
 | 21                                               55  |
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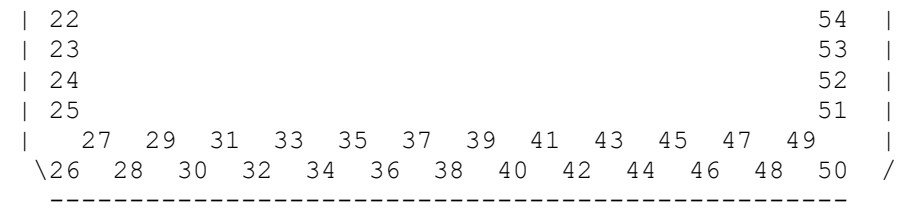

Pin No.	Signal Name	Pin No.	Signal Name
1	OUT_delay_e	51	VCCIO-1.8
2	KPR	52	KPR
3	OUT_delay_d	53	IN_delay_dip<0>
4	OUT_delay_clk	54	IN_delay_dip<1>
5	VCCAUX	55	KPR
6	KPR	56	KPR
7	KPR	57	VCC
8	KPR	58	IN_delay_dip<2>
9	KPR	59	IN_delay_dip<3>
10	KPR	60	IN_delay_dip<4>
11	KPR	61	IN_delay_dip<5>
12	OUT_clkbuf_en<2>	62	GND
13	OUT_clkbuf_en<1>	63	IN_delay_dip<6>
14	OUT_led<7>	64	IN_delay_dip<7>
15	OUT_led<8>	65	OUT_aux_fakra
16	OUT_led<9>	66	IN_aux_fakra
17	OUT_led<10>	67	IN_delay_dip<24>
18	KPR	68	IN_delay_dip<25>
19	KPR	69	GND
20	VCCIO-1.8	70	IN_delay_dip<26>
21	GND	71	IN_delay_dip<27>
22	IN_clk	72	IN_delay_dip<28>
23	KPR	73	IN_delay_dip<29>
24	KPR	74	IN_delay_dip<30>
25	GND	75	GND
26	VCC	76	IN_delay_dip<31>
27	KPR	77	IN_delay_dip<16>
28	KPR	78	IN_delay_dip<17>
29	KPR	79	IN_delay_dip<18>
30	KPR	80	IN_delay_dip<19>
31	GND	81	IN_delay_dip<20>
32	KPR	82	IN_delay_dip<21>
33	KPR	83	TDO
34	KPR	84	GND
35	KPR	85	IN_delay_dip<22>
36	KPR	86	IN_delay_dip<23>
37	KPR	87	IN_delay_dip<8>
38	VCCIO-1.8	88	VCCIO-3.3
39	KPR	89	KPR
40	KPR	90	IN_delay_dip<9>
41	KPR	91	IN_delay_dip<10>
42	KPR	92	IN_delay_dip<11>
43	KPR	93	IN_delay_dip<12>
44	IN_period_dip<7>	94	IN_delay_dip<13>
45	TDI	95	IN_delay_dip<14>
46	KPR	96	IN_delay_dip<15>
47	TMS	97	KPR
48	TCK	98	VCCIO-3.3
49	KPR	99	OUT_frame_trig

```
 50 KPR                              100 GND


Legend :  NC  = Not Connected, unbonded pin
         PGND  = Unused I/O configured as additional Ground pin
          KPR  = Unused I/O with weak keeper (leave unconnected)
          WPU  = Unused I/O with weak pull up (leave unconnected)
          TIE  = Unused I/O floating -- must tie to VCC, GND or other signal
          VCC  = Dedicated Power Pin
       VCCAUX  = Power supply for JTAG pins
    VCCIO-3.3  = I/O supply voltage for LVTTL, LVCMOS33, SSTL3_I
    VCCIO-2.5  = I/O supply voltage for LVCMOS25, SSTL2_I
    VCCIO-1.8  = I/O supply voltage for LVCMOS18
    VCCIO-1.5  = I/O supply voltage for LVCMOS15, HSTL_I
         VREF  = Reference voltage for indicated input standard
        *VREF  = Reference voltage pin selected by software
          GND  = Dedicated Ground Pin
          TDI  = Test Data In, JTAG pin
          TDO  = Test Data Out, JTAG pin
          TCK  = Test Clock, JTAG pin
          TMS  = Test Mode Select, JTAG pin
   PROHIBITED  = User reserved pin
 ***************************  Compiler Options  ***************************

Following is a list of all global compiler options used by the fitter run.

Device(s) Specified                           : xc2c128-7-VQ100
Optimization Method                           : DENSITY
Multi-Level Logic Optimization                : ON
Ignore Timing Specifications                  : OFF
Default Register Power Up Value               : LOW
Keep User Location Constraints                : ON
What-You-See-Is-What-You-Get                  : OFF
Exhaustive Fitting                            : OFF
Keep Unused Inputs                            : OFF
Slew Rate                                     : FAST
Set Unused I/O Pin Termination                : KEEPER
Global Clock Optimization                     : ON
Global Set/Reset Optimization                 : ON
Global Ouput Enable Optimization              : ON
Enable Input Registers                        : ON
Function Block Fan-in Limit                   : 38
Use DATA_GATE Attribute                       : ON
Set Tristate Outputs to Termination Mode      : KEEPER
Default Voltage Standard for All Outputs      : LVCMOS18
Input Limit                                   : 32
Pterm Limit                                   : 16
```

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