Pin Diagrams 20-Pin SSOP 18-Pin PDIP, SOIC RA0/AN0 ←→ 20 ■ RB3/CCP1/P1A ☐ → RB3/CCP1/P1A RA0/AN0 → □ 1 ◆ RB2/P1B/INT2 RA1/AN1/LVDIN ◀ 19 RB2/P1B/INT2 RA1/AN1/LVDIN ←→ 2 17 → OSC1/CLKI/RA7 RA4/T0CKI → 18 ☐ → OSC1/CLKI/RA7 16 RA4/T0CKI → PIC18F1X20 → OSC2/CLKO/RA6 MCLR/VPP/RA5-17 MCLR/Vpp/RA5 → OSC2/CLKO/RA6 PIC18F1X20 ____ VDD 5 16 - VDD/AVDD Vss/AVss -5 14 □ 🕶 **→** □ 6 AVDD AVss -15 RB7/PGD/T10SI/ RA2/AN2/VREF- → □ 6 13 RB7/PGD/T10SI/ P1D/KBI3 RA2/AN2/VREF-→ 14 RB6/PGC/T1OSO/ T13CKI/P1C/KBI2 P1D/KBI3 RA3/AN3/VREF+ → 7 12 🗆 🔫 RB6/PGC/T10SO/ RA3/AN3/VREF+◀ 13 T13CKI/P1C/KBI2 ➤ RB5/PGM/KBI1 8 RB0/AN4/INT0 → □ ► RB5/PGM/KBI1 RB4/AN6/RX/ RB1/AN5/TX/ → RB0/AN4/INT0→ 12 10 RB4/AN6/RX/ DT/KBI0 CK/INT1 RB1/AN5/TX/→ 10 11 DT/KBI0 CK/INT1 28-Pin QFN RA1/AN1/LVDIN RB3/CCP1/P1A RB2/P1B/INT2 RA4/T0CKI RA0/AN0 200 27 2 25 \\ 24 \\\ 23 \\\ 23 \\\ □ - OSC1/CLKI/RA7 MCLR/VPP/RA5 20 → OSC2/CLKO/RA6 NC 19 → VDD PIC18F1X20 18 → NC 17 → AVDD **AVss** 16 → RB7/PGD/T10SI/P1D/KBI3 NC **→** □6 15 → RB6/PGC/T10S0/T13CKI/P1C/KBI2 RA2/AN2/VREF- ← □7 RB4/AN6/RX/DT/KBI0 RA3/AN3/VREF+ RB0/AN4/INT0 RB1/AN5/TX/CK/INT1 20 RB5/PGM/KBI1