Improved Inverter Utilisation Using Third Harmonic Injection

Mr. JOBY JOSE, Prof. G.N.GOYAL and Dr. M.V.AWARE

Abstract—**In this paper, a comparative analysis of the carrier based pulse width with modified zero space vector modulation or third harmonics injection used in the inverter control is presented. The placement of zero space vector components with in the carrier interval determines the harmonic performance of the modulation strategy. The space vector pulse width modulated inverter gives 15 percent more line to line voltage as compared with the conventional sine pulse width modulated (SPWM) inverter. The optimized zero vector injection controls the blanking time and minimum pulse width of an operating inverter switch. The simulation results are presented for the three phase voltage source inverter to ascertain the effect of this technique. It is also tested on the laboratory prototype inverter to confirm the effectiveness of this modified SVPWM technique.**

Index Terms- **Sine pulsewidth modulation, space vector pulsewidth modulation, voltage source inverter, current harmonics.**

I. INTRODUCTION

PULSE WIDTH modulated (PWM) voltage source inverters (VSI's) are widely utilized in ac motor drive application. Many PWM-VSI drives employ carrier based PWM methods due to fixed switching frequency, low ripple current, and well-defined harmonic spectrum characteristics. But a pulse width modulated inverter employing pure sinusoidal modulation cannot supply sufficient voltage to enable a standard motor to operate at rated power and rated speed. Sufficient voltage can be obtained from the inverter by over modulating, but this produces distortion of the output waveform. The linear output range of SPWM is restricted to 0.785 compared with six step inverter. The non-linear region operation (over-modulation) is leading to large amounts of sub carrier frequency harmonic currents, reduction in fundamental voltage gain and switching device gate pulse dropping. In variable speed v/f controlled PWM-VSI induction motor drives, operation in this range results in poor performance, and frequent over current faults conditions [1].In current controlled drives, in addition to the inherent modulator sub carrier frequency harmonic-distortion dependent waveform degradation, current–regulator dependent performance reduction results. Also, full inverter voltage utilization is restricted which is important from cost and power density improvement prospective. The voltage can be increased by harmonic suppression [2] for the rectifiers as well as inverters. This can be mainly done by injecting the third harmonic [3]-[6]

In recent past space vector pulse width modulation (SVPWM) is developed and widely used for three phase PWM inverter and the multilevel inverter [7]-[9]. In three phase PWM inverter SVPWM technique gives 15.5% higher output voltage and lower harmonic distortion than the conventional SPWM method [1],[10],[8]. It has been generally reported that space vector modulation strategies offer superior performance compared to regular sampled pulse width modulation, in terms of reduced harmonic current ripple, optimized switching sequence and increased voltage transfer ratios [11]. The main difference between regular sampled and space vector modulation is that the placement of the active space vector components in each half carrier interval and that therefore any harmonic difference between these technique must be only attributed to this placement. The SVPWM is also used for controlling the multiphase inverter with ANN [12].

In this paper, analogue space vector modulator is proposed. The appropriate placement of active and zero space vector components within the modulation strategy is adopted This ZSVPWM control inverter increases the output voltage up-to 15.5 % without any pulse dropping or any other form of over modulation.

This paper contributes for the analysis and comparison of the Zero Space Vector PWM (ZSVPWM) with respect to the conventional SPWM technique using MATLAB/SIMULINK. The performance of the designed circuit is presented with the hardware results on a 2 kW laboratory prototype.

II. ZERO SPACE VECTOR MODULATION

The standard topology of three phases VSI is shown in fig.1, which consists of three phase legs with two switches per leg, arranged so that each phase output can be connected to either the upper or the lower dc has desired. The process of PWM determines the duty cycle for each phase leg.

Mr. Joby Jose is with Department of Electrical Engineering, Visvesvaraya National Institute of Technology Nagpur as a research student (E-mail:jobyproject@yahoo.com).

Prof. G.N.Goyal is with Department of Electrical Engineering, SRKNEC, Nagpur, Maharashtra, India as a Assistant Professor (E-mail: gaurav.goyal13@gmail.com).

Dr. M.V. Aware is with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, Maharashtra, India as a Professor (E-mail: mva_win @ yahoo.com).

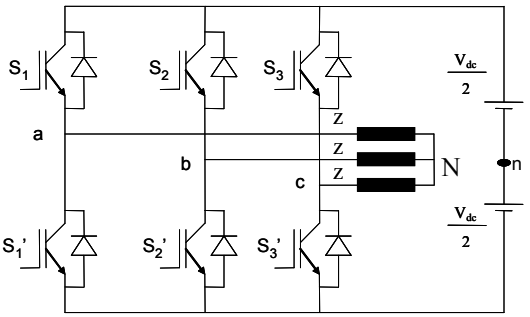

Fig.1. Topology of voltage source inverter

In regular sampled PWM, [10] the upper phase leg switching periods in each half carrier interval have been given as

$$\left.\begin{aligned} m_1(t) &= \frac{m'}{2}\left\{\cos(w_o t) - \frac{1}{6}(3w_o t)\right\} + \frac{1}{2} \\ m_3(t) &= \frac{m'}{2}\left\{\cos(w_o t - 2\pi/3) - \frac{1}{6}(3w_o t)\right\} + \frac{1}{2} \\ m_5(t) &= \frac{m'}{2}\left\{\cos(w_o t + 2\pi/3) - \frac{1}{6}(3w_o t)\right\} + \frac{1}{2} \end{aligned}\right\} \quad (1)$$

Where 0<m'<1.5 when a common mode third harmonic of $1/6^{th}$ of the reference magnitude is added at each reference wave form to achieve the maximum possible voltage transfer ratio

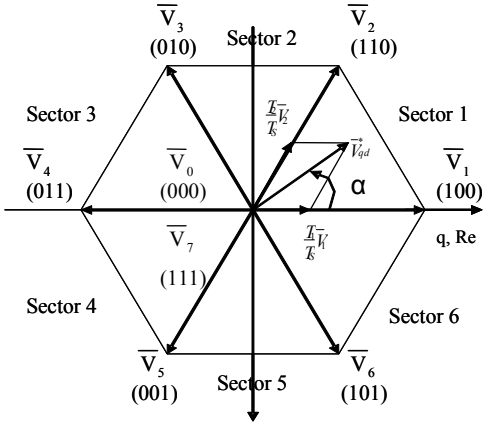

Fig 2: Phasor representation of inverter voltage

In the space vector modulation, the duty cycle for each phase leg that is required to generate a sampled target phasor by selecting at each sample time the nearest two of the six active space vector combinations for three phase VSI as shown in fig. 2, for some of the half carrier period ΔT/2, and filling in the reminder of the period with zero space vectors ($T_0/2$) as shown in fig 3.The fractional period of each active space vector depends on the modulation depth. The space vector modulation strategy in placement and order of the active space vectors within the switching period and it is these additional degree of freedom which gives noise to difference in the harmonic performance of space vector sampled carrier modulation strategies.

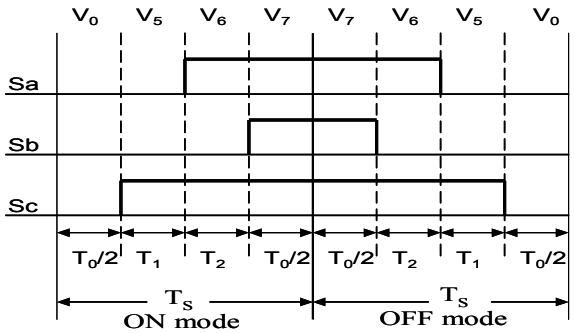

Fig.3.Switching pulses pattern (in sector V)

A. Zero space vector modulation

The main function of any PWM strategy is to identify the active pulse width within each carrier interval which contributes the same fundamental volt-second average is the original target reference waveform over that interval. The pulse placement for 50% duty cycle voltage applied to the inductive load. The average current is zero in both the cases, the current ripple magnitude when the pulses are centered in the carrier interval is significantly less than the current ripple magnitude which occurs when the pulses are positional back to span across two carrier intervals as shown in the fig.4. The modulation strategies which place their switched pulses closer to the center of each carrier interval have a superior harmonic performance compared to those which do not center the pulses, irrespective of how the switched pulse width is calculated to achieve this improved pulse placement is to add a common mode third harmonic of ¼ reference magnitude [10], instead of 1/6 as describe before. This approach centers the space vector pulses at 30^0 steps during the fundamental cycle with minor deviations from the center within each 30^0 interval. The maximum possible modulation range without saturating is slightly reduced to 0<m'<1.12 under this modulation strategy [10].

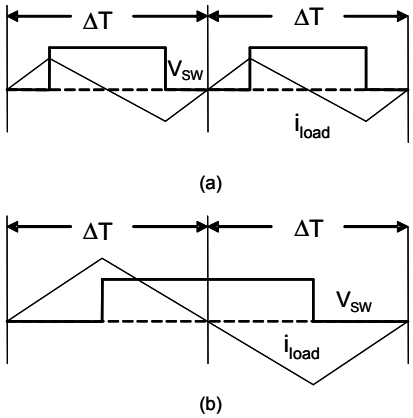

Fig.4. (a) Best case placement of active voltage pulses within carrier interval (b) Worst case placement of active voltage pulses within carrier interval

B. Voltage Gain comparison

The modification of modulating waveform to increase the inverter voltage gain requires the addition of one-sixth of third harmonics. The effect of reducing the peak value of the output waveform by a factor of 0.866 without changing

the amplitude of the fundamental. The fig.6 (b) illustrated the modified reference modulating waveform. It is possible to increase the amplitude of the modulating wave by a factor K, so that the full output voltage range of the inverter is again utilized [10].

The generalized modulating waveform become

$$V = K(\sin \omega t + \frac{1}{6}\sin 3\omega t) \quad (2)$$

The factor K for the peak value unity with 0.866 factors gives

$$1 = K \times 0.866 \Rightarrow K = 1.155 \quad (3)$$

This indicates 15.5 percent increase in the amplitude fundamental of the phase voltage waveform. When minimum pulse width limitations are taken into consideration, line waveform is undistorted since the third harmonic components in the phasor waveform gets cancel.

III. Design of ZSVPWM control

A. Calculation of optimum distortion

The generation of the phase voltage waveform having no third harmonics can be generated by addition of the third harmonics in the sinusoidal reference waveform. These additions of the various amounts of third, ninth, fifteenth etc. harmonics is used to produce flat-tapped phase waveforms which improves the efficiency of the class B inverters. The optimal amount of each third harmonic should extend the ratings of all PWM inverters. The best modification that can be made to the inverter phase output waveform is assumed a priori to be the addition of a measure of third harmonics. The desired waveform of the type

$$y = \sin \omega t + A \sin 3\omega t \quad (4)$$

Where A is to be determined for the optimal of Y, this can be obtained as

$$\frac{dy}{dt} = \cos \omega t + 3A \cos 3\omega t = 0 \quad (5)$$

The maxima & minima of the waveform therefore occur at

$$\cos \omega t = 0 \quad \text{And} \quad \cos \omega t = (\frac{9A-1}{12A})^{1/2} \quad (6)$$

$$\text{For } \sin \omega t = 1 \quad \text{and} \quad \sin \omega t = (\frac{1+3A}{12A})^{1/2} \quad (7)$$

Manipulating the (4) using identity, we get

$$y = (1+3A)\sin \theta - 4A \sin^3 \theta \quad (8)$$

Substituting the values of $\sin \theta$ obtained in (7), we get

$$\hat{y} = 1 - A \quad \text{and} \quad \hat{y} = 8A(\frac{1+3A}{12A})^{\frac{3}{2}} \quad (9)$$

The optimum value of A is that value which minimizes $\hat{y}$ and can be found by differentiating the expression for $\hat{y}$ and equating it to zero.

Thus the values of A are

$$A = \frac{-1}{3} \quad \text{And} \quad A = \frac{1}{6}$$

The value of $\hat{y}$ cannot be greater than unity for this reason we discard the value A=-1/3. The required value of A is therefore 1/6, and the required waveform is

$$y = \sin \theta + \frac{1}{6}\sin 3\theta \quad (10)$$

B. Zero sequence component generator

The zero sequence voltage generator comprises of three-phase Diode Bridge and an inverting adder. The voltages at the output of the bridge are given by V_A & V_B, along with the output voltage of the inverting adder is shown in the fig.5.

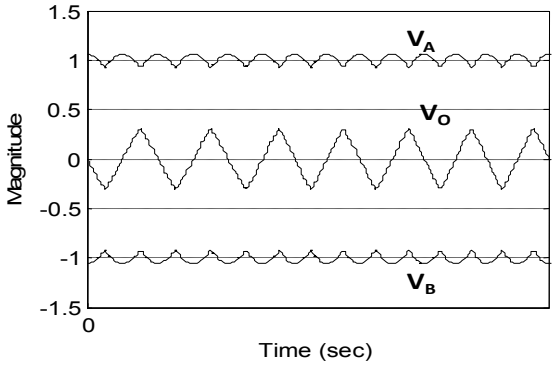

Fig. 5: Input and output voltage of zero sequence voltage generator

C. Generation of Switching Signals

The general block diagram for generation of the switching pulses is shown in the fig.6 (a). The reference voltage V_{ref} is added with signal having frequency three times of fundamental frequency and the magnitude is $1/6^{th}$ of the fundamental amplitude. The resultant is then passed through comparator which compares the modified signal with the carrier signal of frequency 2 KHz. In the fig.6 (b) the combination of all the three signal is been shown.

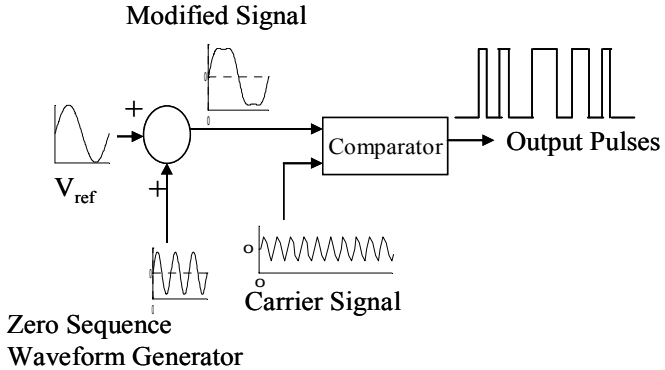

Fig. 6(a) Block diagram for generation of SVPWM pulses

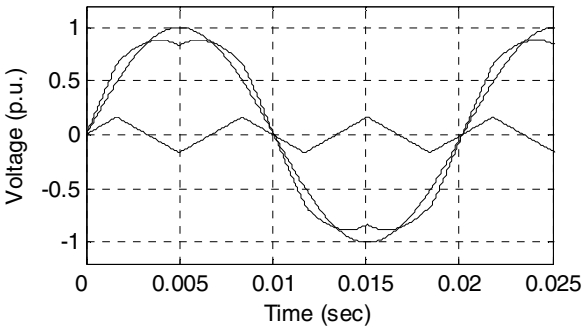

Fig.6 (b) Waveform of fundamental signal, Third harmonic signal and resultant

The output pulses of the fig.6 (a) are passed through deadband circuit and the driver circuit before applying to the inverter. The general block diagram for generation of the gating signal is shown in the fig 7. The Dead band circuit is used to introduce a dead time in the pulses to avoid short-circuit of the switches of the same leg of the inverter, and the optocoupler circuit is to provide isolation between control circuit and the power circuit.

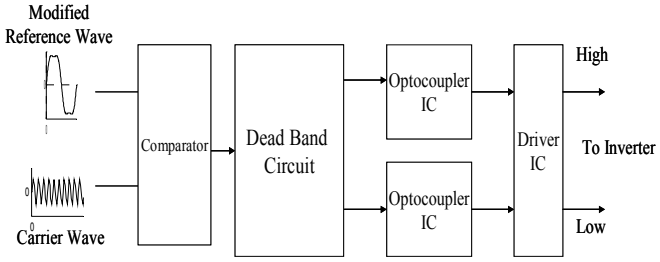

Fig.7 Block diagram for switching signal generators

IV. Performance Simulation

A. Generation of SPWM

The fig.8 (a) shows the carrier and the reference waveform for generation of SPWM. The pulses obtained are shown in fig.8 (b). The harmonic analysis of the SPWM is shown in the fig.8 (c). It is observed from fig.8(c) that the magnitude of the third harmonic is present and the total harmonic distortion in the voltage waveform is 13.47%.

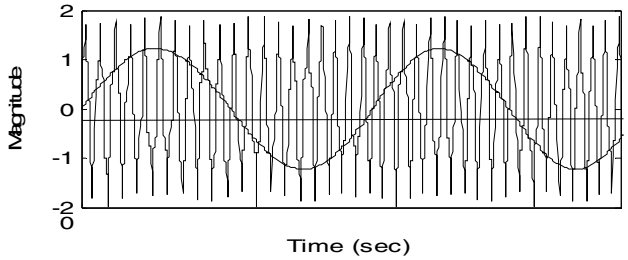

Fig.8 (a): Carrier and Reference waveform for SPWM for Ma=0.85
Carrier Frequency= 2kHz, Reference Frequency=50Hz

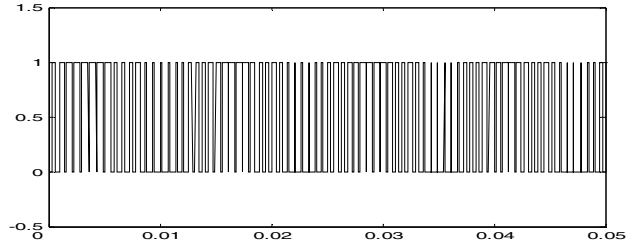

Fig. 8(b): SPWM Pulses

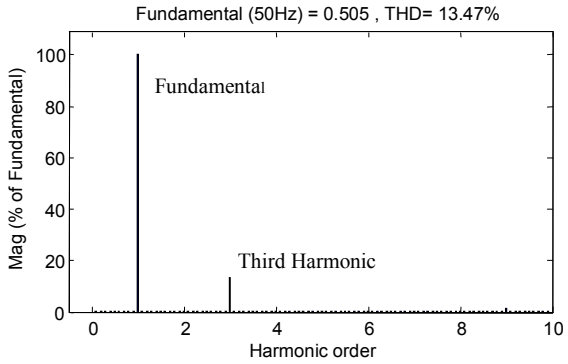

Fig.8(c): FFT Analysis of SPWM Voltage

B. Generation of SVPWM

The fig.9 (a) shows the carrier and the modified reference waveform. The modified reference waveform is obtained by addition of zero sequence voltage to the reference wave as shown in fig.6 (b). The SVPWM pulses are shown in the fig.9 (b). The harmonic analysis of the voltage waveform is shown in the fig.9(c). It can be observed from fig.8(c) and fig.9(c) that the magnitude of the third harmonic has been considerably reduced in case of SVPWM and the THD of the voltage waveform is 0.26%.

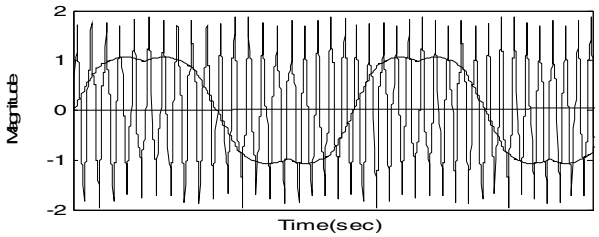

Fig.9 (a): Carrier and Reference waveform for SVPWM
Carrier frequency = 2kHz, Modified Reference frequency= 50Hz

Fig.9 (b): SVPWM pulses

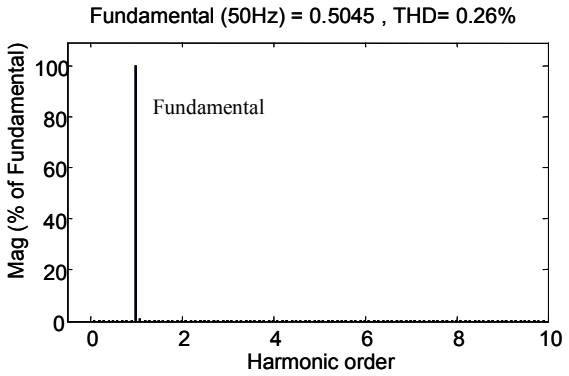

Fig.9(c): FFT Analysis of SVPWM Voltage

A comparative analysis is done between the phase voltage of SVPWM and SPWM as shown in Table-II. It can be observed from the Table-II that the increase in the phase voltage is almost equal to 15.5 percent as derived in (3)

TABLE- II
COMPARATIVE ANALYSIS FOR INCERESE IN PHASE VOLTAGE

DC Voltage	Phase Voltage		Increase in voltage
	SVPWM	SPWM	
50 V	19.58 V	16.96 V	15.45 %
100 V	39.98 V	34.62 V	15.48 %
150 V	60.38 V	52.29 V	15.47 %
200 V	80.77 V	69.96 V	15.45 %

V. EXPERIMENTAL RESULTS

Experiments were carried using SPWM and SVPWM on induction motor as load. The frequency of the inverter is 2 KHz. The MOSFET IRF 840 is used as switching devices. The dead time in the inverter is as 20μs.

TABLE- I
LAB MODEL (HARDWARE DETAILS)

Switching Frequency	2KHz
MOSFET (IRF 840)	8A,500V
DC Link Voltage	100V
Capacitor	1000μF, 126V

A. Carrier waveform generation

The carrier waveform obtained from the operational amplifier circuit is shown in the fig.10. The frequency and the amplitude of the triangular wave are set as 2 KHz and 2V (peak to peak) respectively. The same carrier signal is used for the pulse generation in both SPWM and SVPWM.

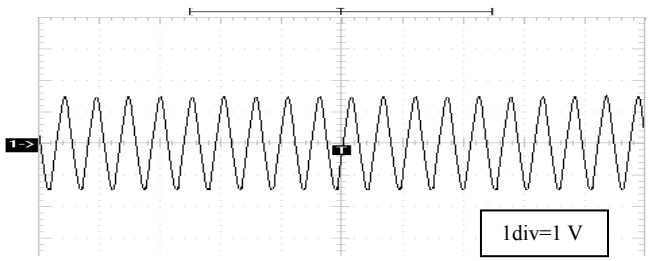

Fig.10: Carrier Waveform (frequency = 2kHz)

B. Voltage and Current Waveforms for SPWM

In the fig.11 (a) the current and the voltage waveforms obtained from the inverter when fed with the SPWM pulses are shown. The current waveform contains some harmonic distortion in the form of spikes i.e. overshooting of the magnitude. The frequency of both current and voltage is 50Hz that can be observed from the waveform.

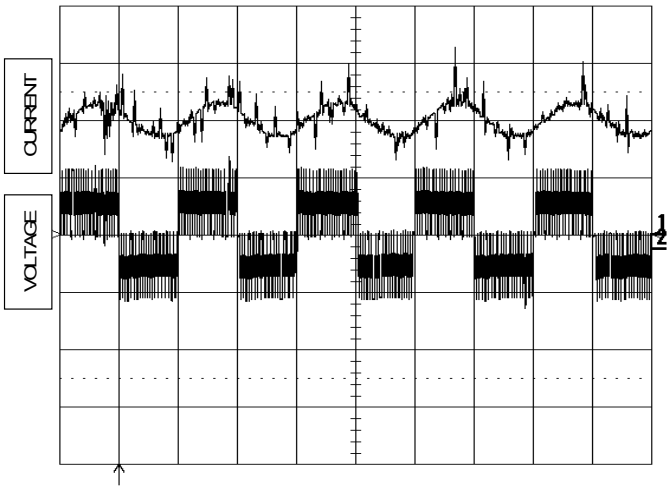

Fig.11 (a): Current and Voltage waveform of SPWM
(1.Voltage Scale -200V/div 2.Current Scale- 5A/div)

In the fig.11 (b) the harmonic spectrum of the current waveform of the inverter fed induction motor is obtained. The analysis shows that the third harmonic component exists in the current obtained from SPWM.

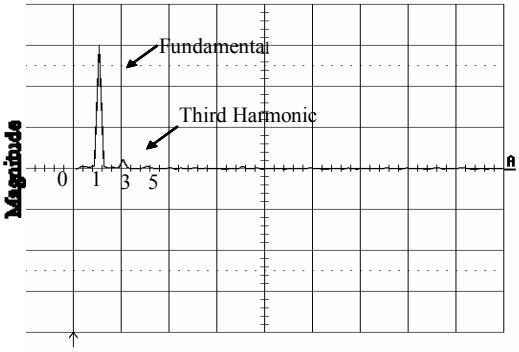

Fig.11 (b): FFT analysis of current waveform of SPWM

C. Current and Voltage waveforms for SVPWM

The zero sequence component and the reference waveforms has been shown in the fig.12 (a). Also the modified reference waveform to be modulated is shown in fig.12 (b)

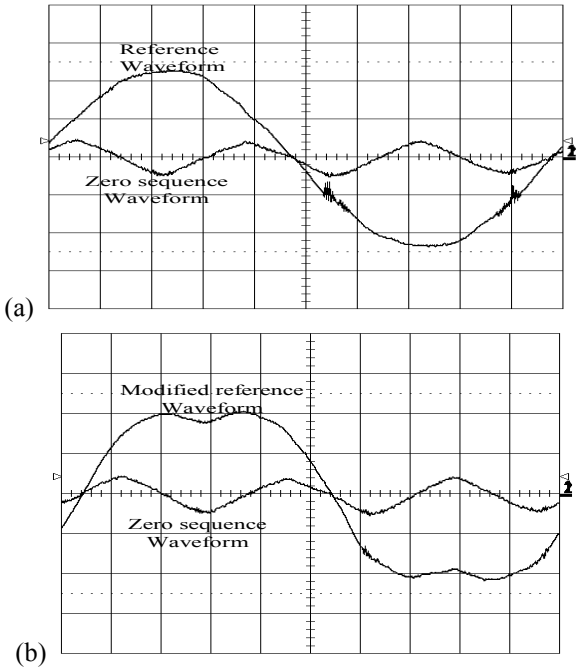

Fig.12 (a) Reference Waveform and Zero Sequence Waveform
(b) Modified Reference Waveform and Zero Sequence Waveform
(Frequency : Ref. Waveform & Modified Ref. Waveform = 50Hz
Zero sequence waveform = 150Hz)

In the fig.13 (a) the current and the voltage waveform of the inverter fed induction motor drive is shown. The harmonic spectrum is observed which is shown in the fig.13 (b). It can be observed from the fig.13 (b) that the third harmonic component is reduced to an extent.

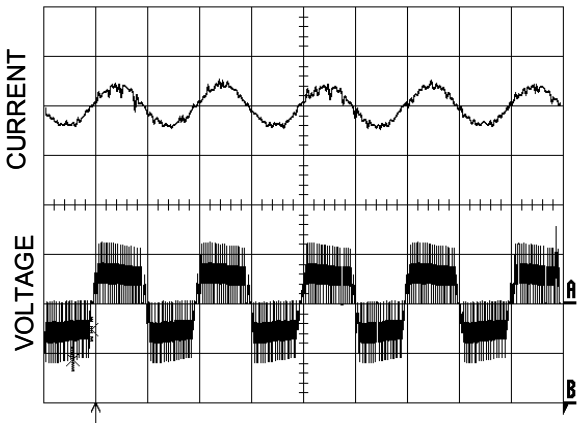

Fig.13 (a): Current and Voltage waveform of SVPWM
(1.Voltage Scale -200V/div 2.Current Scale- 5A/div)

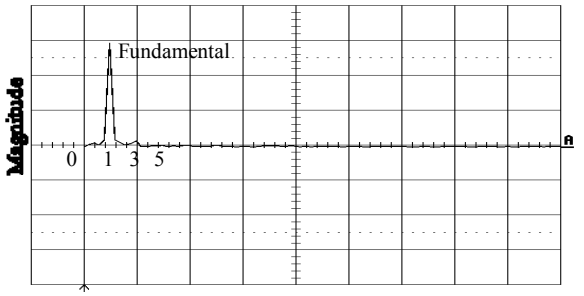

Fig 13(b): FFT analysis of current of SVPWM

VI. CONCLUSIONS

The optimum value of the magnitude of the zero sequence current has been derived and it should be equal to one-sixth of the original reference waveform. The hardware and simulation results have been shown for the zero sequence voltage and the modified reference waveform to increase the line to line voltage by 15 percent. The generated output voltage and the current are analyzed. The results of the FFT indicated the reduction of 3rd harmonic in the output voltage. Thus it gives effective utilization of the inverter and enhancement of rms content of the output voltage

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